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METAL-*N*-TYPE SEMICONDUCTOR OHMIC CONTACT WITH A SHALLOW N^+ SURFACE LAYER

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Abstract—Most papers covering metal-semiconductor ohmic contact theory which have been published up to date consider systems with homogeneous impurity concentration in the semiconductor. However, there are techniques of ohmic contact formation on nondegenerate semiconductor where only a very shallow surface layer is impurity enriched. In this paper a model of such contacts is proposed and a simple approximate analytical expression for the specific resistivity is derived. If the impurity concentration in the surface layer is very high, the contact specific resistivity is essentially proportional to N_B^{-1}, N_B being the semiconductor substrate impurity concentration. To make a good ohmic contact, it is sufficient that the width of the heavily doped surface layer be equal to the equilibrium contact depletion region width. Any further enlargement of the enriched layer practically does not influence the total sample resistance due to the dominant share of the semiconductor body resistance. Experimental results confirm these conclusions qualitatively.

NOTATION

Ai^* effective Richardson's constant
Ao Richardson's constant
d contact diameter
$E_b = \phi_c + \varphi_{F^+}$ built-in barrier potential
E_{CB} energy of the bottom of the conduction band in the semiconductor bulk
E_{CN^+} energy of the bottom of the conduction band in the layer with $N(x) = N^+$
E_F Fermi level
E_t characteristic energy
E_x electron energy corresponding to the motion normal to the metal-semiconductor interface, measured with reference to E_{CB}
E_{00} constant given by eqn. (6)
E_{11} constant given by eqn (8)
h Planck's constant
J contact current density
J_s saturation current density
k Boltzman's constant
K_d semiconductor relative dynamic dielectric constant
K_S semiconductor relative static dielectric constant
m_o free electron mass
m_t, m_l transverse and longitudinal effective electron masses, respectively
m_x electron effective mass for tunnelling along x-axis
N^+ donor impurity concentration in the semiconductor surface region
N_B donor impurity concentration in the semiconductor bulk
N_C effective density of states in the semiconductor conduction band
n_m equivalent minima number of the semiconductor conduction band
q electric charge of the electron
$qV_m = \phi_c + \varphi_{FB} - \Delta\varphi$ potential barrier height seen by the electrons at the bottom of the conduction band in the semiconductor bulk
R_c contact resistance
R_w sample series resistance
R_o rear contact resistance
T absolute temperature
t sample thickness
t_D diffusion time
V contact voltage drops
V_{FB} flat-band voltage of a MOS structure
w_{n^+} equilibrium contact depletion layer width if $N_{(x)} = N^+$
x_{n^+} heavily doped surface layer width
α linear coefficient of the phosphorous penetration
ϕ_c metal-semiconductor barrier height, neglecting barrier lowering
$\varphi_{F^+} = E_F - E_{CN^+}$
$\varphi_{FB} = E_F - E_{CB}$
μ electron mobility
ρ_c specific contact resistivity
ρ_B semiconductor bulk resistivity.

1. INTRODUCTION

Since the pioneer work of Kröger *et al.*[1], who first suggested tunnelling through the barrier as a model for describing the metal-semiconductor ohmic contact characteristics, many papers on this subject have been published. All of them treated metal-semiconductor contact with homogeneous impurity concentration near the interface. However, there are techniques of making metal-nondegenerate semiconductor ohmic contacts where only a shallow surface layer of the semiconductor is more heavily doped than the bulk. This is the case when the metal of the contact acts as the impurity of the same type as the impurity in the substrate. During the sintering process of such contacts, a very shallow diffusion of metal atoms into semiconductor surface region takes place. For instance, this is the situation with ohmic contacts formed on *P*-type silicon with Al or Au–Ga alloy, and on *N*-type silicon with Au–Sb alloy or electroless deposited Ni (containing phosphorus), etc. The same phenomenon is observed when, prior to metallization, the shallow semiconductor surface layer is impurity enriched[2].

In all above examples, the ohmic contact model based

on the assumption of homogeneous impurity concentration near the semiconductor surface is not adequate. The reasons for this are the following: (1) the shape of the contact barrier depends on the impurity concentration and the width of the enriched surface layer. It is certainly different from that corresponding to the impurity concentration in the bulk; (2) even if the width of the enriched layer is greater than the depletion region width, the contact need not behave as having homogeneous impurity concentration equal to that of the enriched layer. Indeed, if the part of the enriched layer width outside the barrier is smaller than the carrier free path in this region, the carriers would pass through it practically without scattering. That means the carriers will communicate directly between the less doped semiconductor substrate and the metal via energy levels above the bottom of the substrate conduction band.

An analysis of some properties of the metal-semiconductor contact with a thin heavily doped surface region has been reported recently[3]. However, these considerations were limited to the case where the width of the heavily doped layer was smaller than the depletion region width, so that contact still behaved like a Schottky diode. The present paper deals with the case where the heavily doped surface layer width is equal to or greater than the barrier width. As indicated in[3], this leads to disappearing of the contact rectifying properties. An analysis of the potential energy dependence on the depth of the enriched layer is carried out and the area of application of the present theory is defined. An approximate analytic expression for the specific contact resistivity is then derived. Finally, experimental results in qualitative agreement with the theory are presented.

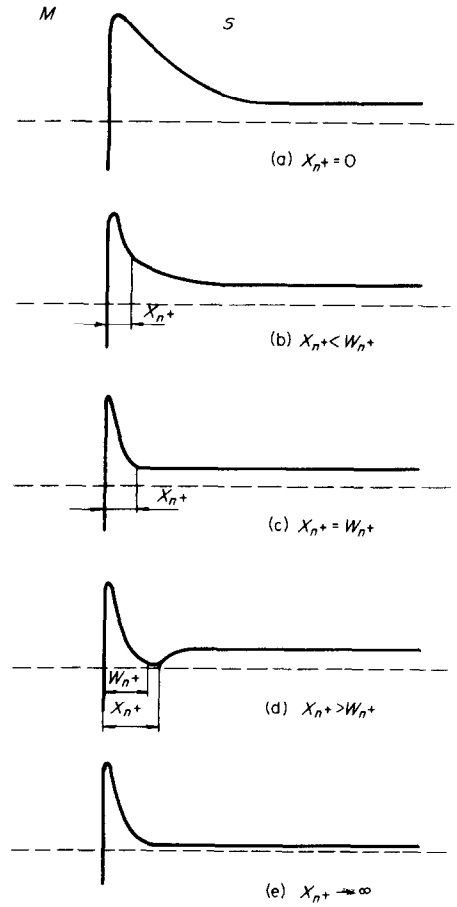

Fig. 1. The shapes of the equilibrium potential barriers for some typical values of the heavily doped layer width.

2. ENERGY DIAGRAMS AND QUALITATIVE ANALYSIS

Consider the potential energy diagram of metal N-type semiconductor contact, when there are two regions in the semiconductor having different impurity concentrations:

$$N(x)=N^+, X\in(0,X_{n^+})$$
$$N(x)=N_B, X\in(X_{n^+},\infty) \quad (1)$$

with $N^+\gg N_B$. The shapes of the equilibrium barriers for some typical values of X_{n^+} are shown in Fig. 1.

The potential energy shape of the metal-semiconductor contact with a homogeneous impurity concentration is shown in Fig. 1(a). This is an example of the well-known Schottky barrier. Figure 1(b) shows the case when the enriched layer depth is smaller than the equilibrium depletion region width corresponding to impurity concentration N^+. The depletion region spreads out of the heavily doped layer, and the surface barrier has two regions with different gradients of the potential energy. This case has been elaborated in[3]. Figure 1(c) shows the boundary case when the enriched layer width is just sufficient to accomodate the depletion region. In Fig. 1(d), the depth of the heavily doped layer is greater than the depletion region width, so there is a part of it outside the barrier. Consequently, a potential well appears behind the barrier. Finally, Fig. 1(e) shows the same situation as Fig. 1(a) except that the impurity concentration is high. This is normally the case for ohmic contacts.

Further considerations will be based on Fig. 1(c) and 1(d), i.e. the impurity enriched surface region is sufficiently wide that the whole of the depletion region, corresponding to a given barrier height and impurity concentration N^+, can be placed in it. Additionally, it is assumed that $x_{n^+}\ll\lambda_{n^+}$.

It is intuitively clear that, for case (b) with $X_{n^+}\to 0$, the specific contact resistivity should increase rapidly, approaching that of structure (a), because practically only the electrons in energy levels higher than $V(X_{n^+})$ are capable of communicating between the metal and the semiconductor. On the other hand, for case (d), when X_{n^+} increases, the specific contact resistivity should approach that corresponding to case (e). This will happen because with X_{n^+} increasing, an increasing number of electrons is subjected to scattering while passing through the N^+ layer, thus getting a chance to communicate with the metal on energy levels below E_{CB}.

In Fig. 2, the potential energy diagram corresponding to that of Fig. 1(d) is shown, with all details and symbols that will be used in the further analysis. Note the potential barrier lowering, designated in the figure by $\Delta\varphi$. To explain this phenomenon, two models have been proposed: (1) the effect of image charge force[4], and (2) the

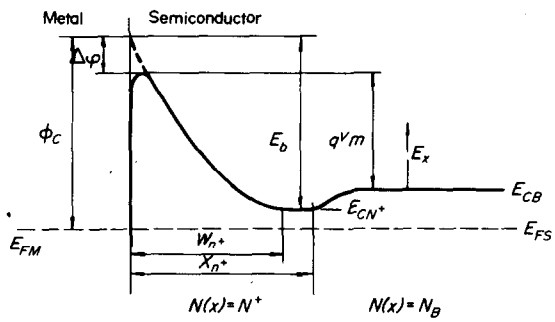

Fig. 2. The detailed contact potential energy diagram corresponding to that in Fig. 1(d).

influence of the space charge due to the quantum mechanical tunnelling of the electrons from the metal into the semiconductor [5, 6]. The first model will be used for two reasons: (1) it is mathematically simpler, and (2) both models lead to very similar numerical values of the specific contact resistivity (see [7, 8])

3. SPECIFIC CONTACT RESISTIVITY

The specific contact resistivity is defined by

$$\rho_c = \left(\frac{\partial J}{\partial V}\Big/ V=0\right)^{-1}. \tag{2}$$

The explicit expression for ρ_c will be derived on the basis of the low-temperature approximation of the $V-I$ characteristic of nondegenerate Schottky diode [12, 13].

$$J = J_s\left[\exp\left(\frac{qV}{E_t}\right) - \exp\left(qV\left(\frac{1}{E_t}-\frac{1}{kT}\right)\right)\right] \tag{3}$$

$$J_s = n_m A_f^* T^2 \exp\left(-\frac{\phi_c-\Delta\varphi}{E_t}\right)\cdot\left(\frac{N_c}{N_B}\right)^{kT/Et-1}\cdot\frac{E_t}{E_t-kT}. \tag{4}$$

The above two follow from the theory of thermionic emission of contact [9], taking into account the quantum-mechanical effects via a generalized WKB approximation [10]. The barrier has been approximated by parabola best fitting the top of the barrier [11]. Since the whole of the barrier is located within the N^+ layer, the characteristic energy E_t is defined by [11]:

$$E_t \simeq \frac{E_{00}}{\pi}\left(8\frac{E_b}{\Delta\varphi}\right)^{1/2} \tag{5}$$

$$E_{00} = \frac{qh}{4\pi}\left(\frac{N^+}{m_x K_S \epsilon_0}\right)^{1/2} \tag{6}$$

$$\frac{E_b}{\Delta\varphi} \simeq \left[\pi\left(\frac{E_b}{E_{11}}\right)^{3/2}\right]^{1/2} \tag{7}$$

$$E_{11} = \frac{q^2}{2\epsilon_0}\left(\frac{N^+}{K_S K_d^2}\right)^{1/3}. \tag{8}$$

The effective Richardson's constant, appearing in eqn (4), is given by

$$A_f^* = A_o\frac{m_t}{m_o}\left(\frac{m_l}{m_x}\right)^{1/2}. \tag{9}$$

Equations (3) and (4) have been derived applying Maxwell–Boltzmann statistics. Although the analyzed structure contains a thin layer of highly doped crystal, this approximation applies since the model implies that only carriers having energies greater than E_{CB} contribute to the charge transport. These carriers, as pointed out in Section 2, are non-degenerate. It should be emphasized that eqns (3) and (4) are valid only if $kT/E_t < 1$. It may easily be calculated that this condition is satisfied over the whole temperature range of interest if $N^+ > 10^{19}\,\mathrm{cm}^{-3}$.

The current density depends upon the applied voltage explicitly, as defined by eqn (3), but also implicitly via dependences of E_t (eqn 5), and $\Delta\varphi$ (eqn 7). If these implicit influences are neglected, the differentiation of eqn (3) by V gives:

$$\rho_c \simeq \frac{k\left(1-\frac{kT}{E_t}\right)\exp\left(\frac{\phi_c-\Delta\varphi}{E_t}\right)}{qn_m TA_f^*}\left(\frac{N_c}{N_B}\right)^{1-kT/Et}. \tag{10}$$

At low temperatures, or very high concentrations in the enriched layer, $kT/E_t \to 0$, and eqn (10) becomes:

$$\rho_c \simeq \frac{k\exp\left(\frac{\phi_c-\Delta\varphi}{E_t}\right)}{qn_m TA_f^*}\frac{N_c}{N_B}. \tag{11}$$

Figure 3 shows the dependences $\rho_c(N_B, N^+)$ computed by means of eqn (10) for silicon with surface orientation (111) and barrier height $\phi_c = 0.7\,\mathrm{eV}$. Numerical values of constants used in these calculations are given in Table 1:

Table 1. Numerical values of constants for (111) oriented N-type silicon, $T = 300\,\mathrm{K}$

Constant	Value	Reference
m_x	$m_x(N^+)$	[7]
m_t	$0.19\,m_o$	[8]
m_l	$0.97\,m_o$	[8]
K_S	11.8	[14]
K_d	11.8	[14]
n_m	6	[8]
N_c	$2.8\cdot 10^{19}\,\mathrm{cm}^{-3}$	[14]

Note that if impurity concentration in the substrate increases, the contact resistivity of the structure approaches the value corresponding to the crystal with homogeneous impurity concentration equal to N^+ (e.g. see [7]).

4. EXPERIMENTAL RESULTS

4.1 *Measurement method*

Measurement of the contact resistance of the described structure can not be performed by direct application of any of the known measurement methods. These methods imply that the contact resistance is greater than the parasitic resistance of the test sample. In the present case, as can be seen on Fig. 3, a large contribution to the measured value should be expected to come from the crystal body resistance. Due to that, even small relative errors in calculating the substrate resis-

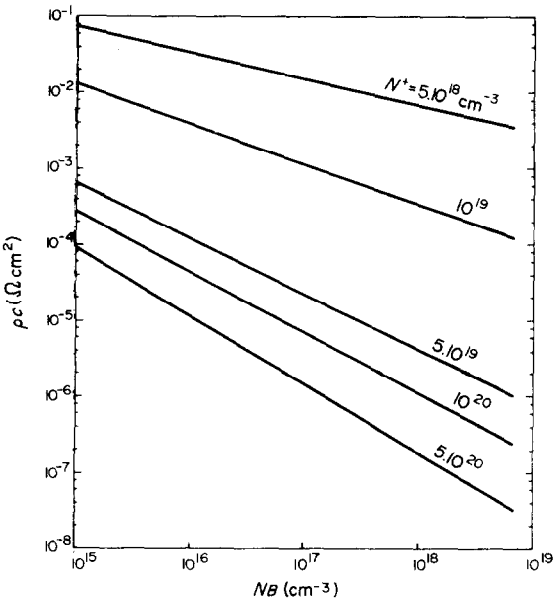

Fig. 3. The theoretical specific contact resistivity of the metal–N^+N silicon contact, for different surface doping levels N^+, vs substrate impurity concentration.

tance may be greater than the contact resistance. However, it turned out that it was possible, at least in principle, to achieve an arbitrarily high ratio of the contact-to-substrate resistance simply by optimization of the test-sample geometry. Indeed, consider the test-sample of Fig. 4, corresponding to the measurement method with a vertical current flow[15]. The total measured resistance is

$$R = R_c + R_w + R_o. \tag{12}$$

For a circular contact geometry and uniformly doped substrate of resistivity ρ_B and width t, it is[15]:

$$R_c = \frac{\rho_c}{\pi d^2/4} \tag{13}$$

$$R_w = (\rho_B/d\pi)\,\text{arc}\,tg(4t/d). \tag{14}$$

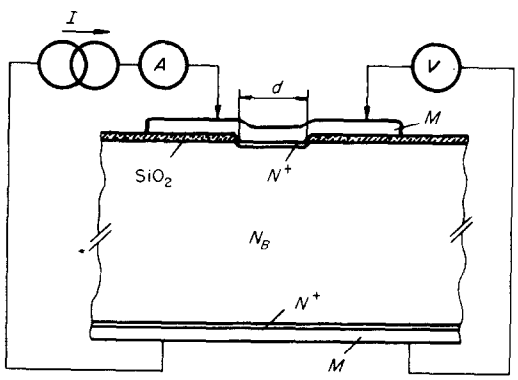

Fig. 4. The test sample and circuit for contact resistivity measurement.

Since

$$\lim_{d/t\to 0}\frac{2}{\pi}\,\text{arc}\,tg\,\frac{4}{d/t} = 1, \tag{15}$$

it follows that

$$\lim_{d\to 0}\frac{R_c}{R_w} = \lim_{d\to 0}\frac{8\rho_c}{\pi\rho_B d} = \infty. \tag{16}$$

Hence, the relative influence of the substrate parasitic resistance decreases as the diameter of the contact decreases. The ratio R_c/R_w for small but finite contact diameter is:

$$\frac{R_c}{R_w} \simeq \frac{8}{\pi d}\,\frac{k\exp((\phi_c-\Delta\varphi)/E_t)N_c}{n_m T A_t^*}\,\mu, \tag{17}$$

where the use is made of eqn (11) and

$$\rho_B = (q\mu N_B)^{-1}. \tag{18}$$

Finally,

$$\frac{R_c}{R_w} \sim \frac{\mu}{d}. \tag{19}$$

Therefore, in order to minimize the error resulting from the influence of the substrate resistance, the contact area of the test sample should be as small as possible, and, in order to increase the mobility, the impurity concentration in the substrate—as low as possible. Unfortunately, even if these precautions were taken, it is not easy to identify the contact resistance. An estimate of R_c and R_w, using diagram in Fig. 3 and eqns (13) and (14), gives at room temperature:

$$R_c = 1.53\,\text{K}\Omega,\ R_w = 4.9\,\text{K}\Omega,$$

for $N_B = 10^{15}$ cm^{-3}, $\rho_B \simeq 4.9\,\Omega$cm, $N^+ = 10^{20}$ cm^{-3} and $d = 5\,\mu$m.

This shows that the measurement is rather difficult even with optimized sample geometry. Consequently, in what follows only a qualitative experimental check of the theoretical results will be considered.

4.2 *Device fabrication*

The model of the contact considered here contains in the surface region a thin layer of homogeneous, high impurity concentration. The technology that could be used to meet such requirements is alloying. Because of the very poor control of geometry in alloying, the use is made of shallow diffusion profiles obtained by low-temperature phosphorus diffusions in silicon, reasonably resembling the "square" distributions[16].

The process of sample preparation was as follows: commercially available, polished, (111) oriented N-type silicon wafers of resistivities 4–6 Ωcm were used. Wafers were cleaned by standard procedure and steam oxidized at 950°C, for 30 min. Circular windows 5 μm in diameter were etched in the oxide by the photolithographic process. Wafers were then separated into several lots

and each of them was subjected to phosphorus deposition from $POCl_3$[17] at 850°C, for different deposition times. Gas flow rates were adjusted to provide conditions for a high phosphorus glass deposition rate, e.g. the exceptionally anomalous impurity concentration profiles: $N_2 = 1500\,cm^3/min$ and $O_2 = 200\,cm^3/min$ (by pass) and $N_2 = 60\,cm/min$ (through bubbler). Phosphorus glass was then removed and aluminium was vacuum evaporated. Metal patterns were then defined by photolithography, Fig. 4. After that, the wafers were annealed in 20% H_2 – 80% N_2 gas mixture for one hour at 250°C. According to the results of Ref.[18], under these conditions Al–Si contact is made almost completely free of interface states and oxide layer, without any dissolution of Si in Al. In addition, both the interface state density and the fixed positive charge density at the Si–SiO_2 interface simultaneously decrease. This makes the conditions at the surface approach the ideal ($V_{FB} \simeq 0$), as assumed while deriving relation (14) for R_w. The measurements on the control wafers showed the contact barrier height to be $\phi_c = 0.7\,eV$, in agreement with[18]. The control wafers were processed in the same way, except for the phosphorus deposition.

4.3 *Results and discussion*

The measurement of the sample resistance was done using the circuit shown in Fig. 4. Substrate resistance, calculated by eqn (14) was substracted from the measured value, in accordance with (12) (the rear contact resistance being neglected).

The results are shown in Fig. 5. Data for X_{n^+} have been calculated as function of the diffusion time, on the basis of the results of Ref.[16]. The barrier width was computed by the total depletion approximation with $\phi_c = 0.7\,eV$ and $N^+ \simeq 4 \times 10^{20}\,cm^{-3}$[16]. The slight disagreement between the theoretical and "measured" (actually, it was computed as $X_{n^+} = \alpha t_D$[16]) critical N^+ layer depth, evident in Fig. 5, could be explained by nonadequacy of the diffusion model used for such shallow and short (≃ 1 min) diffusions.

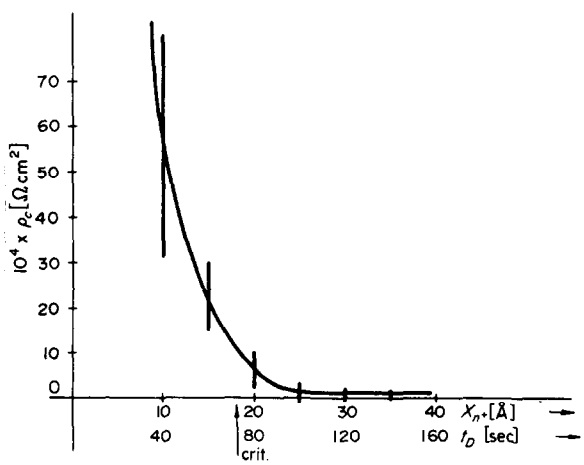

Fig. 5. Experimental results—the specific contact resistivity vs phosphorus deposition time. X_{n^+} is computed as $X_{n^+} = \alpha t_D$[16]. The calculated critical diffusion time (when $x_{n^+} = w_{n^+}$—see Fig. 1c) is 72 sec.

The results are in qualitative agreement with the conclusions concerning contact resistivity dependence on the N^+ layer width. The same holds for the order of magnitude of ρ_c. However, as could be expected from the previous analysis, the absolute value of ρ_c is difficult to measure precisely due to the dominating contribution of the sample body resistance. This is more emphasized here than in the example mentioned before, because the impurity concentration N^+ is now considerably higher. As a result, there are some "negative" values of ρ_c in Fig. 5. This is certainly due to errors in estimating the device parasitic resistances.

The measurement would be much easier to carry out if the samples were of lower impurity concentrations N^+ than those discussed. Unfortunately, such samples with a "square" impurity profile are not easy to fabricate. On the other hand, such effort would not have much practical justification: if one makes surface impurity enriched in order to obtain an ohmic contact, it should be done up to the impurity solubility limit.

5. CONCLUSIONS

A metal N-type semiconductor contact with a thin heavily doped surface region has properties of an ohmic contact if the following conditions are fulfilled:

(a) The impurity concentration N^+ in the surface region is very high (e.g. $N^+ > 5 \times 10^{19}\,cm^{-3}$) or at least much higher than in the bulk of the crystal;

(b) Surface layer width should be equal to or greater than the equilibrium width of the barrier depletion region.

If (b) is satisfied, any further increase of N^+ layer width does not influence the total device resistance, for it is almost completely dependent on the substrate resistance.

The same conclusions also hold for metal P-type semiconductor contacts. But as forming a good ohmic contact on P-type semiconductor usually does not make any problems, this case was not specially treated in the present paper.

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