# Recent Advances of High Voltage AlGaN/GaN Power HFETs

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## ABSTRACT

We review our recent advances of GaN-based high voltage power transistors. These are promising owing to low on-state resistance and high breakdown voltage taking advantages of superior material properties. However, there still remain a couple of technical issues to be solved for the GaN devices to replace the existing Si-based power devices.

The most critical issue is to achieve normally-off operation which is strongly desired for the safety operation, however, it has been very difficult because of the built-in polarization electric field. Our new device called GIT (Gate Injection Transistor) utilizing conductivity modulation successfully achieves the normally-off operation keeping low on-state resistance. The fabricated GIT on a Si substrate exhibits threshold voltage of +1.0V. The obtained on-state resistance and off-state breakdown voltage were 2.6mΩ•cm2 and 800V, respectively.

Remaining technical issue is to further increase the breakdown voltage. So far, the reported highest off-state breakdown voltage of AlGaN/GaN HFETs has been 1900V. Overcoming these issues by a novel device structure, we have demonstrated the world highest breakdown voltages of 10400V using thick poly-crystalline AlN as a passivation film and Via-holes through sapphire which enable very efficient layout of the lateral HFET array avoiding any undesired breakdown of passivation films. Since conventional wet or dry etching cannot be used for chemically stable sapphire, high power pulsed laser is used to form the via-holes.

The presented GaN power devices demonstrate that GaN is advantageous for high voltage power switching applications replacing currently used Si-based power MOSFETs and IGBTs.

**Keywords:** GaN, high voltage, low on-state resistance, normally-off, hole injection, Si, sapphire, via hole, laser drill

## 1. INTRODUCTION

AlGaN/GaN heterojunction field effect transistors (HFETs) are widely investigated for high power switching applications. Most of the reported AlGaN/GaN HFETs are normally-on type taking advantage of the inherent high sheet carrier density caused by the built-in polarization electric field [1-2]. However, such normally-on type HFETs are not applicable to the actual power switching applications in which safety operation is the main concern. Thus, in these applications, Si-based power MOSFETs/IGBTs have been exclusively used so far. Normally-off operation is strongly desired for AlGaN/GaN HFETs while keeping the low on-state resistance. In order to meet such requirements, it is necessary to reduce the two-dimensional electron gas (2DEG) density in the channel. Since the 2DEG is caused by the difference of the polarization-induced fixed charges between GaN and AlGaN, reduction of the Al mole fraction or the thickness of AlGaN effectively reduces those carriers and thereby shifts the threshold voltage toward the positive direction. This approach easily achieves the normally-off operation, however, the resultant drain current would be low since the applicable positive gate voltage is limited by the low barrier height on the AlGaN with high sheet resistance. Thus the reduction of the on-state resistance is limited with this approach [3-6].

So far, the reported breakdown strength of GaN is far larger than that of conventionally used Si so that extremely high breakdown voltages could be achieved in smaller chip size with the lateral device configuration. Field-plates help to increase the breakdown voltage, however, the relatively low breakdown strength in conventional SiN passivation is the bottleneck in this case. Thus, reported off-state breakdown voltage of AlGaN/GaN HFETs maintaining low on-state resistance has been below 1900V [7-11] at highest to the best of our knowledge.

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In this paper, we demonstrate a new operation principle of a GaN-based normally-off transistor with high drain current, which we call a GIT (Gate Injection Transistor). The GIT utilizes hole injection from the p-type gate to the 2DEG region bringing out the conductivity modulation as is observed in IGBTs [12]. This new concept enables both normally-off operation and high current driving capability by applying high positive gate voltage with low gate current.

So far, we demonstrate ultra high breakdown voltages of AlGaN/GaN HFETs using thick poly-crystalline AlN (poly-AlN) passivation combined with field plates. The poly-AlN gives high breakdown strength underneath the field plates together with better heat dissipation suppressing the effect of the surface traps that would cause so-called current collapse [10]. The obtained off-state breakdown voltages increase proportionally by the extension of the gate-drain distance (Lgd) resulting in the highest value of 10400V with the Lgd of 125μm.

## 2. NORMALLY-OFF GAN TRANSISTOR (GIT:GATE-INJECTION-TRANSISTOR)

### 2.1 Operation Principle of GIT

The most notable feature of the GIT is the p-AlGaN gate formed over undoped the AlGaN/GaN hetero-structure as shown in Fig. 1. The p-AlGaN lifts up the potential at the channel, which enables normally-off operation as shown in the band diagram in Fig. 2.

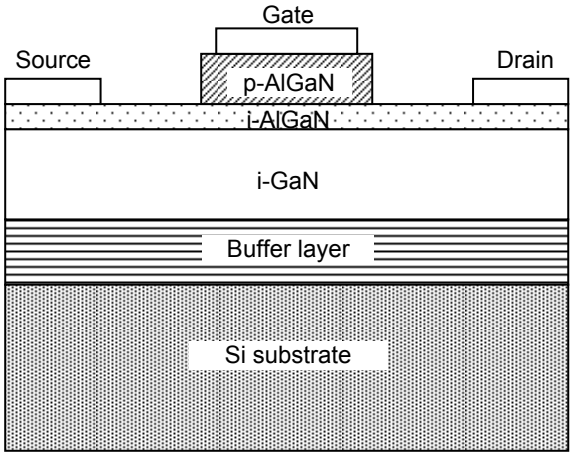


Fig. 1 Schematic illustration of the GIT (Gate Injection Transistor) structure.

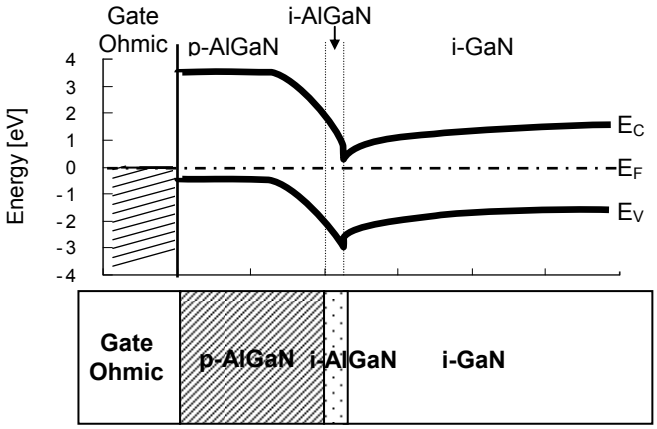


Fig. 2 A calculated band diagram of the GIT under the gate bias of 0V.

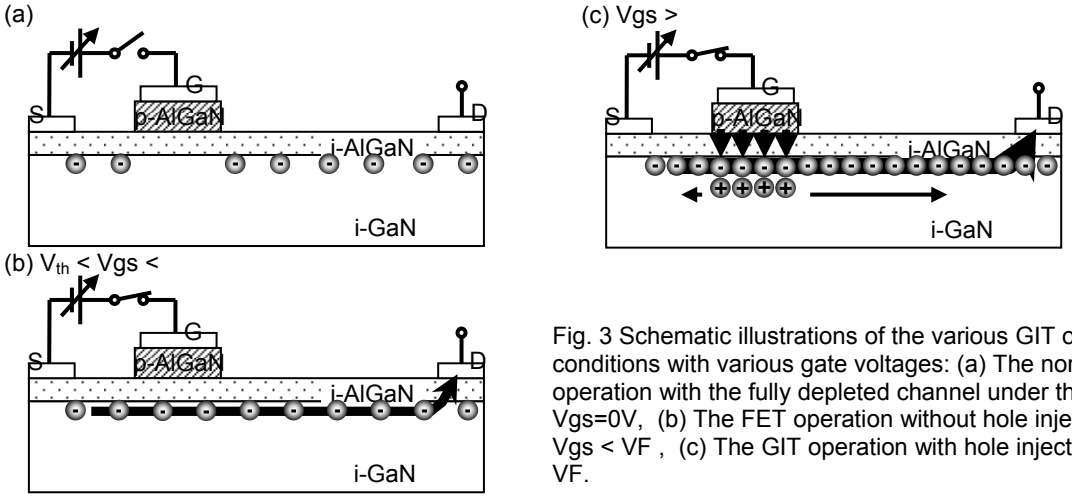


Fig. 3 Schematic illustrations of the various GIT operation conditions with various gate voltages: (a) The normally-off operation with the fully depleted channel under the gate at Vgs=0V, (b) The FET operation without hole injection at Vth < Vgs < VF , (c) The GIT operation with hole injection at Vgs > VF.

Fig. 3 illustrates the basic operation of the GIT. At the gate voltage of 0V, the channel under the gate is fully depleted and the drain current does not flow. At the gate voltages up to the forward built-in voltage Vf of the pn junction, the GIT is operated as a field effect transistor. Further increase of the gate voltage exceeding the Vf results in the hole injection to the channel from the p-AlGaN. Note that the injection of the electrons from the channel to the gate is well suppressed by the hetero-barrier at AlGaN/GaN. The injected holes accumulate the equal numbers of electrons which flow from the source to keep charge neutrality at the channel. The accumulated electrons are moved by the drain bias with high mobility, while the injected holes stay around the gate because the hole mobility is at least two orders of magnitude lower than that of the electron. This conductivity modulation results in a significant increase of the drain current keeping the low gate current.

Fig. 4 shows the distributions of holes and electrons in the GIT obtained by a two-dimensional device simulation at three gate voltages where a drain voltage of 0.1V is applied. With the gate voltage of 0V, the channel under the gate is fully depleted. With the gate voltage of 2V, the drain current flows with the increased sheet charge density in the 2DEG, although the pn-junction gate is not in the on-state and no hole is injected into the i-GaN layer. With the gate voltage of 6V, the holes start being injected into i-GaN generating large numbers of electrons.

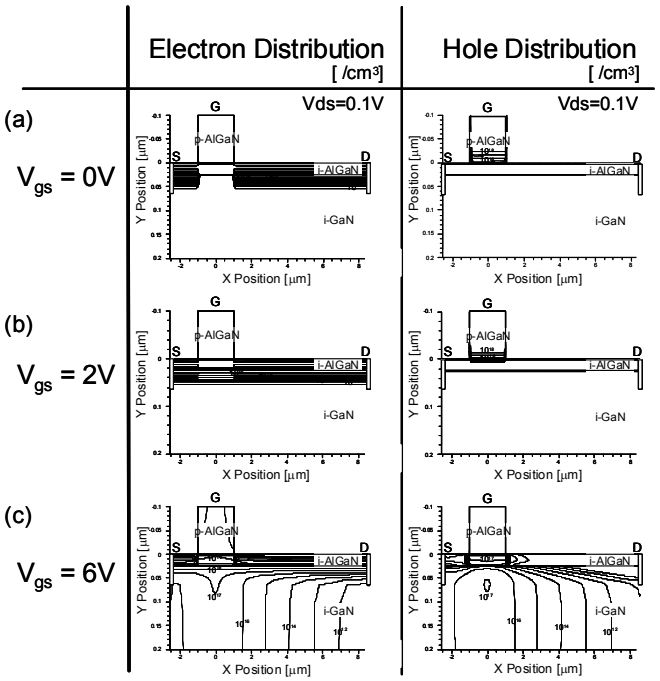


Fig. 4 Contour maps of distributions of holes and electrons in a GIT with various gate voltages calculated by a 2D device simulation: (a) Vgs=0V : normally-off, (b) Vgs=2V : without hole injection, (c) Vgs=6V : with hole injection.

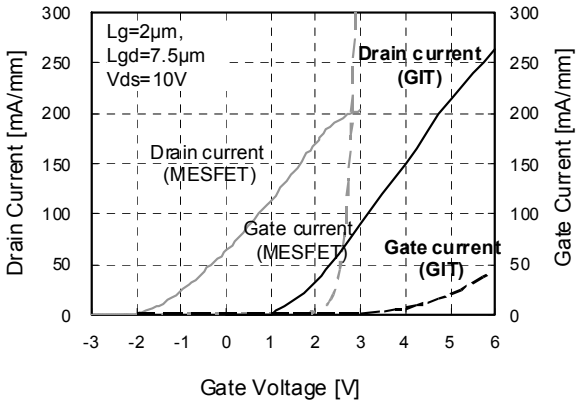


Fig. 5 The calculated drain current and gate current as a function of the gate voltage for both a GIT and for a conventional MESFET.

Fig. 5 shows the simulated drain current and the gate current as a function of the gate voltages for both a GIT and for a conventional Schottky-metal gate HFET (MESFET). The drain current of the conventional MESFET is saturated when the gate current flows with the gate bias over 2V. On the contrary, the drain current of the GIT is dramatically increased by the above mentioned conductivity modulation, even though the gate current starts to flow. The simultaneously accumulated electrons move to the drain with high mobility and relatively low gate current is maintained with the gate voltages up to 6V. The dramatic increase of the drain current with the low gate current enables low on-state resistances keeping the normally-off operation.

### 2.2 Device structure and fabrication of GIT

The process flow of the GIT of which cross section is shown in Fig. 1 is summarized as follows. A p-AlGaN/i-AlGaN/GaN hetero-epitaxial structure for the GIT is grown on a Si substrate with buffer layers consisting of the GaN/AlN multi-layers on top of the AlGaN/AlN initial layers. The both layers effectively relieve the strain in the overgrown GaN caused by the lattice and thermal mismatch between GaN and Si [13]. The total thickness of the nitride epitaxial layer is 4.7 μm. In order to realize the normally-off operation, the Al mole fraction and the thickness of i-AlGaN are optimized to be 15% and 25nm. The p-type gate is formed by the selective etching of the p-AlGaN. The Al mole fraction and the thickness of the p-AlGaN are chosen to be 15% and 100nm. After the formation of device isolation area, the Ti/Al source/drain and Pd gate metals are formed. As a passivation film, 400nm-thick SiN was deposited by PECVD. Au interconnections are made by electroplating.

A cross sectional SEM image of the fabricated GIT is shown in Fig. 6. The gate length defined by the p-AlGaN width is 2.0μm and the distance between the gate and the drain is 7.5μm.

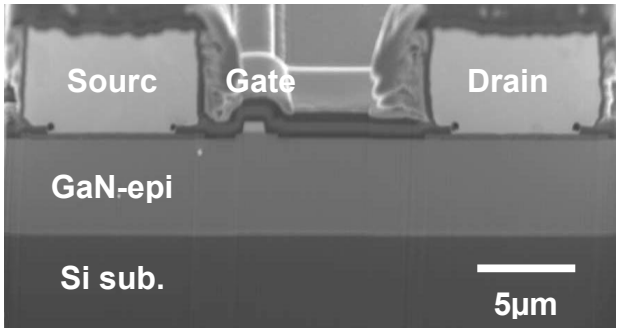


Fig. 6 A cross sectional SEM image of the fabricated GIT on a Si substrate.

### 2.3 Device performances of GIT

Fig. 7 shows on-state and off-state Ids-Vds characteristics of the fabricated GITs. A normally-off operation with the threshold voltage of 1.0V is achieved. The maximum drain current, Imax, is as high as 200mA/mm. The resultant specific on-state resistance is 2.6mΩ•cm2 and the off-state breakdown voltage is 800V. No current-offset is observed at zero drain-bias as shown in Fig. 7 (a), indicating a low level of the gate current under the forward gate voltage. The fabricated GIT has a slightly positive temperature dependence in which the threshold voltage is 1.0V at 25°C and 1.05V at 150°C, respectively. This is due to the increase of the gate resistance at the elevated temperature. Thus, a thermal positive feedback does not occur in the GIT and therefore, the GIT can safely be operated even at higher temperatures.

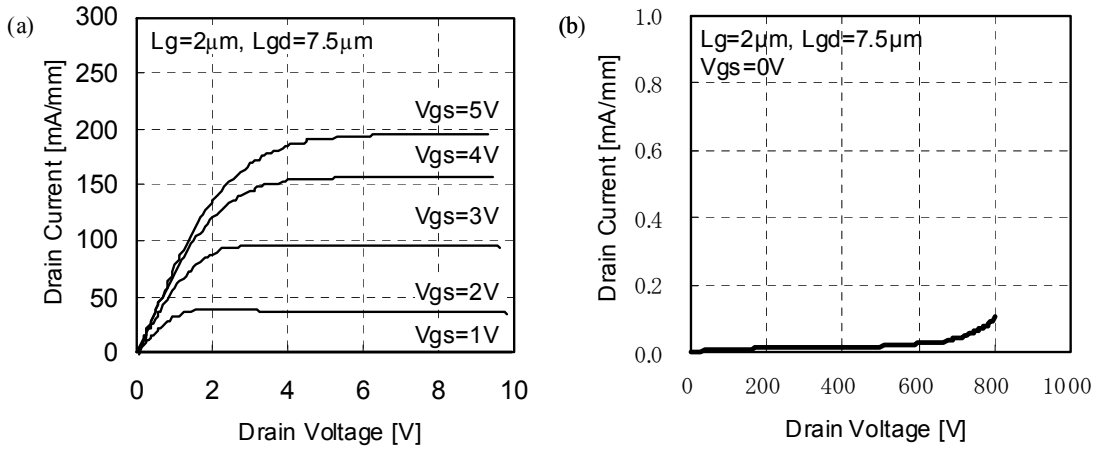


Fig. 7 (a) On-state and (b) Off-state at Vgs=0V Ids-Vds characteristics of the fabricated GIT (Vth=+1.0V, Ron·A=2.6mΩ·cm2, Imax=200mA/mm, Breakdown voltage=800V).

Fig. 8 shows the Ids-Vgs and gm-Vgs characteristics of the fabricated GIT compared with those of the conventional Schottky-gate MESFET. For the GIT, the forward gate voltages up to 6V can be applied while the applicable forward gate voltage is limited below 2V in the conventional MESFET. The GIT exhibited peculiar transconductance characteristics with two peaks as seen in Fig. 8. The device is operated as a FET up to the gate voltage of 3V. Further increase of the gate voltage super-linearly increases the drain current corresponding to the second gm peak. This observed second peak of the gm is the evidence of the hole injection in the GIT. At such high gate voltages, the recombination of the injected holes and electrons in the 2DEG causes light emission as shown in Fig. 9. The electroluminescence at 364nm corresponds to the optical band gap of GaN. The light emission is diminished when the drain bias is given. This indicates that the accumulated electrons move to the drain so that the recombination is suppressed.

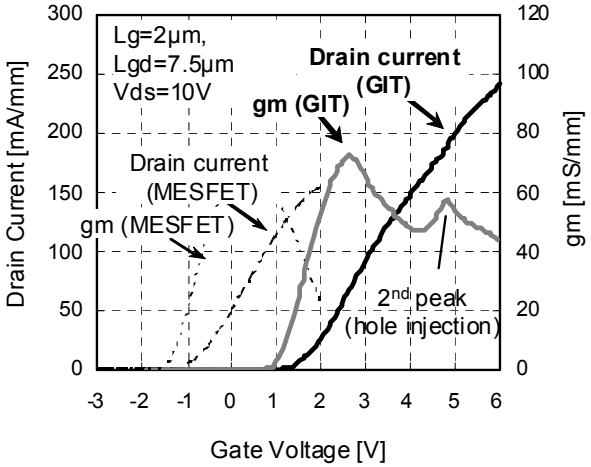


Fig. 8 Ids-Vgs and gm-Vgs characteristics of the fabricated (a) GIT and (b) a MESFET. GIT exhibited peculiar transconductance characteristics with two peaks.

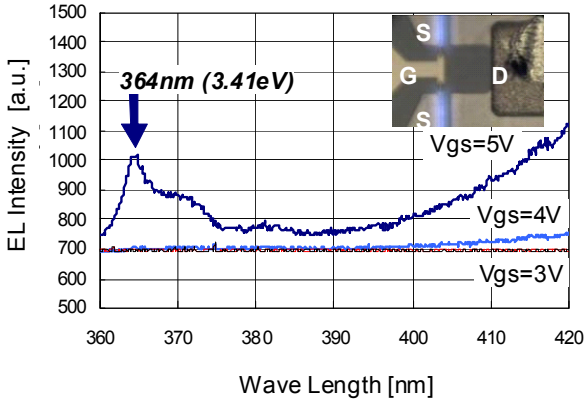


Fig. 9 An electroluminescence spectrum obtained from the fabricated GIT with different gate voltages.

Typical Gummel plots of the GIT and the MESFET, the drain and gate currents as functions of the gate voltages, are shown in Fig. 10 (a). The drain current of the GIT increases owing to the hole injection at higher gate voltages, where the gate current increases. Such increase of the drain current is not observed with the MESFET. The ratio of ΔId and Δ Ig, the current gain hFE is plotted as a function of the gate voltages in Fig. 10 (b). At higher gate voltages, the hFE of the GIT stays from 100 to 1000. This experimentally obtained hFEs well agree with the mobility ratio of the electrons to the holes, which supports the operation principle of the GIT.

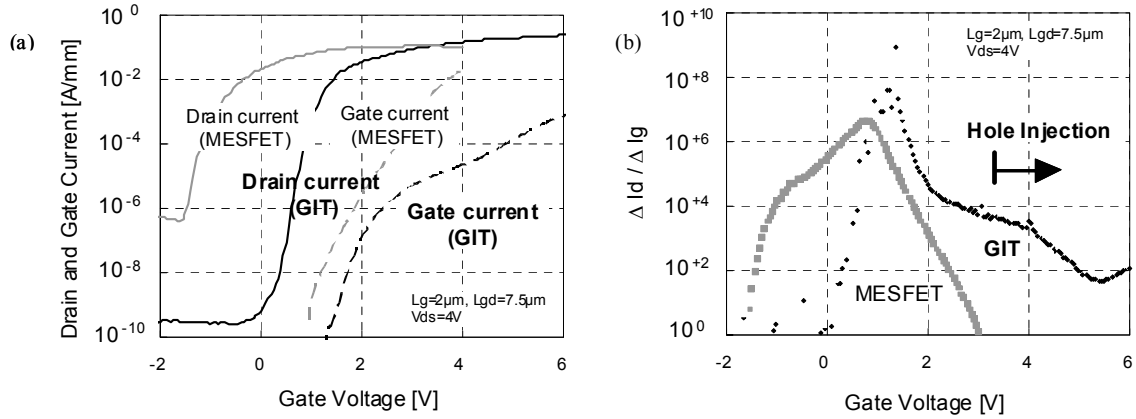


Fig. 10 Comparison of the obtained characteristics of the GIT and the MESFET : (a) Gummel plots and (b) Ratio of DId and D Ig (the current gain, hFE).

Fig. 11 summarizes the switching characteristics of the fabricated GIT. The definition of the switching parameters are summarized in inserted figure in Fig. 11. The given drain bias and driving current are 100V and 10A, respectively, using 10 Ω load resistance. The rise time, the fall time, the on-delay time and the off-delay time of the drain current are measured by varying the gate voltages as shown in Fig. 11. The measured rise times and the on-delay times are on the order of 10 ns, which are shorter than those of the conventional Si-based MOSFETs and IGBTs. The fall time and the off-delay times are slightly longer due to the slow recombination of the injected holes even though the values are still smaller than those of Si-based MOSFETs and IGBTs.

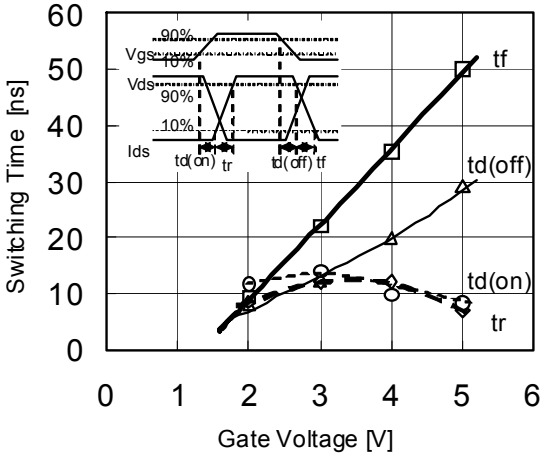


Fig. 11 Switching characteristics of the fabricated GIT (the definition of the switching parameters inserted)

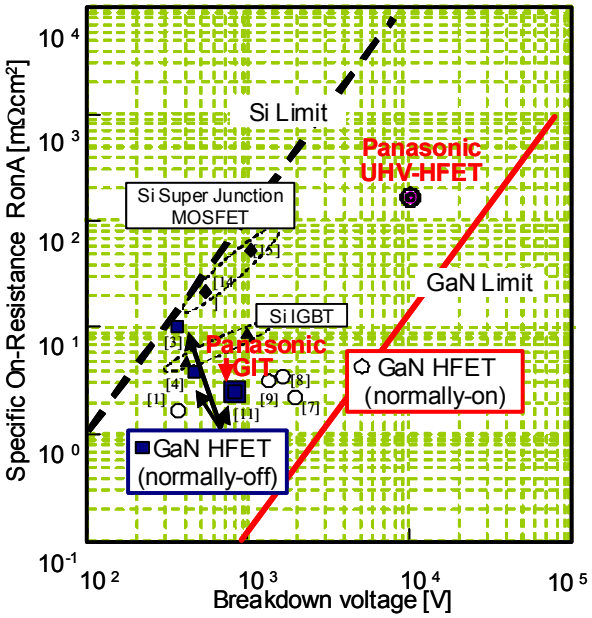


Fig. 12 State-of-the-art Ron·A and breakdown voltage of normally-off GaN-based devices compared with those of Si-based devices.

Fig. 12 summarizes the state-of-the-art performances of the normally-off GaN-based power transistors as compared with those of conventional Si-based power transistors [1, 3-4, 7-9, 11, 14-15]. The Ron•A and breakdown voltage of the GIT are the best values among the GaN-based normally-off transistors to the best of our knowledge. Note that they are as comparably good as those of SiC devices. The GIT on a Si substrate can provide the following advantages in addition to the low cost fabrication. The use of a conductive substrate enables Source-Via Grounding (SVG) structure [1]. By the SVG, the source can be ohmic-contacted to the conductive Si substrate through the surface via-hole. The SVG plays three important roles. Firstly, it reduces the source interconnection resistance, which makes the specific on-state resistance in a large area device much lower. Secondly, the source parasitic inductance is also significantly reduced because of the eliminated source wires and bonding. Thirdly, the SVG structure relieves the electric field between the drain and the gate since the grounded substrate acts as a backside field plate.

## 3. ULTRA HIGH BREAKDOWN VOLTAGE GAN TRANSISTOR

### 3.1 Device structure and fabrication

Fig. 13 shows the schematic cross section of the fabricated AlGaN/GaN HFET with poly-AlN passivation and field plates. The thick poly-AlN passivation film of 1μm is deposited by DC-sputtering technique which has 200 times higher thermal conductivity than that of conventional SiN. The obtained breakdown electric field strength of sputtered poly-AlN film is as high as 6MV/cm which is almost 2 times higher than conventional. PE-CVD SiN film. A closely-packed layout is used as shown in Fig. 14, in which the electrodes are placed in a concentric manner with via-holes through sapphire at the drain electrodes.

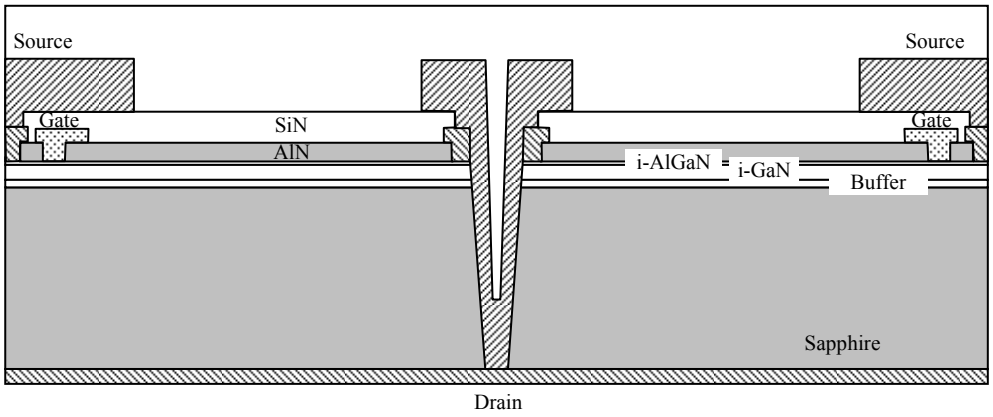


Fig. 13 A schematic cross-section of the fabricated ultra high voltage HFETs with AlN passivation and via-holes through the sapphire substrate.

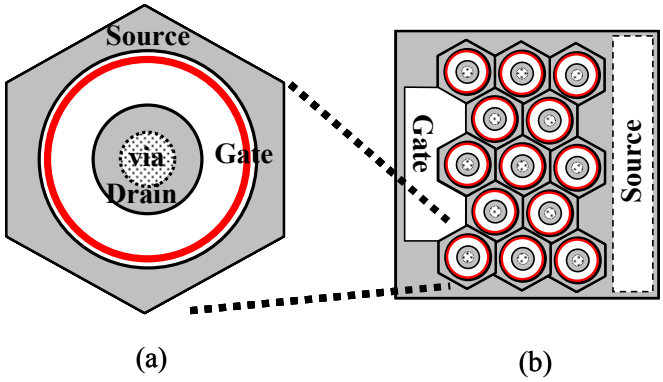


Fig. 14 A schematic top view of (a) a unit cell and (b) an arrayed chip of ultra high voltage HFETs with hexagonal closely packed layout with via-holes at drains.

Fig. 15 shows the calculated thermal distribution of AlGaN/GaN HFETs on sapphire substrate with and without via-holes under the condition of uniform power generation of 8W/mm in the channel. Integration of the via-holes reduces the maximum channel temperature down to 150C, while that without the via-holes is as high as 225C. The metal filling the via-holes greatly helps to reduce the temperature.

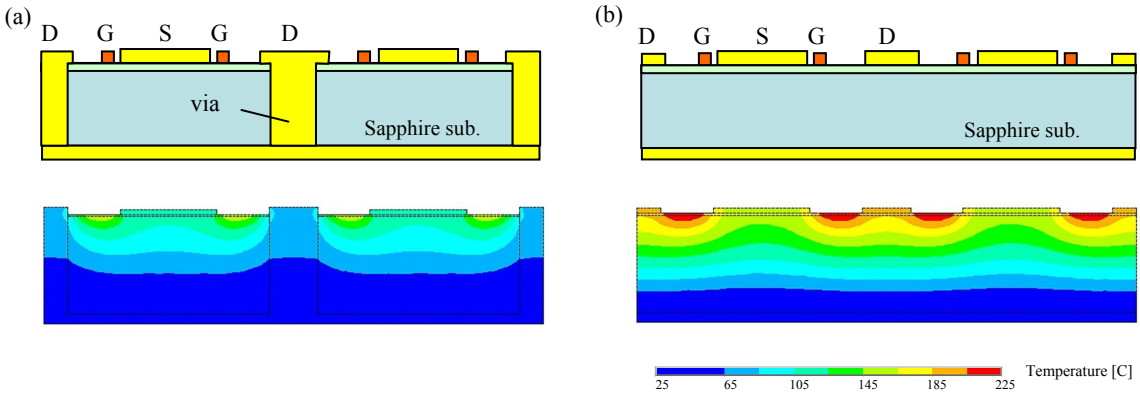


Fig. 15 Calculated thermal distribution of AlGaN/GaN HFETs on sapphire substrate (a) with and (b) without via-holes under the condition of uniform power generation of 8W/mm in the channel.

Since conventional wet or dry etching technique cannot be used for forming via-holes through chemically stable sapphire, high power pulsed laser is used to form the via-holes through a sapphire substrate. Thick gold plating, wafer thinning and backside metallization follow the laser drilling of sapphire. The above process successfully forms via-holes through a sapphire substrate with the depth of 100μm as shown in Fig. 16.

The optical microscopic image and cross sectional SEM image of the fabricated HFET are shown in Fig. 17 and Fig. 18, respectively.

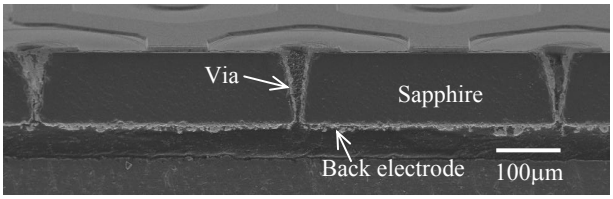


Fig. 16 Cross sectional SEM image of fabricated via-holes through sapphire.

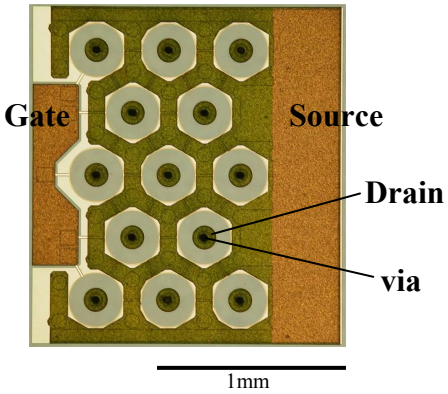


Fig. 17 Microphotograph of the fabricated ultra high voltage HFET array.

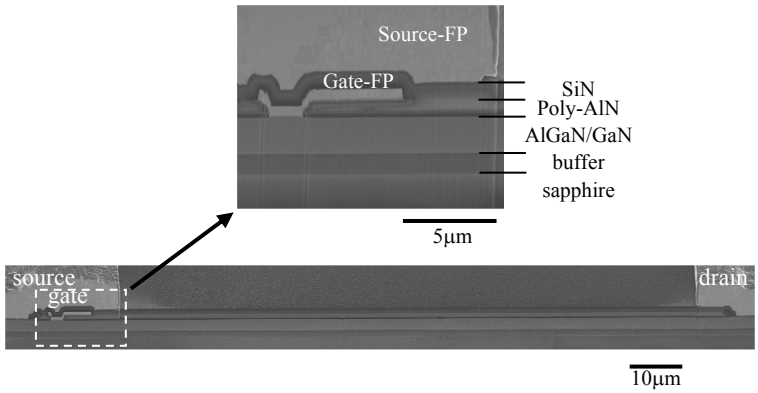


Fig. 18 Cross sectional SEM image of the fabricated ultra high voltage HFET using poly-AlN passivation and field plates.

### 3.2 Device Performances

We systematically investigate the device characteristics of the fabricated AlGaN/GaN HFETs in which the gate-drain spacing distances (Lgd) are varied up to 125μm.

Fig. 19 shows the resultant off-state breakdown voltages (BVds) as a function of the Lgd for various passivations. With AlN passivation, the BVds proportionally increases as Lgd increases, while the BVds saturates at 3000V with SiN passivation. The obtained 10400V with Lgd of 125μm is the highest value ever reported for GaN-based transistors, which shows, in addition, a strong sign of further increase with the extension of Lgd over 125μm.

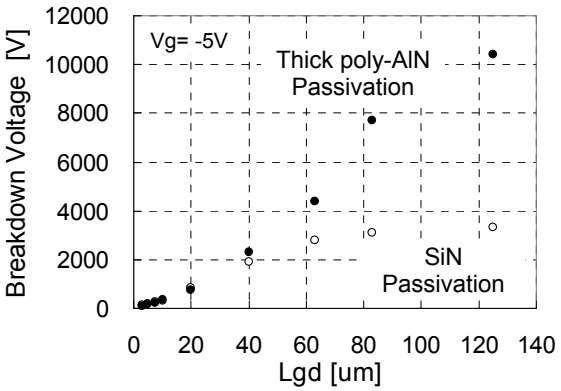


Fig. 19 The off-state breakdown voltages (BVds) of fabricated HFETs for various Lgd. BVds of 10400V at Lgd=125um is obtained with AlN passivation.

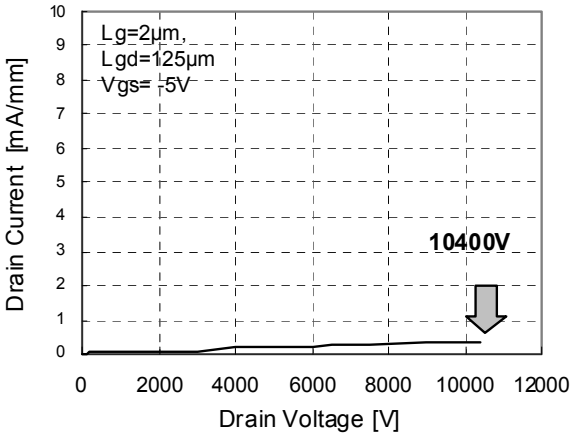


Fig. 20 Off-state Ids-Vds characteristics of the fabricated HFET (Breakdown voltage=10400V).

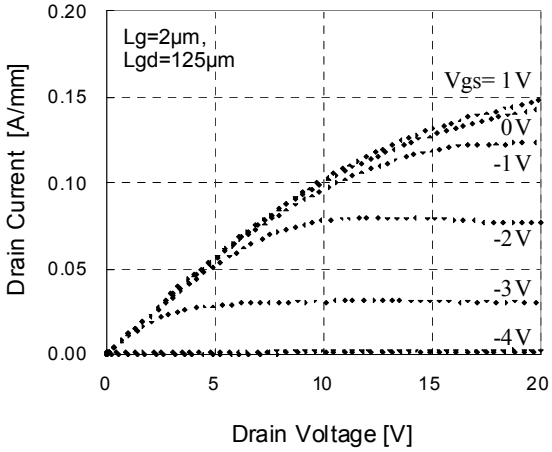


Fig. 21 On-state Ids-Vds characteristics of the fabricated HFET. (Ron·A=186mΩ·cm2, Imax=150mA/mm)

Fig. 20 and Fig. 21 summarize the DC characteristics of the fabricated ultra high voltage AlGaN/GaN HFET with Lgd of 125μm. The off-state breakdown voltage is greatly improved by the AlN passivation with field plates. The specific on-state resistance Ron•A is 186mΩ•cm2 with the Imax of 150mA/mm.

The result is plotted in Fig. 12 comparing the state-of-the-art values including those of conventional Si-based transistors [7-11]. The presented device demonstrates that GaN is also advantageous in the ultra high voltage ranges.

## 4. CONCLUSIONS

We have successfully developed a new normally-off AlGaN/GaN transistor with the high drain current. The transistor called a GIT utilizes hole-injection from the p-AlGaN formed over the i-AlGaN/GaN resulting in a dramatic increase of the drain current at high gate voltages owing to the conductivity modulation. The resultant Ron•A and the breakdown voltage are 2.6mΩ•cm2 and 800V, respectively. The GIT achieves a high drain current of 200mA/mm with the threshold

voltage of 1.0V. It is noted that using Si substrates makes the GIT more cost effective than ordinary GaN-based HFETs fabricated on sapphires or on SiCs. The presented GIT on Si is much advantageous for power switching applications especially in the middle voltage range below 1000V.

So far, we have successfully demonstrated 10400V of BVds in AlGaN/GaN HFETs with thick poly-AlN passivation. The thick poly-AlN passivation with field plates and via-holes through sapphire substrate enable high breakdown voltages. The presented ultra high voltage transistors would be applicable to practical high power switching systems far beyond 1000V.

## 5. ACKNOWLEDGEMENT

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