Journal of The Electrochemical Society, **153** (7) G644-G649 (2006)
0013-4651/2006/153(7)/G644/6/$20.00 © The Electrochemical Society

Galvanic Corrosion during Processing of Polysilicon Microelectromechanical Systems

The Effect of Au Metallization

M. Huh, Y. Yu, H. Kahn,[z] J. H. Payer,[*] and A. H. Heuer

Department of Materials Science and Engineering, Case Western Reserve University, Cleveland, Ohio 44106-7204, USA

Immersion in aqueous hydrofluoric acid (HF), a standard processing step in fabricating microelectromechanical systems devices, causes rougher and weaker polycrystalline silicon (polysilicon) films in the presence of Au metallization and leads to relatively thick surface oxides. The origin of these effects is the galvanic corrosion that takes place due to the difference in electrochemical potential between the noble Au metallization and the polysilicon in HF solution, resulting in the accelerated formation of a porous surface layer due to corrosion of the silicon. The electrochemical behavior and the evolving microstructural morphology are correlated. In HF solution, Si is dissolved and porous silicon (PS) is formed. The PS first develops along the polysilicon grain boundaries and then extends into the grain interiors. After rinsing in water and exposure to air, the pore walls form the usual oxide, leading to a Si/SiO_2 composite with a gradient in composition—from a high fraction of SiO_2 near the surface to 100% Si deeper into the polysilicon. Inasmuch as the galvanic corrosion requires positively charged holes, these effects can be minimized by using n-type dopants in the polysilicon and performing the HF immersion in the absence of illumination.
© 2006 The Electrochemical Society. [DOI: 10.1149/1.2199139] All rights reserved.

Manuscript submitted November 8, 2005; revised manuscript received December 1, 2005. Available electronically May 12, 2006.

In typical microelectromechanical systems (MEMS) devices, the structural material is polysilicon and the release layer beneath the structural material that must be dissolved to enable the devices to move freely is usually SiO_2. Therefore, one of the last processing steps before packaging, termed "release," is to immerse the entire substrate in HF solution, which efficiently dissolves the SiO_2. Typically the release step takes several minutes. A 49% HF solution is usually used because that is the highest concentration commercially available, and the etching rate of SiO_2 in HF solution is roughly proportional to the HF concentration.[1]

It is common to deposit Au, or another noble metal, onto the contact pads of MEMS devices for making electrical contact. However, several adverse phenomena have been reported for doped polysilicon MEMS devices using Au contacts following HF release. These include increased polysilicon roughness,[2,3] increased polysilicon resistivity,[4] decreased polysilicon device resonant frequency,[4] and relatively thick ($\sim$30 nm) surface oxides.[5] It has been suggested that these phenomena involve galvanic corrosion which occurs due to the presence of Au in electrical contact with the polysilicon.[4,6,7] Au is the more noble member of the galvanic couple in HF solution, and the more active polysilicon is anodically polarized with a resulting increase in corrosion.

The mechanism for the observed degradation is similar to that of porous silicon (PS) formation utilizing external voltages.[8,9] Actually, PS formation has been achieved in the absence of external voltages, i.e., by galvanic corrosion, using the noble metals Au and Pt deposited onto the silicon.[10]

Figure 1a shows a typical anodic current–voltage (i–v) curve for silicon in HF. Under cathodic polarization, silicon is stable and does not dissolve. In the low-potential anodic regime, the current increases exponentially with increasing potential. This region represents PS formation, with a wide variety of pore morphologies observed for varying parameters, including applied potential, HF concentration, Si orientation, Si conductivity, and Si geometry.[8,9] In this region, Si dissolves directly to form SiF_4 in an electrochemical reaction that requires two holes.[9]

As the anodic potential increases further, the slope of the i—v curve passes through a maximum and then the current itself reaches a maximum. These two occurrences bound a transition region. At higher potentials, above the maximum current, the electropolishing region is entered. Here the Si dissolves by first forming a surface SiO_2 layer by reacting with H_2O, the SiO_2 being subsequently dissolved in the HF.[9] In the electropolishing regime, the surface maintains a relatively smooth morphology.[8] Figure 1b shows the different regions in relation to the corrosion current density and HF concentration. The behavior is not affected by the nature of the Si doping.

While the detrimental phenomena observed after MEMS release have been convincingly correlated with undesired electrochemical effects between Au and polysilicon,[4,6,7] the microstructural development of the PS in polysilicon and the thick oxide growth in this system have not been determined. In general, PS formation in polysilicon has hardly been investigated, in contrast to PS development in single-crystal Si. In fact, PS has been incorporated into the designs of several MEMS devices due to its unique structural and etching properties.[11-13] This report describes the development of the PS structure and the subsequent formation of relatively thick oxide in phosphorus-doped polysilicon (phosphorous–polysilicon) due to galvanic corrosion when electrical contact involves Au metallization on devices released in 49% HF. We also briefly discuss strategies for avoiding unwanted electrochemical effects during processing of MEMS devices.

Experimental

Phosphorus–polysilicon samples were fabricated, as follows: Si(100) substrates were thermally oxidized to form a 100 nm SiO_2 layer. Then, a 2 μm thick undoped polysilicon layer was deposited via low-pressure chemical vapor deposition (LPCVD) at 580°C, using SiH_4 at 100 sccm and 300 mTorr in a 225 mm diam furnace. Under these conditions, a fine-grained equiaxed polysilicon microstructure results.[14] To achieve phosphorus doping via solid-state diffusion, a 2 μm thick phosphosilicate glass (PSG) layer was deposited via LPCVD at 450°C using SiH_4, O_2, and PH_3. The wafers were then annealed at 1100°C for 1 h in nitrogen to allow phosphorus diffusion into the polysilicon to a doping level of $\sim 10^{18}$–10^{19} cm^{-3}. The PSG was removed in buffered oxide etchant (a solution of HF and NH_4F), and the wafers were removed from the etchant as soon as the PSG was cleared to minimize any effects to the polysilicon. The Si wafers were then cut into small rectangular pieces. The exposed area of each phosphorus–polysilicon sample was 1.8 cm^2. On some of the pieces, a $\sim$30 nm thick Au film was sputter-deposited onto one side, covering approximately half the area. Even with no sputtered Au, the phosphorus-polysilicon samples were sufficiently conductive to allow direct electrical connections.

All of the electrochemical experiments were performed at room temperature under fluorescent light, except as noted otherwise. An-

* Electrochemical Society Active Member.
[z] E-mail: harold.kahn@case.edu

Downloaded 03 Mar 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

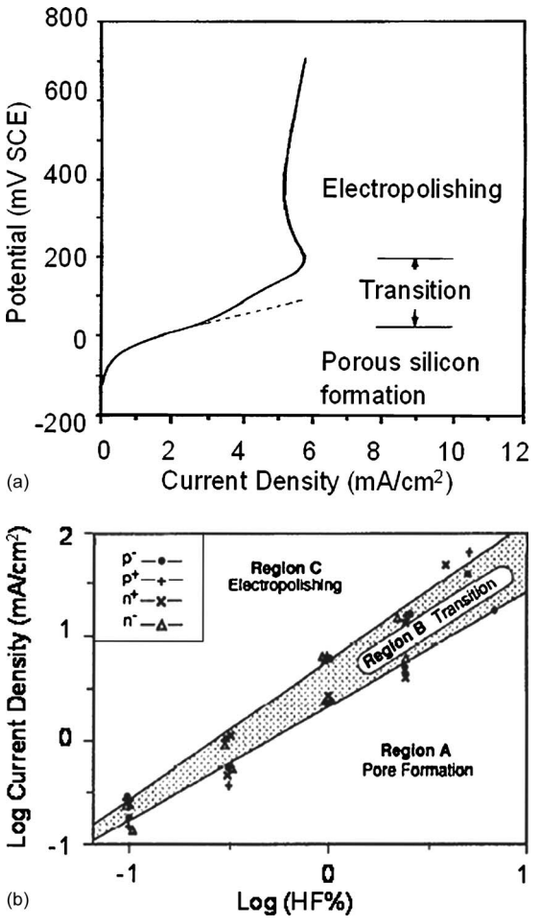

Figure 1. (a) Typical anodic i–V curve measured on moderately doped p-type single-crystal Si in 1% HF solution;[9] (b) log current density vs log (HF%) for variously doped Si, showing the regions of PS formation and electropolishing.[8]

odic polarization measurements were performed in 49% HF, using a Solartron Instrument SI 1280B potentiostat, Pt as the counter electrode, and a saturated calomel electrode (SCE) as the reference electrode. The potentiodynamic tests used a fixed scan rate of 1 mV/s, with fresh HF solution being used for each experiment.

Galvanic testing was performed using a gold strip as the cathode and a phosphorus–polysilicon anode. The net current flow between the anode and the cathode was measured, the potential again being measured with respect to a SCE reference electrode. The exposed surface areas of the gold and silicon electrodes in HF solution were approximately equal, and the distance between two electrodes was 10 mm. Samples were rinsed with deionized (DI) water after each experiment, unless otherwise indicated.

After electrochemical testing, the phosphorus–polysilicon samples were examined by a variety of techniques, including cross-sectional scanning electron microscopy (SEM), cross-sectional transmission electron microscopy (TEM), X-ray energy-dispersive spectroscopy (XEDS), nanoindentation, and X-ray photoelectron spectroscopy (XPS).

Results and Discussion

Electrochemical measurements.— The i–v polarization curves obtained from a bare phosphorus–polysilicon sample and a partially Au-coated sample in 49% HF are shown in Fig. 2. Both curves have the same general shape as that seen in Fig. 1a, which is for a single-crystal Si sample in HF solution. More specifically, both

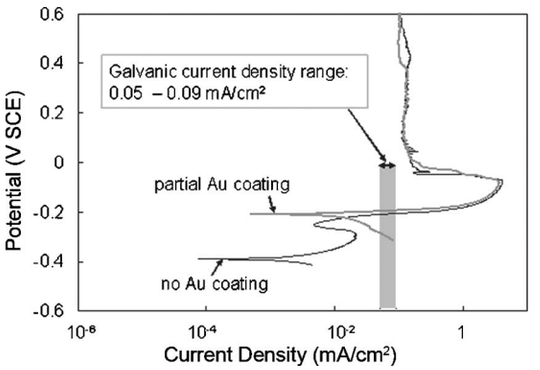

Figure 2. i–V polarization curves for phosphorus–polysilicon samples in 49% HF, with and without partial Au coating. The shaded area corresponds to the current density range 0.05–0.09 mA/cm^2 (see Fig. 3).

phosphorus–polysilicon curves in Fig. 2 show a low-potential region of exponentially increasing current before reaching a peak current, conditions known to lead to PS formation. Figure 2 also shows that the partially Au-coated sample has an open-circuit potential (OCP) ~0.2 V higher than that of the bare sample. The OCP of Au by itself in 49% HF was 0.65 V_{SCE}, while that of phosphorus–polysilicon was −0.4 V_{SCE}. Thus, Au metallization will readily place a phosphorus–polysilicon sample in an anodic potential condition.

This was confirmed by setting up a galvanic cell between Au and phosphorus–polysilicon. This experimental environment is electrochemically identical to polysilicon MEMS devices containing Au metallization. The galvanic current as a function of time is shown in Fig. 3 for several phosphorus–polysilicon samples tested in 49% HF for a range of times, and for one phosphorus–polysilicon sample tested in 25% HF. In all cases, the galvanic action resulted in anodic polarization of the phosphorous–polysilicon. In 49% HF, the galvanic current density varied from 0.05 to 0.09 mA/cm^2 and remained constant with time. As seen in Fig. 2, this current density range lies precisely within the exponentially increasing portion of the i–V curve that represents PS formation. In addition, while these galvanic cell conditions lie off the right edge of the graph in Fig. 1b (log 49% HF = 1.7 and log 0.09 mA/cm^2 = −1), if the graph were extended, these conditions would clearly be positioned well within the pore-forming region. We conclude that the Au/phosphorus–polysilicon galvanic cell current represents Si dissolution leading to PS formation.

Microstructural investigations.— Cross-sectional SEM images were taken from several of the phosphorus–polysilicon samples

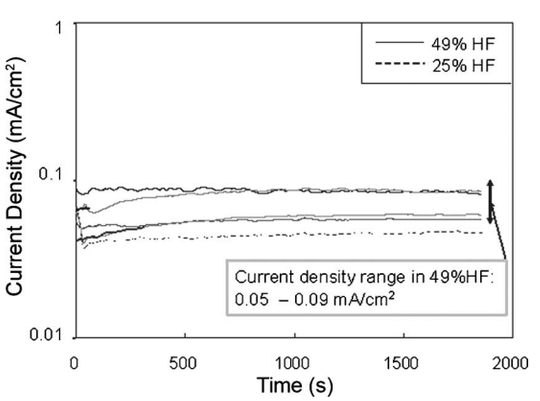

Figure 3. Galvanic current density measurements of phosphorus–polysilicon in HF. The solid lines represent tests in 49% HF, and the dashed line a single test in 25% HF.

Downloaded 03 Mar 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

Table I. Galvanic cell test conditions for four phosphorus–polysilicon samples whose test results are shown in Fig. 3. (Current density has been converted to current.)

Sample	HF (%)	Current, i (mA)	Time, t (s)	Charge, q(mC)= i(mA) × t(s)	Apparent surface layer thickness (μm)
A	49	~0.14	1800	~260	~1.0
B	25	~0.07	1800	~130	~0.6
C	49	~0.09	300	~27	~0.2
D	49	~0.13	60	~8	~0

whose galvanic currents are shown in Fig. 3. The galvanic cell test conditions for these samples are listed in Table I. The samples were cleaved and viewed in the SEM at an angle nearly perpendicular to the cleaved surface, as shown in Fig. 4. The phosphorus–polysilicon cross-sectional sample in Fig. 4a reveals two different morphologies. The ~1 μm thick region near the surface appears much rougher than the bottom ~1 μm region. A "surface layer" of increased roughness can also be seen in Fig. 4b and c but with decreasing thickness. The surface layer thicknesses, included in Table I, scale with the total charge, q, that flowed during the galvanic corrosion of each sample. As discussed above and confirmed with TEM below, the surface layer detected by cross-sectional SEM is the

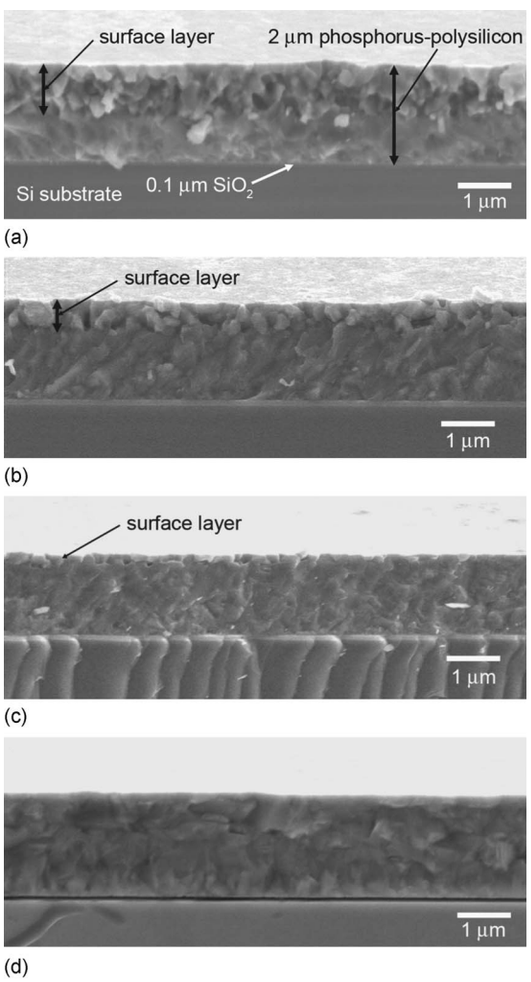

Figure 4. Cross-sectional SEM images of phosphorus–polysilicon samples after galvanic corrosion. (a–d) Samples A–D, respectively. Testing conditions are listed in Table I.

portion of the phosphorus–polysilicon that has developed very fine scale porosity due to the galvanic action during the exposure to HF solution.

The surface layer of the sample shown in Fig. 4a was investigated using cross-sectional energy-filtering (EF) TEM, and the images are shown in Fig. 5. The elemental maps obtained using EFTEM show increased brightness in those areas that contain greater amounts of the specific element of interest. Thus, the silicon and oxygen maps shown in Fig. 5b and c reveal that the top ~1 μm of the phosphorus–polysilicon is richer in oxygen than the bottom ~1 μm, which is relatively richer in Si. This thickness agrees well with the surface layer thickness seen in the cross-sectional SEM image (Fig. 4a). Porosity cannot be seen in this image, suggesting that the pores that developed due to the galvanic action are filled with SiO_2. (Even in high-resolution TEM, pores were not observed.) That is, the pore walls formed the conventional surface oxide, and since the volume of SiO_2 is ~2.25 times greater than the volume of the Si it replaces, the pores were completely replaced with SiO_2.

The bottom region of the phosphorus–polysilicon film is shown in Fig. 5d and e. In this portion of the film, the phosphorus–polysilicon nearest the surface was removed during TEM sample preparation. As indicated in the elemental maps, the oxide in this region forms a weblike structure which appears to follow grain boundaries. This morphology agrees with previous work which showed that electrochemical etching of polysilicon resulted in pore formation along grain boundaries.[15] From the TEM images in Fig. 5, we conclude that during galvanic corrosion, PS initially forms along the grain boundaries and then grows into the grain interiors. Therefore, the regions near the surface have been completely transformed to PS, while toward the bottom of the phosphorus–polysilicon, the only evidence of (prior) PS is at grain boundaries.

In the oxygen maps (Fig. 5c and e), the oxygen-rich regions are not as bright as the SiO_2 layer beneath the phosphorus–polysilicon, implying that the concentration of oxygen is not as high as in stoichiometric SiO_2. An XEDS linescan depth profile of the phosphorus–polysilicon cross section was performed in the TEM, as shown in Fig. 6. The oxygen content decreases from approximately 24 atom % at the surface to near zero at ~1.1 μm below the surface. Clearly, due to the galvanic action, the surface layer of the phosphorus–polysilicon is a mixture of Si and SiO_2. The SiO_2 volume fraction is greatest at the surface and decreases to zero toward the bottom of the film. This agrees with a scenario of porosity developing in the phosphorus–polysilicon, beginning at the top surface, with the pores being subsequently filled with SiO_2.

Nanoindentation was performed to compare the Young's modulus and hardness of the phosphorus–polysilicon sample before and after a 1800 s galvanic experiment in 49% HF. A Berkovitch tip and a 4 mN load were used. Three indents were made on each sample, and the maximum indentation depths did not exceed 82 nm in the sample before the galvanic experiment or 116 nm in the sample after the galvanic experiment. After galvanic testing, Young's modulus decreased from 183 to 105 GPa, and hardness decreased from 9.6 to 6.1 GPa. These values are consistent with a polysilicon sample partially transforming to a mixture of polysilicon and SiO_2.

Using the total charge, q, transferred during the galvanic corro-

Downloaded 03 Mar 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

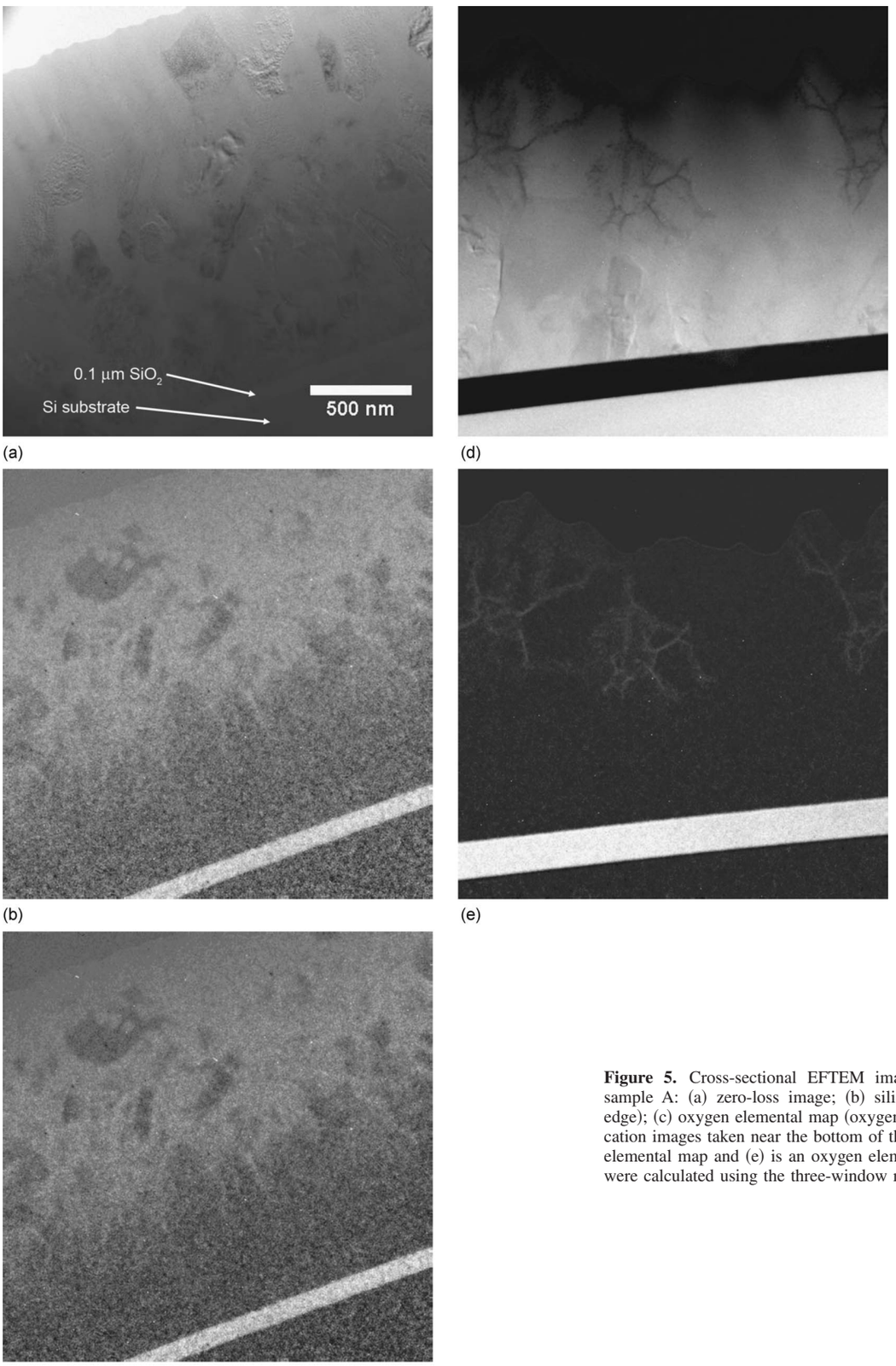

Figure 5. Cross-sectional EFTEM images of phosphorus–polysilicon sample A: (a) zero-loss image; (b) silicon elemental map (silicon-L_{23} edge); (c) oxygen elemental map (oxygen-*K* edge); (d, e) higher magnification images taken near the bottom of the sample, where (d) is a silicon elemental map and (e) is an oxygen elemental map. The elemental maps were calculated using the three-window method.[18]

sion of the sample shown in Fig. 4a and 5 (~260 mC, Table I), the amount of silicon dissolved was determined. The layer thickness based on this estimate was compared to the direct measurements of PS surface layer thickness. Assuming a 1 μm thick layer, the coulometric calculation predicts that 9% of the Si atoms were dissolved. Oxidizing the pore walls to completely fill the pores with SiO_2 results in an oxygen atomic fraction of 14%. This calculation is in good agreement with the TEM XEDS results (Fig. 6).

Downloaded 03 Mar 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

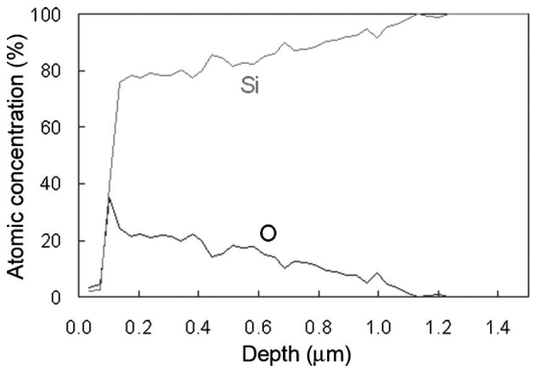

Figure 6. XEDS linescan results for the phosphorus–polysilicon cross section seen in Fig. 5.

Oxide growth.— The discussion in the Introduction indicates that there should be no SiO_2 formed in the HF solution during galvanic corrosion. Therefore, it is interesting to investigate when exactly the SiO_2 appears during the MEMS processing. Figure 7 shows XPS depth profiles for two phosphorus–polysilicon samples galvanically tested in 49% HF for 1800 s. The sample that was not rinsed in DI water was measured ~7 h after the galvanic test and had a small oxygen content, ~3%. The sample that was rinsed in DI water showed an initial oxygen concentration of ~35% that decreased to ~10% at a thickness of 5 nm. The rinsed sample was also analyzed 24 and 44 days after galvanic testing. The surface oxygen content remained at ~35%, and the near-surface oxygen content continued to increase, from ~10 to ~ 17 to ~ 21%.

The sample that was not rinsed showed minimal oxide formation during the 7 h it was exposed to air, presumably because H-termination passivated all the polysilicon surfaces.[9] (Oxide formation on H-terminated silicon typically requires several days to form in air,[16] depending on the ambient conditions.) This confirms the supposition that no SiO_2 formed during galvanic corrosion. The sample that was rinsed in DI water lost its H-termination and immediately developed some SiO_2, either in the DI water or upon exposure to laboratory air. In nonporous Si, this "native" oxide passivates the surface and oxidation stops after reaching a thickness of ~2 nm.[17] However, in the samples being studied here, oxide growth continued for at least 44 days, with the SiO_2-rich layer extending to a depth of over 1 μm into the film (Fig. 6). Presumably, the porous structure provided paths for oxygen diffusion over considerable distances and for long times, and the large exposed surface area promoted formation of a significant volume of SiO_2.

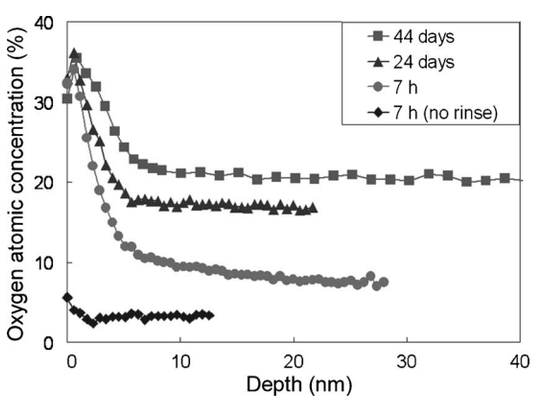

Figure 7. XPS oxygen concentration depth profiles of phosphorus–polysilicon.

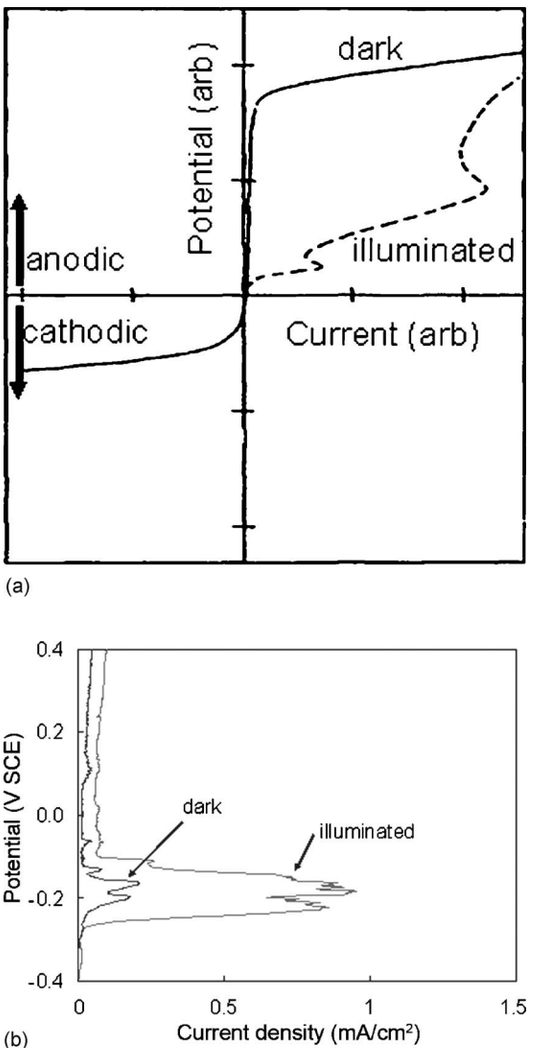

Figure 8. (a) Typical i–V curve for n-type Si in HF.[8] (b) i–V polarization curves for phosphorus–polysilicon, illuminated and in the dark.

Implications for MEMS processing.— Because of the reduced Young's modulus, reduced hardness, reduced strength, and increased surface roughness that result from galvanic corrosion of polysilicon, these effects should be avoided in MEMS processing. Galvanic corrosion can be reduced by decreasing the galvanic potential or decreasing the corrosion kinetics. The potential would be decreased if the contact metallization had a lower OCP, closer to polysilicon. Unfortunately, the two noble metals that are relatively immune to HF and could replace Au—Pd and Pt—have similar OCPs in HF solution. The well-known area effect for galvanic corrosion could be applied where feasible during the design stage. It is desirable to minimize the anode–cathode area exposed to the HF solution, i.e., Au–PS area. A lower area ratio decreases the level of detrimental anodic polarization of the PS.

Figure 3 shows that the galvanic current is modestly reduced when using 25% HF compared to 49% HF. However, because the rate of SiO_2 etching that is necessary for MEMS release will also be reduced, the release time would have to be increased, probably negating any advantage of the reduced current. Figure 1b implies that only an extremely low HF concentration would preclude PS formation, and such a solution would be impractical for MEMS release.

Phosphorus is an n-type dopant in Si, and holes are required for the galvanic corrosion reaction. Therefore, in phosphorus-doped

Downloaded 03 Mar 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

polysilicon, the holes must be photogenerated. Figure 8a shows typical i–V curves for n-type Si in HF solution, illuminated and in the dark. When the potential is applied in the dark, no current is seen until a very high voltage is reached, much higher than the PS formation region and much higher than the galvanic potential that results from the galvanic action between Au and Si in HF solution. Figure 8b contains polarization curves for phosphorus–polysilicon in 49% HF, illuminated and in the absence of illumination, that confirm this phenomenon. Therefore, to reduce the detrimental effects of galvanic corrosion during MEMS processing, n-type polysilicon should be used, and the HF release should take place in the absence of illumination.

Conclusion

The effects of Au metallization on polysilicon structure during release of MEMS devices in HF solution have been studied. When phosphorous–polysilicon and Au are in contact and exposed to HF solutions, PS forms on the Si surface due to galvanic action. This detrimental galvanic action is established during the conventional release process for phosphorous–polysilicon MEMS devices with Au contact pads. The extent of the corrosion reaction increases with increasing time and HF concentration. The porous regions first develop along the grain boundaries and then extend into the grain interiors. Porosity penetrates deeper than 1 μm after 1800 s in 49% HF.

After removal from the HF solution, the PS pore walls form a surface oxide upon rinsing in DI water and exposure to air. Because the porous network creates easy diffusion paths for air and contains significant surface area, the surface oxide formation continues for a considerable time, and SiO_2 forms deep into the PS layer and eventually through the entire layer thickness of the PS. The resulting microstructure is a composite of polysilicon and SiO_2, with greater SiO_2 content toward the surface of the polysilicon, where the porosity was greatest. Because the electrochemical reactions governing PS formation require holes, the galvanic corrosion effects can be avoided in MEMS processing by using n-type polysilicon and releasing in the absence of illumination.

Acknowledgments

We thank Dr. Xi Shan and Dr. Kui Du for useful discussions.

References

1. K. R. Williams and R. S. Muller, *J. Microelectromech. Syst.*, **5**, 256 (1996).
2. E. K. Chan, K. Garikipati, and R. W. Dutton, *IEEE Des. Test*, **16**, 58 (1999).
3. I. Chasiotis and W. Knauss, *J. Mech. Phys. Solids*, **51**, 1533 (2003).
4. D. C. Miller, K. Gall, and C. R. Stoldt, *Electrochem. Solid-State Lett.*, **8**, G223 (2005).
5. C. L. Muhlstein, E. A. Stach, and R. O. Ritchie, *Acta Mater.*, **50**, 3579 (2002).
6. H. Kahn, C. Deeb, I. Chasiotis, and A. H. Heuer, *J. Microelectromech. Syst.*, **14**, 914 (2005).
7. O. N. Pierron, D. D. Macdonald, and C. L. Muhlstein, *Appl. Phys. Lett.*, **86**, 211919 (2005).
8. R. L. Smith and S. D. Collins, *J. Appl. Phys.*, **71**, R1 (1992).
9. X. G. Zhang, *J. Electrochem. Soc.*, **151**, C69 (2004).
10. C. M. A. Ashruf, P. J. French, P. M. M. C. Bressers, and J. J. Kelly, *Sens. Actuators, A*, **A74**, 118 (1999).
11. M. W. Losey, R. J. Jackman, S. L. Firebaugh, M. A. Schmidt, and K. F. Jensen, *J. Microelectromech. Syst.*, **11**, 709 (2002).
12. G. Lammel, S. Schweizer, S. Schiesser, and P. Renaud, *J. Microelectromech. Syst.*, **11**, 815 (2002).
13. R. W. Tjerkstra, G. E. Gardeniers, J. J. Kelly, and A. van den Berg, *J. Microelectromech. Syst.*, **9**, 495 (2000).
14. H. Kahn, A. Q. He, and A. H. Heuer, *Philos. Mag. A*, **82**, 137 (2002).
15. P. Guyader, P. Joubert, M. Guendouz, C. Beau, and M. Sarret, *Appl. Phys. Lett.*, **65**, 1787 (1994).
16. D. Gräf, M. Gründner, R. Schulz, and L. Munlhoff, *J. Appl. Phys.*, **68**, 5155 (1990).
17. S. K. Ghandhi, *VLSI Fabrication Principles*, p. 373, Wiley, New York (1983).
18. *Energy-Filtering Transmission Electron Microscopy*, L. Reimer, Editor, Springer-Verlag, Berlin (1995).

Downloaded 03 Mar 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp