High Speed CMOS - Si Light Emitters for On-Chip Optical Interconnect

Amitabh Chatterjee and Bharat Bhuva
Department of Electrical Engineering and Computer Science
Vanderbilt University
Nashville, TN 37235

and

William C. Cieslik
Hamamatsu Photonic Systems
360 Foothill Road, Bridgewater, NJ 08807-091
Email: amitabh.chatterjee@vanderbilt.edu

The delays and power requirements associated with long metal lines for 70nm and beyond technologies make on-chip optical interconnects an attractive option. The semiconductor industry has not enthusiastically responded to on-chip optical interconnects due to the difficulties associated with fabrication of optical emitters on Silicon substrate. Most emitters being researched use materials other than Silicon technologies - not compatible with conventional Si fabrication process. Hence, an optical inter-connect incorporating Si light emitter that can be fabricated shows excellent promise. A reverse biased Si-based p-n junction is known to emit broadband visible and infrared light emission in the range of 400-900 nm. Due to indirect band-gap in Si, the speed of operation and power requirement of Si based light emitting diodes has been considered to be non feasible for VLSI implementation. In this paper, the speed of operation of a reverse biased pn junction has evaluated using a streak camera. Power requirement for optical interconnects has been calculated using the experimental value of quantum efficiency. Results from the experiments clearly show that Si-based diodes are capable of operating in minimum of 10's of GHz and will require power less than conventional global metal interconnects on an IC. These results clearly indicate that optical interconnects are a viable option for the future IC technologies.

Introduction

A major roadblock, according to SIA Roadmap at the 70nm node and below; is the problems of global interconnect for which evolutionary approaches look inadequate [1]. Transmission of global signals (such as clock) across an increasing die size with increased R and C from scaling is becoming more difficult with decreasing clock cycle. The concept of all silicon optical interconnects as shown in the fig 1, involving use of Si-based light emitter, receiver and a wave-guide is a novel and revolutionary approach to address the above problem. In this presentation, Si-based light emitting devices are shown to operate with pico-second response time and better power budget than conventional metal interconnects for on-chip global interconnects. Si-based light emitters do not show any adverse effect of accelerated aging through voltage and temperature stressing. The present work demonstrates the viability of optical interconnects for the 70nm and beyond technologies.

Light Emission Behavior in Silicon

Integration of photonics with Si-based technologies had not been attempted successfully due to the difficulties involved in fabricating non-Si-based optical elements on Si substrate. The fact that photodetectors, waveguides, wavelength demultiplexers and modulaters have been fabricated in silicon-based technology makes the Si light emitters a potential for Opto-Electronic VLSI. A reverse biased silicon pn junction emits light between 400 nm and 800 nm and it has been explained due to be combination of following different mechanism (1) inter-band transitions between hot electrons and holes. (2) Direct intra-band electron transitions, Brem-strahlung radiation from hot electrons scattered by charged coulombic centers and phonon assisted electron transitions. (3) Indirect inter-band recombination of electrons and holes under high-field conditions. (4) Intra-band transitions of hot holes between the light and heavy mass valence bands. Fig 1 shows the light emission from silicon p-n junction that has been routed using a fibre having a core of 50μm

Light-Emitting Diodes: Research, Manufacturing, and Applications VI, E. Fred Schubert, H. Walter Yao,
Editors, Proceedings of SPIE Vol. 4641 (2002) © 2002 SPIE · 0277-786X/02/$15.00

to a silicon photo-detector with a signal transmission of 100KHz. Due to the indirect band-gap of Si, light emission from reverse-biased Si p-n junctions is considered slow and inefficient.

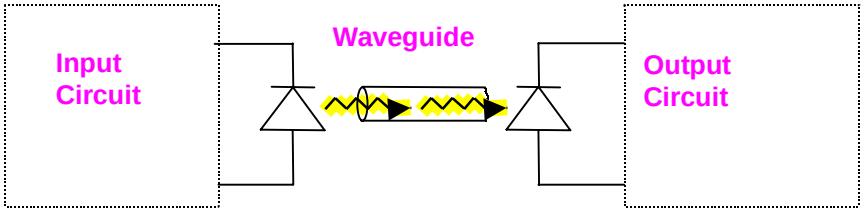

Figure 1 Concept of on-chip optical inter-connects with Si emitter, waveguide, reciever.

Layout Dependency

To address these concerns, light emission behavior from multiple tests structures having different layout scheme and different junction design was evaluated. Fig 2 shows light emitting behavior of a test wafer fabricated with conventional CMOS process and with different layouts for emitters. Quantum efficiency of these test structure were estimated at 2.22×10^{-5}. Light emission behavior was non-uniform at low values of breakdown current, however the flowery structure

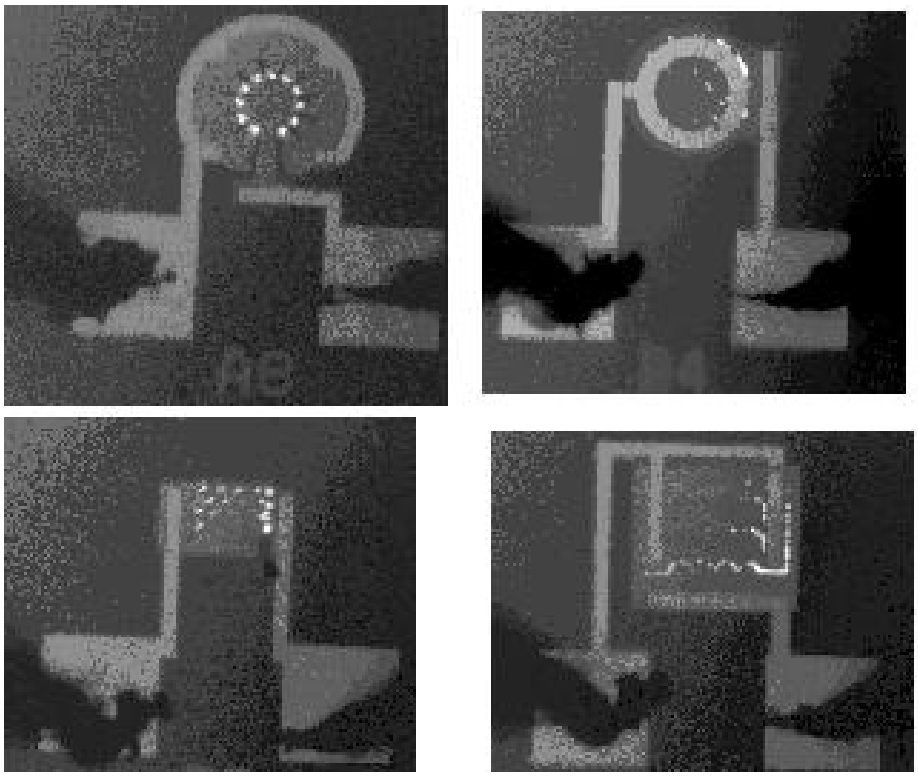

Figure 2 Light emission from test chip having four different structures a) Flowery b) Circular c) Square d) Weave pattern. Strong dependence of light emission was observed on layout.

had more consistent light emission at the sharp corner points. This is consistent with the idea that light emission takes place along the micro-channel called 'micro-plasmas' that have preferential sites of formation depending upon defects or crystal imperfection, creating electric field in-homogeneities across the junction and causing the micro-plasmas to light up.

Efficiency

A comparative study showing the power requirement of such a system with conventional metal interconnects is shown in the Table 1. The power estimation was done using the experimental value for the quantum efficiency of light and the estimates of metal line capacitance from SIA roadmap and published data [2,3]. The power requirements for global interconnects for metal and optical interconnects are equivalent and the differences are negligible when compared with the total power requirements for a chip. Fig 3 shows the threshold for metal inter-connect length beyond which optical interconnects will require less power than metal interconnects. Fig 4 shows a similar comparative study of delay between the two systems. It is evident from these results that optical interconnects are better in terms of power and delay for global connections on a chip.

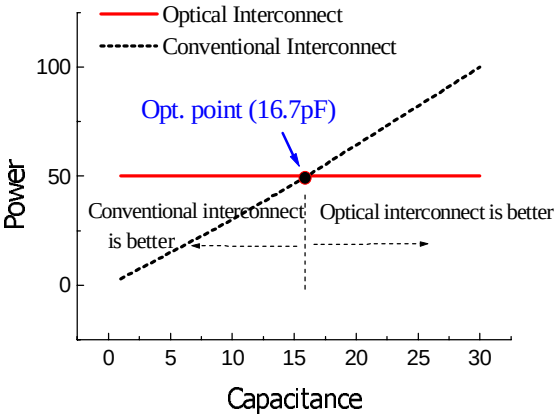

Figure 3 Power comparison between two systems in terms of line capacitance.

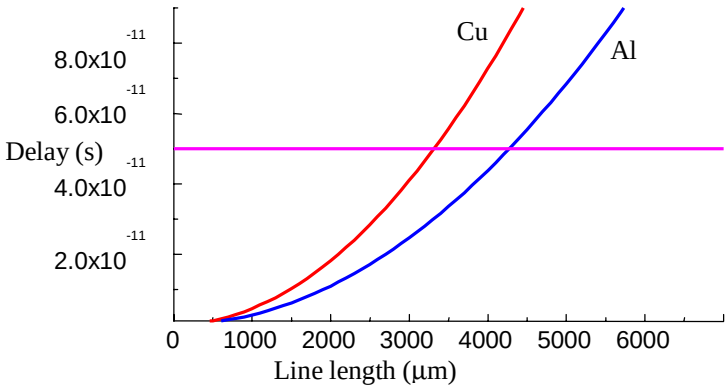

Figure 4 Line delay compared for Aluminum, Copper and optical interconnect.

Table 1. Comparative Analysis of Global Power Consumption for three different clock distribution system, Grid, H-tree and Optical, calculated for three cases. *Case 1* 0.25µm Al , *Case 2* 0.10µm Al, and *Case3* 0.10µm Cu with low-k dielectric.

Power (Watts)	Case 1 0.25µm 2 V 750 MHz Al k=4 16 spines			Case 2 0.10µm 1.2 V 2 GHz Al k=4 28 spines			Case 3 0.10µm 1.2 V 2 GHz Cu k=2 28 spines		
	Grid	H-tree	Optical	Grid	H-tree	Optical	Grid	H-tree	Optical
P_G	0.6	0.6	0.8	1.00	1.00	1.12	0.33	0.33	1.12
P_{Local}	9.42	3.27	3.27	15.82	5.50	5.50	8.35	4.99	5.50
$*P_{Total}$	10.02	3.873	4.07	16.83	6.51	6.62	8.67	5.32	6.62

Speed of operation

Another concern had been the speed of operation for Si-based emitters. High frequency response of the Si-LED was observed by modulating the breakdown voltage across the device. The resulting light modulation was observed using a streak camera with a time resolution of 2ps. In the pulsed mode, 4ns pulses at a repetition rate of 10 KHz were applied to the circuit from the signal generator. Fig 5 shows the streak response to the light emission from the pulsed excitation. An associated ringing with the pulsed excitation modulates the breakdown voltage across the junction. The fact that

the junction responds to the fast ringing in 100 ps range shows the capability of these devices to operate at 10's of GHz range. Fig 6 shows the response of the light emitter to the CW input signal of 1.2 GHz.

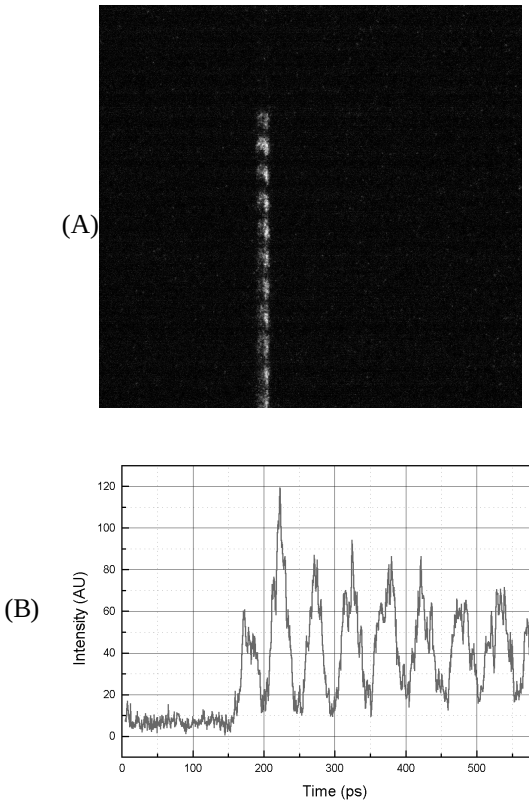

Figure 5 a) Streak Camera (C5680) image of light emission from the pulsed excitation shows the device response in the pico-second range. b) Intensity of light emission vs time plot.

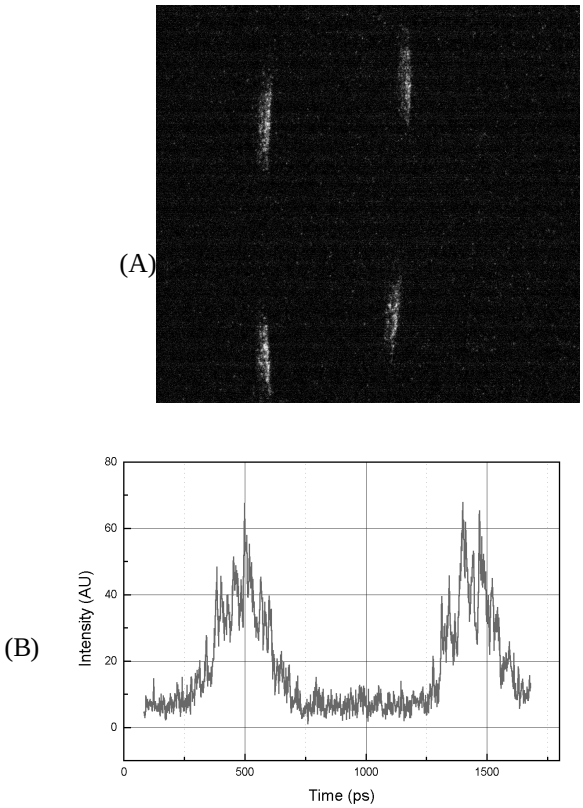

Figure 6 a) Streak Camera (C5680) image of light emission from the CW excitation. b) Intensity of light emission vs time plot.

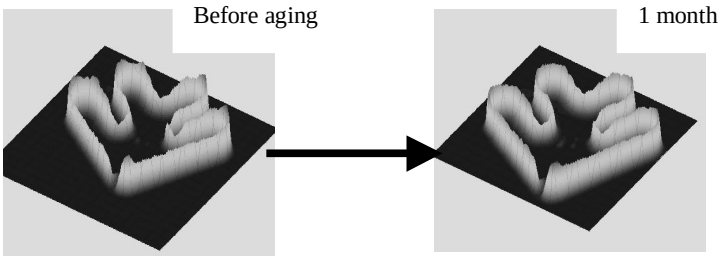

Figure 7 Spatial variation of emission from p-n junction subjected to DC stressing with breakdown current at 46mA. No light coalescence observed.

Reliability

To evaluate the reliability of these emitters, emitters were stressed under different conditions of accelerated stressing - AC, DC (excitation at different breakdown currents) and higher temperature stressing. Fig 7 shows that devices showed no change in emission pattern when stressed at breakdown current higher than 25 mA. However, low

current stressing (<25mA) resulted in a phenomenon of 'light coalescence' with the device aging as shown in the Fig 8. This is a reversible phenomenon as the remission of light coalescence takes place when re-stressed at high current for few minutes as shown in Fig 9. This behavior is consistent with the model of boron compensation due to interfacial hydrogen causing the junction breakdown voltage to vary - resulting in light coalescence [4]. The high current dissociates the hydrogen from boron resulting in the removal of the light coalescence effect.

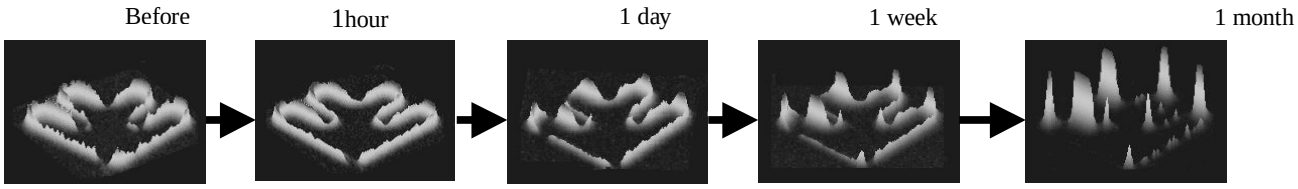

Figure 8. Light coalescence as a function of time under DC stressing with breakdown current at 24mA.

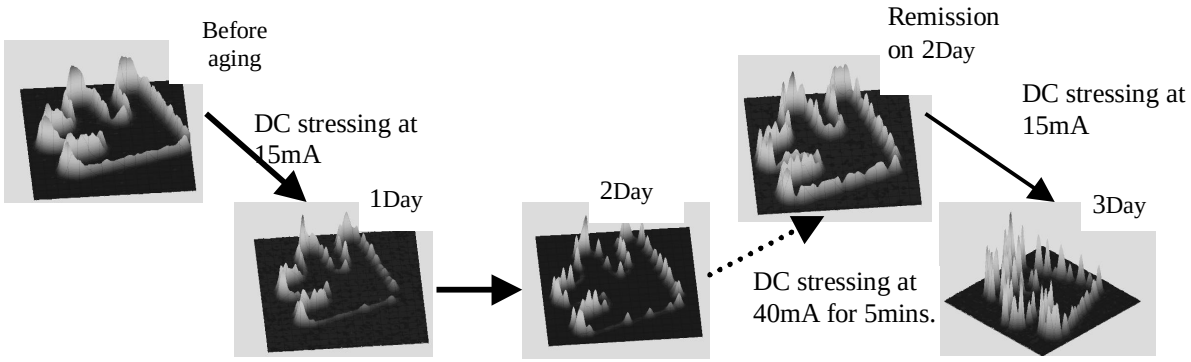

Figure 9. Light coalescence as a function of time under DC stressing with breakdown current at 15mA till the 2nd day. After 5min of high current DC stressing at 40mA, causes remission phenomenon. Coalescence behavior reappears when re-stressed at 15mA for 1day

References:
[1] SIA Roadmap
[2] Brian Floyd et al, "The Projected Power Consumption of a Wireless Clock Distribution System and Comparison to Conventional Distribution Systems" *Proc. of IITC*, June 1999, pp. 248-250.
[3] MOSIS foundry Service
[4] P.K. Gopi et al, "New degradation mechanism associated with hydrogen in bipolar transistors under hot carrier stress," *Appl. Phys. Lett*. August 1993, 63(9), pp. 1237-1230