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Microwave Properties of Schottky-barrier Field-effect Transistors*

Abstract: The microwave properties of silicon Schottky-barrier field-effect transistors (MESFET's) with a gate-length of one micrometer are investigated. The scattering parameters of the transistors have been measured from 0.1 GHz up to 12 GHz. From the measured data an equivalent circuit is established which consists of an intrinsic transistor and extrinsic elements. Some of the elements of the intrinsic transistor, notably the transconductance, are strongly influenced by the saturation of the drift velocity. Best performance of the intrinsic transistor is obtained with highly doped and thin channels. The measured power-gain is in good agreement with theoretical values deduced from the equivalent circuit. The best device has a maximum frequency of oscillation f_{max} of 12 GHz. The investigation reveals that the extrinsic elements, especially the resistance of the gate-metallization and the gate-pad parasitics, degrade the power-gain considerably. Without them a value of f_{max} close to 20 GHz is predicted.

Introduction

Since the invention of the first practical field-effect transistor[1] these devices have always had smaller cutoff frequencies than bipolar transistors. However, in the last few years the frequency gap began to close, especially after the Schottky-barrier field-effect transistor (MESFET) appeared on the scene.[2-5] Recently, a Si-MESFET was realized with a maximum frequency of oscillation of 12 GHz,[6,7] which is considerably higher than for previously known FET's and at least as high as for the best bipolar transistor of today. In the present paper the microwave properties of such MESFET's are described.

A prime requirement for good high-frequency performance is a small carrier transit time in the device. This has been obtained by using a gate length of only one micrometer and a channel design which allows full use to be made of the limited drift velocity. In addition, parasitics have to be kept low, a goal which still has not been met in every respect.

Device description

MESFET's have been prepared in a number of ways in our laboratory.[8-12] Only the properties of the best design with respect to microwave performance will be dealt with in the following sections. The technological features of this design are discussed in detail elsewhere.[10-11] For convenience, a brief description of the device geometry is repeated here. The cross section is shown in Fig. 1 and a top-view photograph in Fig. 2.

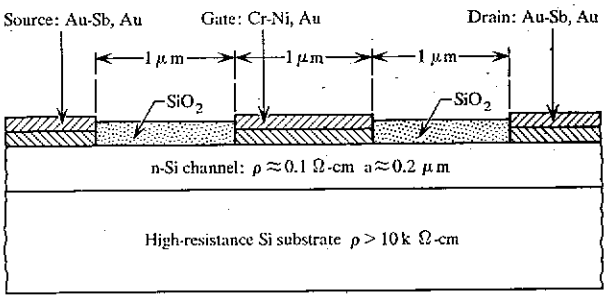
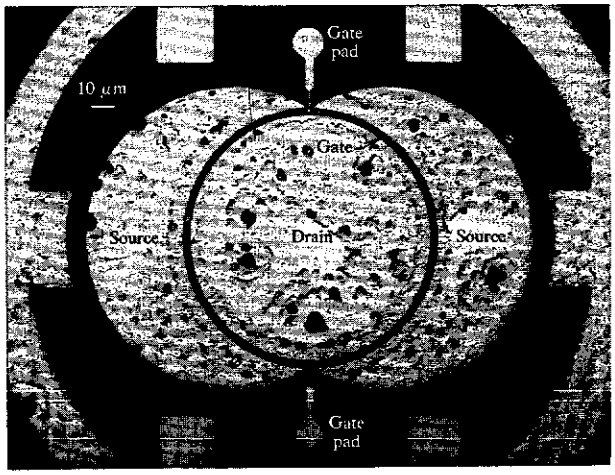


Figure 1 Cross-section of a Schottky-barrier FET.

Figure 2 Microphotograph of the top-view of a Schottky-barrier FET.



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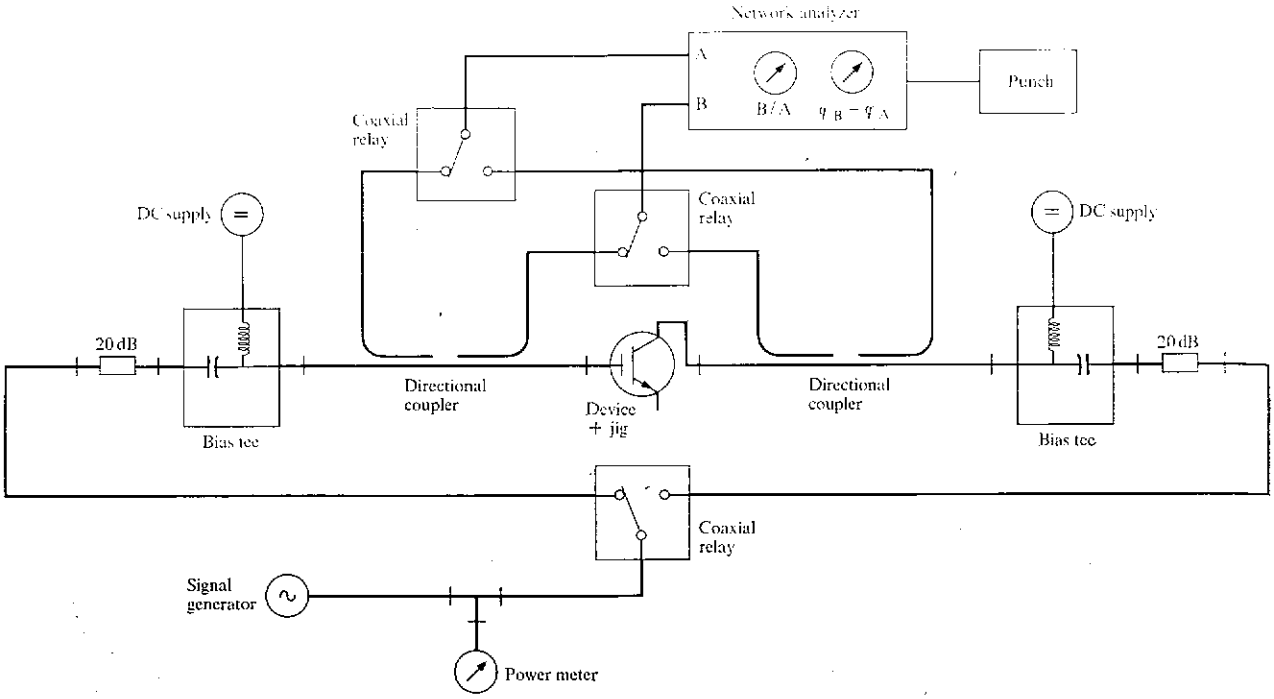


Figure 3 Schematic diagram of the setup for the measurement of the *s*-parameters from 0.1 GHz to 12 GHz. Thick lines symbolize 50-ohm coaxial lines.

High-resistance silicon is used as a substrate. Compared to a p-substrate, this material keeps parasitics low, especially at the drain, where they are most harmful. The channel is n-doped with a concentration of about 10^{17} cm^{-3} and has a thickness between 0.1 and 0.2 micrometer. A special low-temperature epitaxial process is used for the fabrication of the channel.[12] The low temperature ($T \approx 950$°C) also prevents conversion of the substrate to a low-resistivity state. The gate, made by means of the projection masking technique,[10] has a length of one micrometer, a width of 400 μm, and consists of a Cr-Ni sandwich of about 0.05 μm thickness. To reduce the resistance of the gate it is electroplated with gold. Source and drain contacts are a complicated sandwich that consists mainly of gold-antimony alloyed to the silicon. New metallurgical processes are used[11] which considerably facilitate fabrication of the small structures required.

As seen in Fig. 2, the gate encloses the drain completely. In this way, leakage paths from source to drain which could increase the drain conductance are prevented. In order to decrease the adverse effects of the resistance of the gate metallization, contact to the gate is made on two sides by means of two pads. For simplicity these pads are placed directly on the n-layer. Accordingly they are Schottky contacts. In order to reduce parasitics the pads are made quite small and removed from the transistor as far as possible.

Microwave measurement techniques

• *Measurement of scattering parameters*

The two-port parameters of the transistors, most convenient to measure in the microwave range, are the scattering parameters.[13,14] They have been obtained between 0.1 and 12 GHz with the setup shown in Fig. 3. To extract the incident wave and the waves reflected and transmitted by the transistor, dual directional couplers are used. For the broad frequency range, two different sets are required, from 0.1 to 2 GHz model 778 D, and from 2 to 12 GHz model 8472 A, of Hewlett Packard. The amplitudes and phases of the signals at the coupler ports are measured with the Hewlett Packard network analyzer, model 8410 A. The various ports are selected by three coaxial relays. The connections shown in the figure are for measuring s_{11}.

By means of a digital voltmeter and encoding units the results are transferred to punched cards on an IBM punch. The measurement sequence and the setting of the relays are controlled by the program drum of the punch. Further processing is carried out on an IBM System/360 computer, Model 50. The dc power for the transistors is brought into the transmission line system by two newly designed broadband dc-insertion units working from 0.1 to 2 GHz and from 0.5 to 18 GHz.[15]

For ease of handling, the transistor chips are mounted into packages. Mostly T0-46 headers are used, sometimes

also LID-housings (Versa-Pak 4-Post LID, made by Frenchtown/CFI). These packages are connected to the 50-ohm coaxial line system by carefully compensated jigs. In Fig. 4 the T0-46 jig is shown. It has a reflection coefficient Γ of less than 0.1 up to 6 GHz. The LID jig has a $\Gamma \lesssim 0.1$ up to 12 GHz.

The equivalent circuit of the T0-46 header as deduced from measurements is given in Fig. 5. It is valid to about 6 GHz. The losses of the header are negligibly small. Care has been taken to avoid coupling between input and output of the header. Capacitive coupling between the leads is negligible (<0.01 pF). Coupling via the source-lead inductance is minimized by bonding the source of the transistor with four gold wires to the bottom of the header and by grounding the bottom on the metallic block of the jig without a lead. By these measures the source inductance is reduced to 0.15 nH.

For applications, the T0-46 case is not very well suited because its lead capacitances are comparable to those of the transistor. The LID package is much better in this respect; however, its inductances might pose some problems above approximately 6 GHz.

Care has been taken to make the paths of the reflected and transmitted signals via the jig, the couplers, and the coaxial relay to the test channel of the network analyzer as closely equal (electrically) as possible. In this way it is assured that the reference planes at the input and output of the jig are in a symmetric position with respect to each other. The admittances of the transistors are in most cases below 20 millimhos. Therefore, as a reference for coupler calibration, the open-circuit condition is chosen and not, as is more usual, a short circuit. By this means some of the errors due to the couplers and to the line discontinuities are reduced and the precision of the measurements is considerably increased at low frequencies. The open circuit is simply realized by removing the transistor from the jig. The unterminated, very small coaxial lines of the jigs are a reasonably good open circuit. The electrical reference plane is only slightly above the mechanical plane ($\approx$ 0.25 mm for the jig in Fig. 4) and the radiation loss is negligible. Better calibration and error-correction schemes are still possible[16] but have not been necessary so far.

The measurements yield the s-parameters of the combination chip and package. From these values the computer subtracts the equivalent circuit of the package and, finally, after a conversion, the admittance parameters (y-parameters) of the chip alone are obtained. The conversion is made because y-parameters are more convenient for device design and evaluation than s-parameters. In Fig. 6 the y-parameters of a chip measured in a LID-package are shown in the complex plane. Due to the relatively large contribution of the package the chip data are less precise than the data for the combination chip and package. Near 8 GHz the bond wire inductance resonates with the

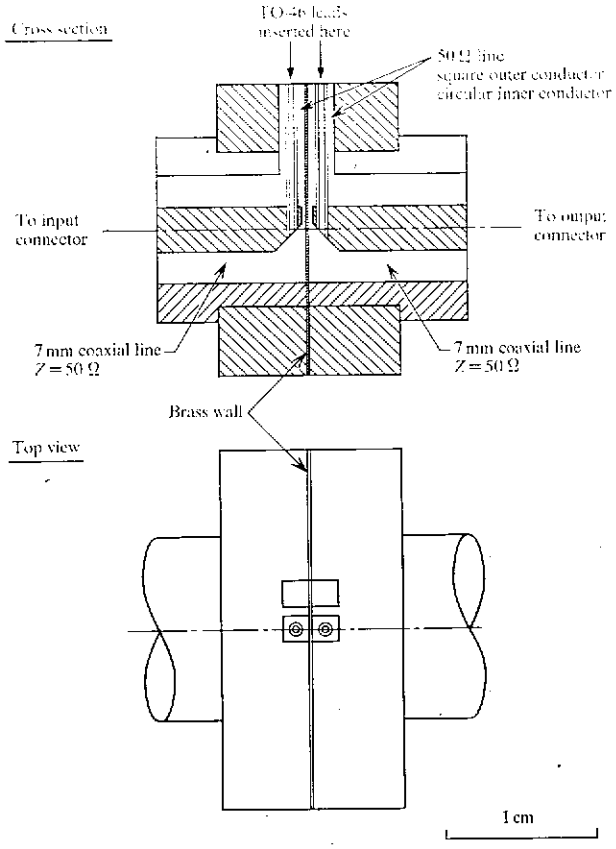
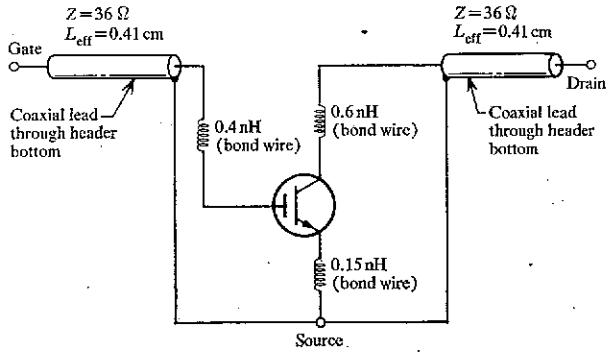


Figure 4 Cross-section of the test-jig for T0-46 headers.

Figure 5 Equivalent circuit of the T0-46 header as measured in the jig shown in Figure 4.



gate capacitance. Therefore above approximately this frequency the chip data become unreliable.

From the measured s-parameters the unilateral gain U (Ref. 17), the stability factor k and for $k \geq 1$ (unconditionally stable transistor) the maximum available gain MAG, or alternatively for $k < 1$ (potentially unstable transistor) the maximum stable gain MSG (Ref. 18) are computed.

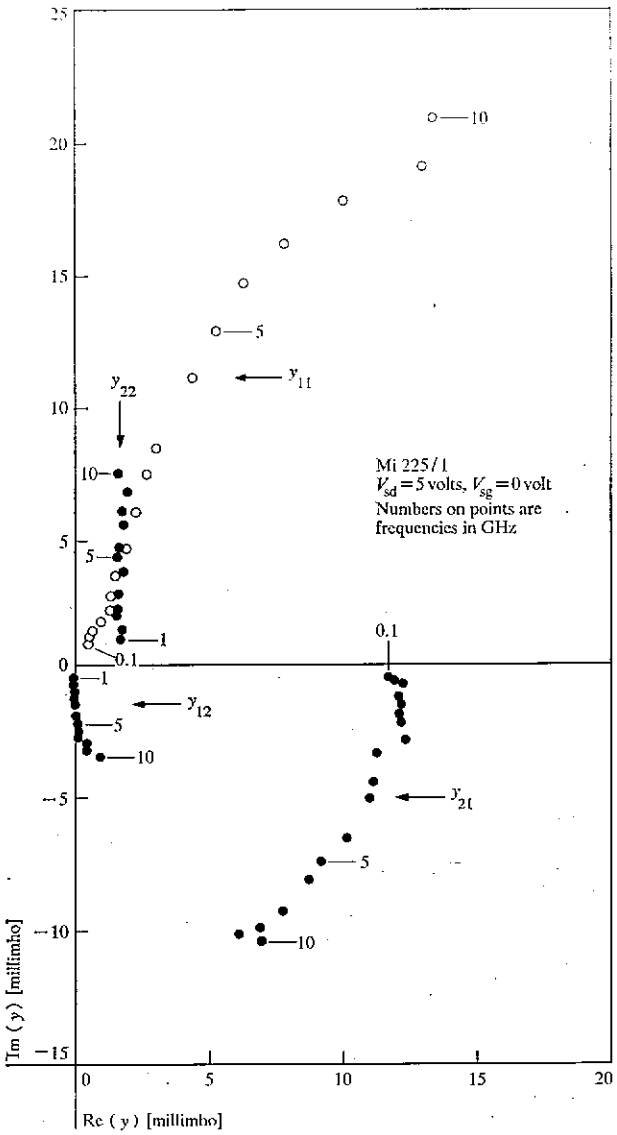


Figure 6 Measured y-parameters of a Schottky-barrier FET. Measuring frequencies, starting from the real axis are 0.1, 0.15, 0.2, 0.3, 0.5, 0.7, 1.0, 1.5, 2.0, 2.5, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, and 10.0 GHz, except for y_{12} and y_{22} where the sequence starts with 1.0 GHz.

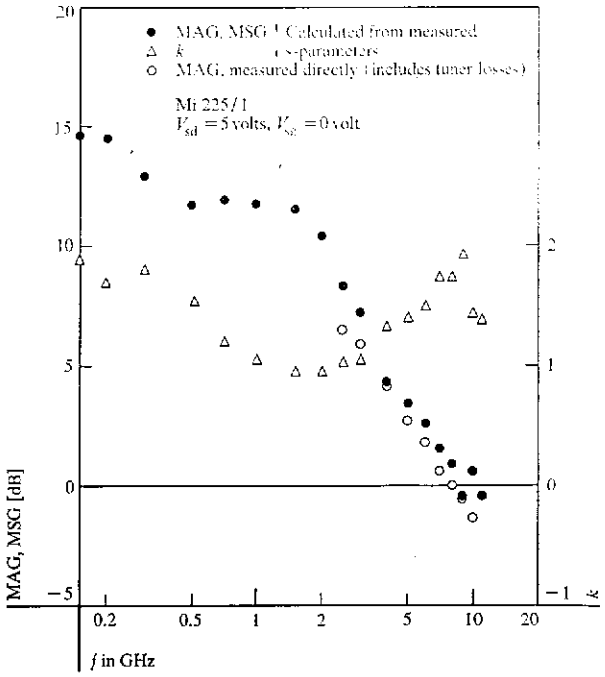


Figure 7 Measured maximum available gain MAG and stability factor k of a Schottky-barrier FET. In the small region, where $k < 1$, the maximum stable gain MSG is given instead of MAG.

The unilateral gain U has the property that it is not influenced by lossless header parasitics and some of the jig and line discontinuities. The same is true for the quantities k, MAG, and MSG provided that in addition no header or jig parasitics exist which lead to a coupling between input and output. As already mentioned all these conditions are well fulfilled for our setup and the packages. Therefore from the s-parameters the aforementioned gain parameters of the chip can be computed without any necessary correction for package parasitics, etc. Compared to the determination of the y-parameters of the chip, where the correction for package parasitics introduces considerable errors, the precision of the results is much better. MAG, MSG and U can be determined up to 12 GHz with errors of less than one dB. Results for one of the transistors are shown in Fig. 7.

• *Direct measurement of maximum available gain*

For determining MAG, a direct method has also been used[19] which is simple and fast. The setup is shown in Fig. 8 and operates in a range from 2 GHz to 14 GHz. The maximum available gain is obtained by simultaneous matching of input and output of the transistors. This is accomplished with slug tuners. The network analyzer serves as a gain indicator. If it were replaced by a power-meter, a range up to 18 GHz could be obtained. As already mentioned, header parasitics and line disturbances do not influence the value of MAG. However, the slug tuners are not loss-free, therefore the measured gain is too small by as much as 2 dB. This can be seen in Fig. 7, where directly measured MAG and MAG as computed from measured s-parameters are shown. It is clear that this tuning method is only applicable if the transistors are unconditionally stable ($k > 1$) at the measuring frequency. This is well fulfilled for most of our transistors. The transistor in Fig. 7 has a small range where k is slightly less than one. However, due to the tuner losses no instabilities occurred in that range.

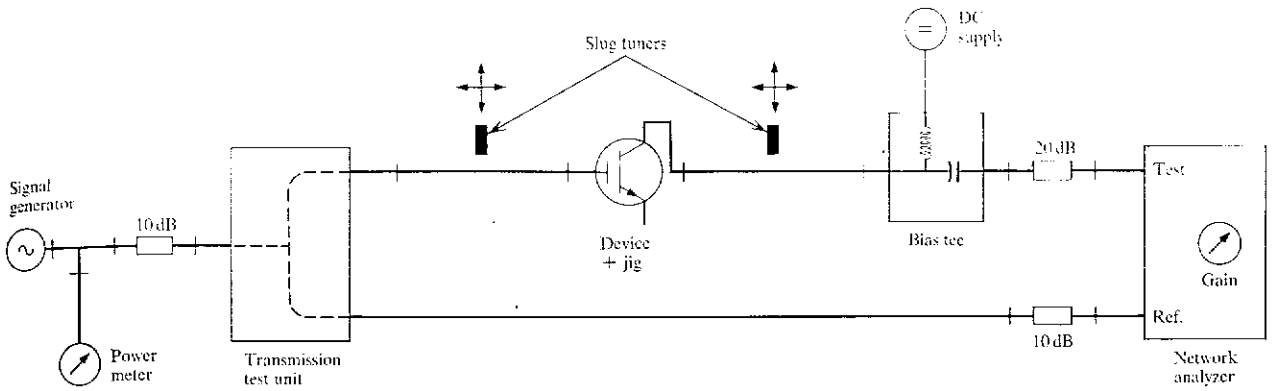


Figure 8 Schematic diagram of the setup for the measurement of the maximum available gain MAG from 2 GHz to 14 GHz. Thick lines symbolize 50-ohm coaxial lines.

Results

• *The y-parameters*

Before going into details, a brief discussion of the measured y-parameters is appropriate. As shown in Fig. 6 the forward transadmittance y_{21} responsible for the amplifying character of the device has a real value of about 12 millimhos at low frequencies. With increasing frequency, y_{21} shows an increasing phase-shift, which is 45° at about 6 GHz. However, the magnitude of y_{21} stays constant up to 10 GHz, the highest frequency measured. Therefore, y_{21} does not set the frequency limit of the device, which is true in general for all types of FET's.

The imaginary and real parts of the input admittance y_{11} increase with frequency. The imaginary part is caused by the gate capacitance and some parasitic capacitances. The real part, which makes the input lossy, is due to various resistive contributions to be dealt with in detail later. The power gain is approximately inversely proportional to Re (y_{11}). Accordingly, the frequency response and the frequency limit of power gain are mainly determined by the real part of y_{11}.

The output admittance y_{22} consists of a nearly frequency-independent real part, caused by the drain conductance, and a capacitive imaginary part.

The reverse transadmittance y_{12} is capacitive except at higher frequencies and is relatively small. Therefore feedback effects are not large in the device.

• *The equivalent circuit*

An approximate equivalent circuit of the MESFET is shown in Fig. 9. Also shown is where the elements of the equivalent circuit are located in the transistor structure. In Table 1 typical values are given. The equivalent circuit consists of the intrinsic transistor with elements g_m, C_{sg}, R_i, G_d, and C_{dg}, and of the extrinsic, unwanted elements R_s, R_g, C_{sd}, R_L, and C_L. It is not possible to establish an

Figure 9 Equivalent circuit of a Schottky-barrier FET (bottom). In the cross-section of the transistor (top) it is shown where the circuit elements are located.

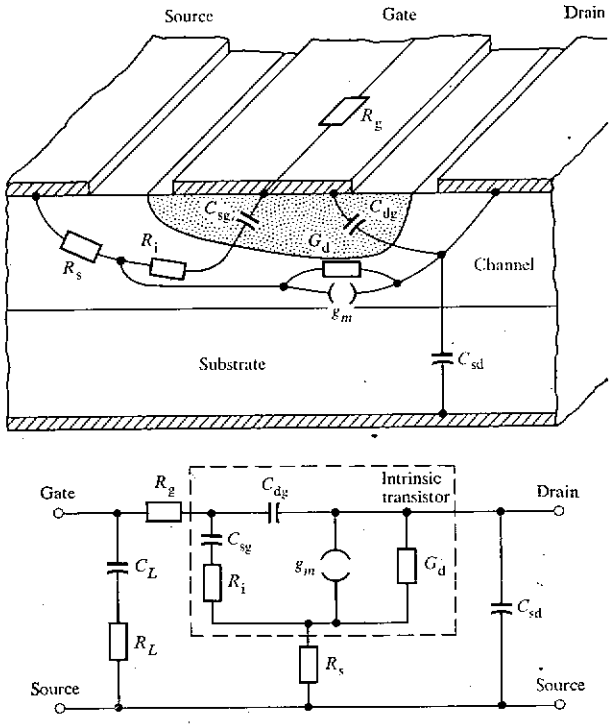


Table 1 Circuit elements of a Schottky-barrier FET.

Mi 212/3 V_{sd} = 5 volts	V_{sg} = 0 volts gate: 1 μm × 400 μm
C_{sg} = 0.47 pF	g_{m0} = 17 millimho,
C_{dg} = 0.07 pF	τ_t ≈ 5 psec,
R_i = 7.5 ohms	G_d = 1.5 millimho
R_s = 11 ohm,	C_{sd} = 0.05 pF
R_g = 11 ohm,	
C_L = 1 pF,	
R_L = 400 ohm	

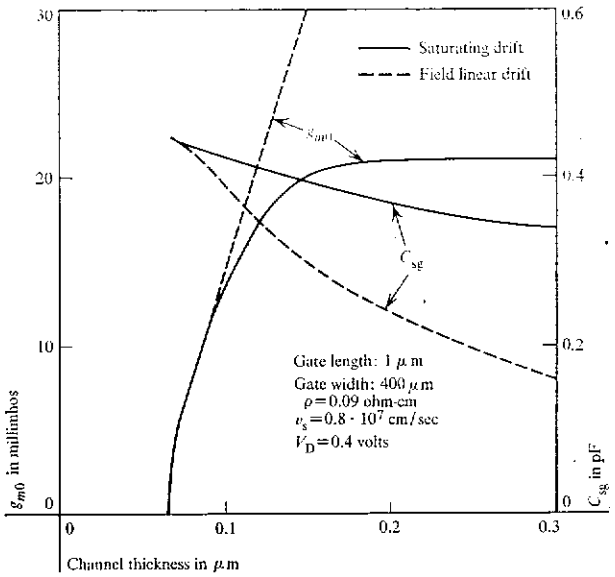


Figure 10 Theoretical values of the transconductance g_{m0} and the source-gate capacitance C_{sg} as a function of the channel thickness.

equivalent circuit from the measured y-parameters (Fig. 6) alone. Various test structures and additional measurements are necessary. Most important is a transistor structure without gate. From it the source-gate resistance R_s and the admittance of the gate pads (R_L, C_L) has been deduced.

a) The intrinsic transistor

The properties of the intrinsic transistor are governed by the saturation of the drift velocity. For electrons in Si with a doping of 10^{17} cm^{-3}, saturation sets in at an electric field $E_S \approx 15$ kV/cm and the saturated velocity is about 10^7 cm/sec (Ref. 20). It is plausible that these effects become significant if in the channel a voltage drop of about $W_S \approx L \cdot E_S$ occurs (L = gate-length), and if at the same time pinch-off is not reached. Under these circumstances the field in the channel is so high that current saturation is caused by drift saturation and not by channel pinch-off. With a 1-μm long channel $W_S \approx 1.5$ V. Accordingly drift-saturation effects are expected to become dominant for channels with pinch-off voltages of more than about 1.5 V. Theoretical values of the transconductance g_{m0} and the source-gate capacitance C_{sg} as a function of the channel thickness are shown for current saturation in Fig. 10. The derivation of these results based on a modified gradual-case theory[1] is given in Appendix A. The gate bias caused by the diffusion voltage $V_D \approx 0.4$ V of the Schottky gate has been taken into account as well as the additional bias owing to the dc current flowing through the source-gate resistance R_S. For comparison, not only saturating drift (full lines) but also field linear drift (broken lines) is assumed.

In channels up to 0.06 μm no current flows because they are depleted by the diffusion voltage of the Schottky gate. For thicker channels conduction sets in and g_{m0} increases rapidly, whereas C_{sg} decreases slowly. However, at about 0.1 μm the influence of drift saturation becomes apparent, which finally, above 0.15 μm, causes g_{m0} and C_{sg} to become roughly constant. If no drift saturation existed then g_{m0} and C_{sg} would still considerably increase or decrease, respectively, with channel thickness. This figure clearly demonstrates that drift saturation is a serious effect with 1 μm gates.

The experimental results are in satisfactory agreement with Fig. 10. It is indeed found that g_{m0} and C_{sg} are about constant for channels thicker than 0.15 μm. The experimental values of g_{m0} are around 15 millimho, somewhat lower than the theoretically predicted value of 21 millimho. The experimental C_{sg} scatters around the theoretical value of about 0.40 pF. For reasons to be explained later, a channel thickness of 0.15 μm was chosen for most devices.

The intrinsic gain-bandwidth product $f_0 = g_{m0}/2\pi C_{sg}$ theoretically amounts to 9 GHz. The experimental value is about 6 GHz.

The transconductance is frequency dependent, because of the RC-transmission line character of the FET. A low-order series expansion in frequency, sufficient for our purposes, would look like

$$g_m = g_{m0}(1 - j\omega\tau_t - \omega^2\tau_u^2 + \cdots).$$

The time constant τ_t has been derived in Appendix A; values are given in Fig. 11. The assumptions made are the same as for Fig. 10. For the channel thickness of 0.15 μm most often used, $\tau_t \approx 5$ psec. This would lead to a 45° phase-shift of g_m at $f_{45} = 1/2\pi\tau_t \approx 30$ GHz. In order to predict the absolute value of g_m, the coefficient of the ω^2-term has to be known, which we did not calculate. From other theoretical investigations[21,22] it seems that $|g_m|$ stays nearly constant up to at least f_{45}. The constancy of the measured $|y_{21}|$ up to 10 GHz lends support to this prediction. However, it is difficult to test the theoretical value of τ_t, because, as will be dealt with later [see Eq. (C5d) of Appendix C] it is not only τ_t that contributes to the phase-shift of y_{21}, but also the feedback capacitance C_{dg} and the extrinsic elements R_s and R_g. As can be seen from Fig. 6 all these contributions lead to a 45° phase-shift of y_{21} at $f_{45} \approx 6$ GHz, which corresponds to a time constant of roughly 25 psec. It was not possible to extract a good value for τ_t from these results, but it seems that the theoretical value of τ_t is consistent with the experimental findings.

A similar situation exists for the gate time-constant $\tau_i = C_{sg} \cdot R_i$. As follows from Fig. 11, a value of about 3 psec is predicted for a channel thickness of 0.15 μm, leading to a resistor R_i of roughly 7 ohms. Due to this

resistor a lossy input with a conductance Re $(y_{11}) \approx \omega^2 C_{sg}^2 R_i$ is expected. Again due to some of the extrinsic elements the measured input-conductance is much higher. If their contributions are subtracted, the theoretically expected order for R_i is found.

The feedback capacitance C_{dg} of about 0.07 pF is quite small. As can be seen in Fig. 9 it is a fringe capacitance at the drain end of the depletion layer, which from rough, theoretical considerations should be of the order of $\varepsilon\varepsilon_0 \cdot$ (gate-width) $\approx$ 0.04 pF. This is in satisfactory agreement with the measurements.

The drain conductance G_d of 1.5 millimho is rather high. As a consequence the open-circuit dc voltage gain $\mu = g_m/G_d$ has only values of about 10. For a microwave transistor which anyway has a small gain per stage this is acceptable. Nevertheless, somewhat higher values of μ would be desirable. Theoretically it is very difficult to predict G_d, a situation which in general is found for all types of FET's. In our case G_d seems to be caused by an electrostatic feedback from the drain epitaxial layer via the high-resistive substrate to the channel below the gate.[23] The drain, so to speak, acts as a remote gate with a positive bias. In agreement with this picture it was found experimentally that a p-substrate gives smaller values of G_d because the p-material shields the channel below the gate from drain fields. However, we found that the improvement in G_d with p-substrates is completely offset by the increase in parasitics. Therefore a high-resistive substrate seems to be the better choice despite its adverse effects on G_d.

Finally, we will discuss how the design of the channel influences the elements of the intrinsic transistor. For this discussion it is convenient to use the channel-doping N_D and the pinch-off voltage, $W_0 = (1/2)(eN_D/\varepsilon\varepsilon_0)a^2$, as parameters. For the moment W_0 is kept constant, which requires that if N_D be varied the channel thickness a has to vary as $1/\sqrt{N_D}$. In Appendix A some of the intrinsic elements are derived. Only g_{m0} is given explicitly there, however, it is easy to see that one can write

$$g_{m0} = \frac{1}{R_0} f_1(\mathrm{s}, \mathrm{d})$$

$$C_{sg} = C_0 f_2(\mathrm{s}, \mathrm{d})$$

$$\tau_t = R_0 C_0 f_3(\mathrm{s}, \mathrm{d})$$

$$\tau_i = R_0 C_0 f_4(\mathrm{s}, \mathrm{d})$$

with

$$R_0 = \frac{L}{\mu e N_D a} \approx \frac{1}{\sqrt{W_0 \cdot N_D}}$$

$$C_0 = \frac{\varepsilon\varepsilon_0 \cdot L}{a} \approx \sqrt{\frac{N_D}{W_0}}.$$

For constant W_0 and constant bias voltages, the relative height s of the depletion layer at the source is constant. If in addition the weak dependence of the mobility on doping is neglected, then the saturation parameter W_s/W_0 and hence the relative channel height difference d at the drain is constant. Therefore, for constant W_0, it is found:

$$g_{m0} \sim \sqrt{N_D}$$

$$C_{sg} \sim \sqrt{N_D}$$

$$\tau_t = \text{const}$$

$$\tau_i = \text{const}.$$

This means that if N_D is increased with unaltered W_0 then g_{m0} and C_{sg} increase, whereas the time constants do not change. Apparently the gain-bandwidth product $f_0 = g_{m0}/2\pi C_{sg}$ is constant, too. A change of the channel parameters has little effect on the feedback capacitance C_{dg}. Also there is experimental and theoretical evidence that the drain conductance for fixed W_0 does not depend much on N_D. This means roughly

$$\frac{g_{m0}}{C_{dg}} \sim \sqrt{N_D}$$

$$\frac{g_{m0}}{G_d} \sim \sqrt{N_D}.$$

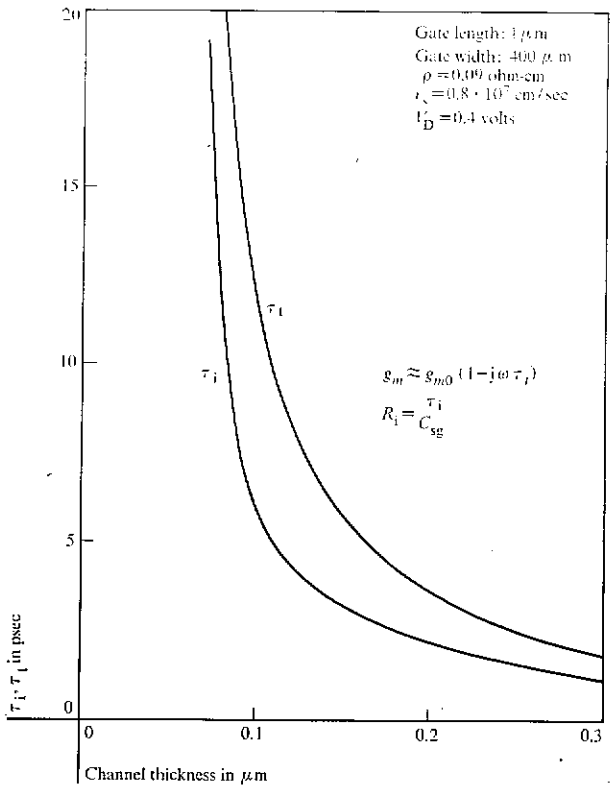


Figure 11 Theoretical values for the time constants τ_i and τ_t as a function of the channel thickness.

From these equations it is clear that for a given W_0 it is advantageous to make the channel doping N_D as high as possible because it not only increases the transconductance g_{m0}, but more important, it decreases the relative influence of the feedback capacitance C_{dg} and increases the dc open-circuit voltage-gain g_{m0}/G_d. However, an increase in N_D decreases the breakdown voltage of the gate. This limits the doping level to about $2 \cdot 10^{17}$ cm^{-3} for our present Schottky-gate technology. Breakdown occurs at the drain edge of the gate, as expected. The breakdown-voltage is less than one-half of that of a planar Schottky junction with guard-ring. Therefore some improvements seem possible in the future, nevertheless a doping of 10^{18} cm^{-3} might be an upper limit, at least for step-junctions.

After N_D has been varied with constant W_0, W_0 is now varied and N_D kept fixed. This means that the channel-thickness a is varied alone, a situation which has already been discussed and shown for g_{m0}, C_{sg}, τ_t and τ_i in Figs. 10 and 11. Because C_{dg} is roughly a constant, the ratio g_{m0}/C_{dg} behaves as g_{m0}. Experimentally it is found that the ratio g_{m0}/G_d decreases with increasing W_0. Therefore some of the elements improve with W_0, others get worse. As a compromise for W_0 and consequently for the channel thickness a with fixed N_D, a value was chosen where drift-saturation just became important, which in Fig. 10 corresponds to $a \approx 0.15$ μm. In terms of the saturation parameter this choice means $W_s/W_0 \approx 0.5$. In this way highest g_{m0} is obtained but at the same time the drain current and the pinch-off voltage kept as low as possible.

To summarize this discussion, doping in the channel is increased until the gate breakdown voltage sets a limit, and the pinch-off voltage is made large enough so that drift-saturation effects just become dominant. This channel design seems to be good for a small-signal microwave transistor, but of course not necessarily for other applications.

b) Extrinsic elements

The extrinsic elements are undesired parasitic contributions. In our present transistor design the technology was kept as simple as possible. To some extent this had to be paid for by large parasitics.

The series resistance R_s in the channel between source and gate is due to the limitations of our present photolithographic techniques with which the source-gate spacing as well as the gate-length cannot be made much smaller than one micron. As shown in Appendix C the influence of R_s on the y-parameters is relatively complicated. Feedback effects of R_s are less than 30% and mostly compensate themselves, because not only is g_{m0} decreased, but C_{sg} and G_d, too. The most adverse effect of R_s is that it increases the input loss; the contribution to the input conductance is about the same as that of R_i. Also R_s in combination with C_{sg} adds to the phase-shift of y_{21} by an amount similar to the intrinsic phase-shift of g_m.

Due to the stripping techniques[11] used in the production of the transistor, metallizations are very thin. Moreover the gate is quite narrow and long. Therefore despite electroplating, the gate resistance is very high, about 100 ohms per 100 μm. The metallization resistance together with the gate capacitance is distributed along the width of the gate and forms a transmission line. In Appendix B it is shown that such a line if connected at one end and open-circuited at the other behaves, at not too high frequencies, as if to the gate a resistor R_g is connected which is $\frac{1}{3}$ of the metallization resistance measured from one end to the other. For a 400 μm long gate connected at one side, R_g would be about 130 ohms, considerably higher than the resistors R_s and R_i. In order to decrease R_g the layout of the transistor was made in such a way that four gates each 100 μm wide are connected in parallel. In this way the effective resistance R_g is cut down to about 10 ohms. To do this parallelling, as Fig. 2 shows, two gate bonding pads are provided. Two gate legs each consisting of a 90° section of a circle and being 100 μm long are connected to each pad. In order to form a closed structure, the free ends of the legs are connected together pairwise. The influence of R_g on the y-parameters is given in Appendix C. R_g contributes to the input conductance by a similar amount as R_i and R_s. It also causes a similar phaseshift of y_{21} as R_s.

The gate bonding pads are another important source of parasitics. As mentioned earlier, to simplify the technology they are Schottky contacts as the gate on the epitaxial n-layer. Their diameter is only 17 μm; nevertheless their area is relatively large, leading to a parasitic capacitance C_L of about one pF. In order to diminish this capacitance, the gate pads are removed from the source metallization as far as possible (Fig. 2). The capacitive currents flowing through the Schottky junction of the pads therefore have also to flow through the n-layer to the source. This resistive path R_L in the n-layer amounts to about 400 ohms. At sufficiently high frequencies, $\omega \gg 1/R_L \cdot C_L$, only R_L is seen at the input. Near 10 GHz this contribution to the input loss is small (about 10%) compared to that caused by R_i, R_s and R_g. However, in the frequency range 100 MHz to about 2 GHz, the resistor R_L is the dominant source of input loss. The representation of the gate pads in the equivalent circuit by a series connection of C_L and R_L is a simplification. In reality, the pads are quite a complicated distributed structure.

• *Power-gain*

The power-gain of one of the transistors is shown in Fig. 7. At low frequencies the maximum available gain MAG has values between 10 dB and 15 dB and varies

slowly with frequency. At higher frequencies a more rapid decrease sets in with a slope between 3 dB and 6 dB per octave. The maximum frequency of oscillation f_{max} is reached at about 9 GHz. The best transistors had an f_{max} of 12 GHz. The unilateral gain U, not shown in the figure, is not much different from MAG. The stability factor k is large at low and high frequencies and has a minimum near 2 GHz. Most of the transistors are unconditionally stable ($k > 1$) in the whole frequency range measured. The transistor in Fig. 7 is somewhat exceptional because its k is slightly less than one near 2 GHz.

It will now be shown how the gain parameters are related to the equivalent circuit and what the influence of the extrinsic elements is. This will be done in two ways, with an exact computer calculation of the gain parameters, and in order to get more insight into the results, with approximate formulas which are derived in Appendix C.

For the stability factor k in Appendix C the following approximate frequency dependence is found:

$$k \approx \frac{k_1}{\omega} + k_2\omega. \qquad \text{(C7b)}$$

This dependence has the right form to explain the measured results in Fig. 7. The behavior is a peculiarity of our present transistors, because the factor k_1 is due to the pad losses. In better designs with negligible gate-pad losses one would expect k to be proportional to ω, which means that at low frequencies the transistors should be potentially unstable. This result should hold in general for all relatively loss-free FET-triodes and is related to the fact that FET's have a high input impedance.

For the gain computations the equivalent circuit of Fig. 9 with the values of Table 1 has been used. In the stable region ($k > 1$) MAG is given as a gain parameter. The unilateral gain U turns out to be not much different, as follows also from the approximate formulas. In the potentially unstable region ($k < 1$) the maximum stable gain MSG and the unilateral gain U are possible gain parameters. This corresponds to two extreme methods of stabilizing an amplifier. One is to neutralize the transistor with U as the resulting power-gain, if input and output of the transistor are matched to signal source and load, respectively. The other is padding the input and output of the transistor with resistors until unconditional stability ($k = 1$) is reached with MSG as the resulting gain. Usually U is considerably larger than MSG. Under practical circumstances, depending on the sophistication of the circuit, a stable gain between MSG and U should be obtainable. In the following for $k < 1$ only MSG will be given, which accordingly is a somewhat pessimistic measure of the gain.

For the computations three assumptions on the extrinsic elements have been made. The resulting gain curves are shown in Fig. 12 with full lines for MAG and broken lines for MSG. Curve 1 is for the full equivalent circuit of Fig. 9. For comparison, the measured MAG of the transistor (the elements of which are given in Table 1) is shown. For curve 2 the gate-pad parasitics C_L and R_L and the gate-metallization resistance R_g are assumed to be absent. Finally, curve 3 has been calculated for the intrinsic transistor only, $R_L = C_L = R_g = R_s = 0$.

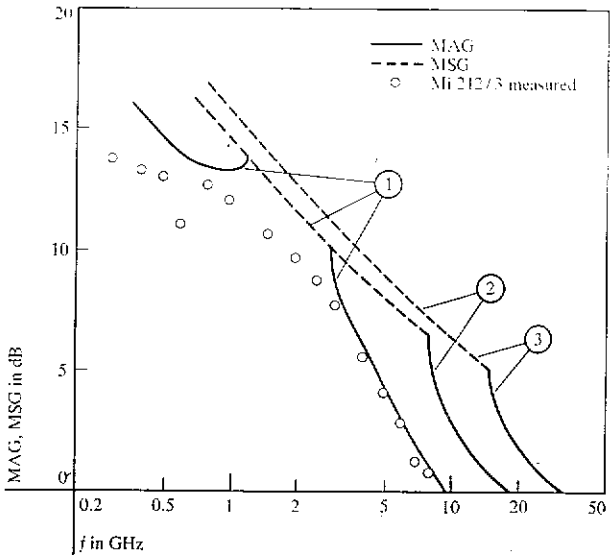


Figure 12 Theoretical power-gain of a Schottky-barrier FET as deduced from the equivalent circuit of Figure 9 and the values for the circuit elements in Table 1. Full lines are for maximum available gain MAG, if the stability factor $k > 1$. Broken lines are for maximum stable gain MSG, if $k < 1$. Three assumptions about the extrinsic elements have been made. Key: 1) Full equivalent circuit. 2) No gate-metallization resistance, no gate-pad parasitics ($R_g = C_L = R_L = 0$). 3) Intrinsic transistor only ($R_g = C_L = R_L = R_s = 0$).

The measured points are in good agreement with the computed curve 1 at higher frequencies. The deviations at lower frequencies are mainly due to the oversimplified representation of the gate pads in the equivalent circuit. Owing to this the computed results show a potential unstable region between about 1 GHz and 3 GHz, whereas the measured transistor is stable in the whole range. However, as already mentioned, the measured k has its minimum, which is close to 1, in that frequency range. In the region above about 4 GHz, as mentioned earlier, pad losses have not much influence, therefore one would expect, according to (C8c) that MAG should show a 6 dB drop per octave. This is not quite what was found; the measured as well as computed results have rather a 4 dB drop per octave. This deficiency of the approximate equation is mostly caused by neglected higher-order terms in ω. However, (C8d) for the maximum frequency of oscillation f_{max} is still in reasonable agreement with the measured value of about 9 GHz, also found by the computer cal-

$$f_{max} = \frac{1}{2\pi}\frac{g_{m0}}{\left[G_d\left\{4C_{sg}(\tau_i + \tau_s + \tau_g) + 2C_{dg}\left[\frac{C_{dg}}{G_d} + \frac{g_{m0}}{G_d}(\tau_i + \tau_s + 2\tau_g)\right]\right\}\right]^{1/2}}$$

direct input losses — input losses caused by feedback

culation. This formula gives a good insight into the factors determining the frequency-limit of the device. In a slightly modified form (C8d) is given above.

The meaning of the time constants and of the other quantities is given in Fig. 9 and in (C5a). In general, the frequency limit of a transistor depends on the transconductance and the losses at input and output. As pointed out earlier, the magnitude of the transconductance of our transistors in their useful frequency range is nearly independent of frequency, leading to the constant factor g_{m0} in the numerator of the approximate formula. Also the drain-conductance G_d as the main source of output loss does not depend much on frequency. G_d is represented as a factor before the curly bracket. Only the input losses, given by the seven terms in the curly bracket, vary with frequency. They therefore lead to the gain variation with frequency. The first three terms in the curly bracket are losses caused by the resistors R_i, R_s and R_g in conjunction with the gate-capacitance C_{sg}. The remaining four terms are losses due to feedback. Part of them as the dc-open-circuit voltage gain g_{m0}/G_d as a factor indicates, is enhanced by some sort of Miller effect.

In our present transistors the time constants are similar; also by chance the other quantities are such that the direct losses and those caused by feedback are roughly equal. The time-constants τ_g and τ_s due to the resistors R_g and R_s are of considerable influence on f_{max}, because they occur twice in the square bracket.

This also becomes evident from the computed curve 2 where the gate-metallization resistance R_g and the gate-pad parasitics C_L and R_L are assumed to be absent. The gain improves considerably and f_{max} goes up to 19 GHz. That a decrease in R_g improves f_{max} is also in agreement with experiments. Our best transistor with an f_{max} of 12 GHz had a gate-width of 300 μm, which reduced R_g compared to our usual devices with 400 μm gate-width. The approximate formulas for MAG and f_{max} are not in good agreement with the exact, computed results of curve 2 (and also curve 3). The neglected higher-order terms in ω are of more influence here, and the condition $k \gtrsim 2$ for the validity of (C8d) is no longer fulfilled. The decreased losses increase the potentially unstable region which now extends to about 8 GHz. Because the gate-pad losses are set to zero, the stable region at low frequencies disappears and the gain goes up there. The computed maximum stable gain MSG is in good agreement with the approximate equation (C6).

Curve 3, where in addition the source-gate series resistance is omitted, shows a further improvement in gain and f_{max} increases to about 35 GHz. The latter figure, as well as the computed gain above about 20 GHz, is perhaps not precise, because the simple equivalent circuit for the intrinsic transistor is expected to lose its validity at these frequencies.

To summarize, one of the main results of the calculations is that the extrinsic elements still have a considerable influence on the power gain of the present devices.

Conclusions

This investigation shows that the operating range of field-effect transistors can be extended far into the microwave region. The Schottky-barrier FET technology is capable of providing transistors with an f_{max} of 12 GHz, which is at least as good as the best bipolar transistors of today. Another important result of the microwave investigations is that further improvements are possible with perhaps little additional technological effort. Only some of the parasitic elements in the transistors have to be reduced. The gate-pad parasitics could be considerably decreased if, for instance, the pads were placed on oxide and not on the epitaxial n-layer. Reduction of the gate-metallization resistance could be achieved either by better electroplating techniques or by using shorter gates. These relatively simple measures might increase f_{max} of the 1-micrometer Si Schottky-barrier FET to 19 GHz. Other improvements, for instance, a further decrease of the gate-length, seem feasible.

Recently, noise measurements were carried out on these devices.[24] The optimum noise figures, for instance $F_0 \approx 5$ dB at 4 GHz, are encouragingly low.

Another attractive possibility for Schottky-barrier FET's is to use GaAs as a material instead of Si. The feasibility has already been demonstrated by various laboratories.[2-4] We have carried out computations, which indicate that the gain and f_{max} should be about a factor of two better than for Si-devices mainly because of the higher drift velocity and mobility in GaAs.[25]

In conclusion it can be stated that Schottky-barrier FET's hold great promise for applications in the microwave range up to the X-band and perhaps above.

Acknowledgments

I am indebted to S. Middelhoek, who was responsible for the design and the fabrication of the transistors used in

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Appendix A: Small-signal parameters in the drift saturated region

The influence of the drift saturation on the small-signal parameters will be treated here in an approximate way. For simplicity it will be assumed that the drift velocity for fields $0 \leq E < E_S$ goes linear with E and then for $E > E_S$ saturates abruptly at a velocity v_S (Fig. 13a) which for Si is about 10^7 cm/sec (Ref. 20). Though the quoted value of v_S was found for lightly doped Si it is expected to be valid for our high doping of about 10^{17} cm^{-3} because the scattering processes leading to drift saturation (for instance optical-phonon emission) should depend mainly on the kinetic energy of the electrons but scarcely on doping. However, with high doping, because of the decreased mobility the critical kinetic energy should be reached at higher fields, in our case $E_S \approx 15$ to 20 kV/cm. If in a transistor the drain voltage is increased, then at a certain critical drain voltage the field E_S is reached in the narrowest point of the channel at the drain end of the gate. It is plausible that a further increase in drain voltage cannot increase the current substantially because the electrons move already with their highest velocity near the drain. An investigation revealed that a dipole layer of charges forms in the channel at the drain end.[21] This layer absorbs nearly all of the drain voltage in excess of the critical voltage, therefore the current saturates. Recent two-dimensional computer solutions of the FET problem confirmed this picture.[26,30]

In order to get a tractable model, simplifications are necessary. It is assumed that as soon as the saturation field E_S is reached, the channel is completely decoupled from the drain electrode. Therefore if the drain voltage is increased above its critical value, the field in the channel remains at E_S at the drain end and the current stays constant. With these assumptions parameters y_{22} and y_{12} are set to zero, a drawback which is shared with the conventional theories in current saturation. Due to the assumptions the whole channel below the gate is in the ohmic region. If in addition it is required that the conditions for the gradual case[1] hold, then the only modification compared to the usual theories is the boundary condition $E = E_S$ in the channel at the drain. It is started with the usual equations for the current in the channel (see Fig. 13b),

$$I = \sigma(a - y)E_x \tag{A1a}$$

the conservation of charge

$$\frac{\partial I}{\partial x} = -eN\frac{\partial y}{\partial t} \tag{A1b}$$

the voltage drop in the depletion layer

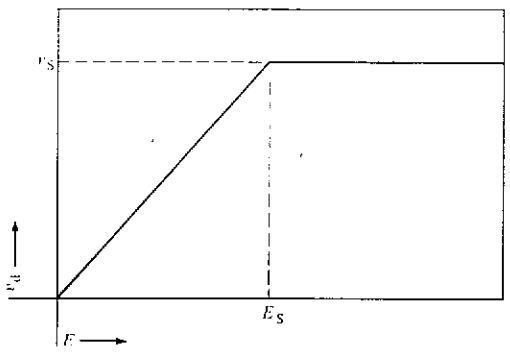
$$V_{cg} = -\tfrac{1}{2}W_0\frac{y^2}{a^2} \tag{A1c}$$

with the pinch-off voltage

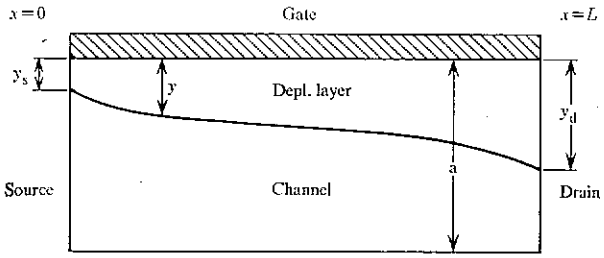
$$W_0 = \frac{1}{2}\frac{eN_D}{\varepsilon\varepsilon_0}a^2 \tag{A1d}$$

and the field in the channel

$$E_x = -\frac{W_0}{a^2}\frac{\partial y^2}{\partial x}. \tag{A1e}$$



(a)



(b)

Figure 13 Simplified drift-velocity characteristics a), and the geometry of the transistor b), as used for the theoretical investigation.

The usual small signal approach is made by assuming that the quantities I, y^2, V_{cg} and E_x are composed of a stationary part with index 0, and a small ac-part with index w and time-dependence $e^{j\omega t}$. For instance, $y^2 = y_0^2 + y_w^2 e^{j\omega t}$.

a) Stationary solution

Because of $\partial I_0/\partial x = 0$ we get from (A1a) and A1e)

$$I_0 = -\frac{W_0}{a^2}\sigma(a - y_0)\frac{\partial y_0^2}{dx}. \tag{A2a}$$

After an integration the usual result for the dc-current is obtained,

$$I_0 = -\frac{W_0}{3R_0}\left[3\left(\frac{y^2}{a}\right) - 2\left(\frac{y}{a}\right)^3\right]_{y_{s0}/a}^{y_{d0}/a} \tag{A2b}$$

with the resistance of the open channel

$$R_0 = \frac{L}{\sigma a}. \tag{A2c}$$

To simplify later calculations it is convenient to introduce the relative channel height difference z,

$$z = \frac{y_0 - y_{s0}}{a - y_{s0}} \tag{A3a}$$

at the source

$$y_0 = y_{s0} : z = 0$$

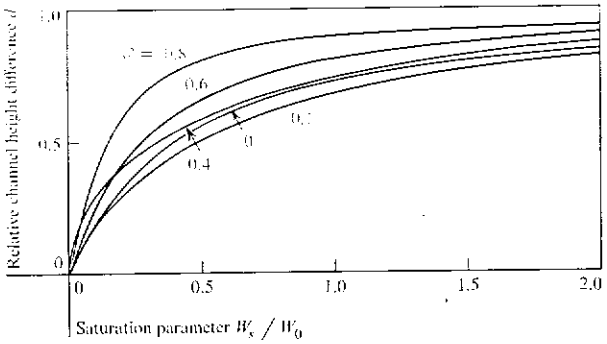


Figure 14 Relative channel height difference d as a function of the saturation parameter W_S/W_0 with the normalized gate-bias $s^2 = -V_{sg,0}/W_0$ as a parameter.

at the drain

$$y_0 = y_{d0} : z = \frac{y_{d0} - y_{s0}}{a - y_{s0}} \equiv d.$$

Here, the value of z at the drain has been named d. In addition we introduce the relative depletion layer thickness s at the source,

$$s = \frac{y_{s0}}{a} = \sqrt{-\frac{V_{sg,0}}{W_0}}, \tag{A3b}$$

with $V_{sg,0}$ as the source-gate bias voltage. This gives

$$I_0 = -\frac{W_0}{3R_0}\, i_0 \tag{A3c}$$

with the normalized current

$$i_0 = (1 - s)^2 \cdot d \cdot [6s + 3(1 - 2s)\, d - 2(1 - s)\, d^2]. \tag{A3d}$$

As explained earlier the drain depletion depth y_d is no longer determined by the drain voltage but by the requirement that at the drain the field in the channel be E_s, which leads to a condition for the drain current

$$I_0 = -\sigma\, |E_S|\, (a - y_{d0}) \tag{A4a}$$

$$= -\frac{W_S}{R_0}(1 - s)(1 - d)$$

with the "saturation voltage"

$$W_S = |E_S| \cdot L. \tag{A4b}$$

By combining equations (A2c) and (A4a) the current I_0 can be eliminated:

$$\frac{W_S}{W_0} = \frac{d}{3(1 - d)}(1 - s) \cdot [6s + 3(1 - 2s)\, d - 2(1 - s)\, d^2]. \tag{A5}$$

This is a relation between the saturation parameter W_S/W_0, the channel height parameter d at the drain and the relative depletion layer thickness s at the source. A plot of d versus W_S/W_0 with the relative gate voltage s^2 as a parameter is shown in Fig. 14. If drift saturation plays no role ($W_S/W_0 \to \infty$), then $d \to 1$, or $y_{d0} \to a$, which means that the Shockley condition for pinch-off is recovered. The more important drift saturation becomes, which means small W_S/W_0, the more open is the channel at the drain at the outset of current saturation.

b) Small signal solution

From equations (A1a-A1e) a differential equation for the small signal depletion layer motion is obtained:

$$\frac{\partial^2}{\partial x^2}[(a - y_0) y_w^2] = j\omega R_0 C_0 \left(\frac{a}{L}\right)^2 \frac{y_w^2}{y_0}. \tag{A6a}$$

with the characteristic capacitance

$$C_0 = \frac{\varepsilon\varepsilon_0 L}{a} \tag{A6b}$$

This is the standard junction FET small signal equation, which in different notation, for instance, can be found in Ref. 27.

Now z is introduced. If in addition it is considered that from Eqs. (A2a) and (A2b)

$$\partial x = \frac{6L}{i_0}(1 - s)^2(1 - z)[s + (1 - s)z]\, \partial z \tag{A6c}$$

then it is found

$$\frac{\partial}{\partial z}\left\{\frac{1}{(1 - z)[s + (1 - s)z]}\frac{\partial}{\partial z}[(1 - z)\, V]\right\} = \alpha(1 - z)\, V. \tag{A6d}$$

The following abbreviations were introduced:

$$\alpha = j\omega \frac{36(1 - s)^3 R_0 \cdot C_0}{i_0^2} \tag{A6e}$$

$$V = \frac{y_w^2}{a^2}. \tag{A6f}$$

The latter is the relative ac-voltage drop in the depletion layer and is related to the absolute ac voltage drop $V_{cg,w}$:

$$V_{cg,w} = -W_0 \cdot V. \tag{A6g}$$

In principle, Eq. (A6c) can be solved exactly with parabolic cylinder functions as a solution for V (Ref. 28). However, because it suffices for our purposes to know the result to low orders of ω, an iterative method for the solution is preferred.[27] We set

$$V = V_1 + \alpha V_2 + \alpha^2 V_3 + \cdots. \tag{A7a}$$

Inserting (A7a) into (A6d) gives

$$\frac{\partial}{\partial z}\left\{\frac{1}{(1 - z)[s + (1 - s)z]}\frac{\partial}{\partial z}[(1 - z)\, V_{n+1}]\right\} = (1 - z)\, V_n \tag{A7b}$$

with the starting condition $V_0 = 0$. It is quite easy though tedious to obtain $(1 - z)\, V_n$ for every desired n by straightforward integration. The lowest order is, for instance,

$$(1 - z)\, V_1 = \left[sz + (1 - 2s)\frac{z^2}{2} - (1 - s)\frac{z^3}{3}\right] \cdot C_1 \cdot V_g + C_2 \cdot V_g. \tag{A8}$$

Here $C_1 \cdot V_g$ and $C_2 \cdot V_g$ are constants of integration which have to be determined by the boundary conditions at source and drain.

At the source it is required that the ac-voltage drop is equal to the externally applied ac source-gate voltage $V_{sg,w}$:

$$x = 0, \qquad z = 0 : V = V_g \equiv -\frac{V_{sg,w}}{W_0} \tag{A9a}$$

or for the iterative solution

$$V_1 = V_g; \qquad 0 = V_2 = V_3 = \cdots . \tag{A9b}$$

At the drain it is required that the field $E_x = E_s$ be constant. Hence for

$$x = L, \qquad z = d : E_{xw} = 0$$

or

$$0 = E_{xw} = -\frac{W_0}{a^2}\frac{\partial y_w^2}{\partial x} \tag{A9c}$$

which leads to

$$\frac{\partial V}{\partial z} = 0$$

or for the iterative solution

$$0 = \frac{\partial V_1}{\partial z} = \frac{\partial V_2}{\partial z} = \frac{\partial V_3}{\partial z} = \cdots . \tag{A9d}$$

This is an open-circuit condition for the ac voltage drop in the depletion layer at the drain end.

For the ac-current in the channel from (A2a) is found

$$I_w = -\frac{W_0}{R_0}\frac{L}{a^3}\frac{\partial}{\partial x}[(a - y_0)y_w^2]. \tag{A10a}$$

With all abbreviations introduced,

$$I_w = -\frac{W_0}{R_0}\frac{i_0}{6(1-s)(1-z)[s + (1-s)z]} \cdot \frac{\partial}{\partial z}[(1-z)V]. \tag{A10b}$$

After straightforward integrations up to order α^2 the following results are obtained:

$$\frac{I_w}{V_{sg,w}} = -\frac{1}{R_0} \cdot \frac{i_0}{6(1-s)}\left[C_1 + \alpha\left\{\left[s + (1-2s)\frac{z}{3} - (1-s)\frac{z^2}{6}\right] \cdot \frac{z^2 \cdot C_1}{2} + C_2 z + C_3\right\} + \alpha^2\left\{\left[\frac{s^2}{4} + s(1-2s)\frac{z}{5} + (2(1-2s)^2 - 7s(1-s)) \cdot \frac{z^2}{60} - (1-s)(1-2s)\frac{z^3}{28} + (1-s)^2\frac{z^4}{112}\right] \cdot \frac{z^4 \cdot C_1}{6} + \left[\frac{s}{3} + (1-2s)\frac{z}{6} - (1-s)\frac{z^2}{10}\right] \cdot \frac{z^3 \cdot C_2}{2} + \left[s + (1-2s)\frac{z}{3} - (1-s)\frac{z^2}{6}\right] \cdot \frac{z^2 \cdot C_3}{2} + C_5\right\}\right]. \tag{A11a}$$

The following is found for the constants:

$$C_1 = -\frac{6(1-s)^2}{i_0 + 6(1-s)^2(1-d)^2[s + (1-s)d]} \tag{A11b}$$

$$C_2 = 1 \tag{A11c}$$

$$C_3 = C_1\Big\{(1-d)^2[s + (1-s)d] \cdot \left[s + (1-2s)\frac{d}{3} - (1-s)\frac{d^2}{6}\right] \cdot \frac{d^2 \cdot C_1}{2} + \left[s^2 + s(1-2s)d + (2(1-2s)^2 - 7s(1-s))\frac{d^2}{10} - (1-s)(1-2s)\frac{d^3}{4} + (1-s)^2\frac{d^4}{14}\right] \cdot \frac{d^3 \cdot C_1}{6} + (1-d)^2 d[s + (1-s)d] + \left[\frac{s}{2} + (1-2s)\frac{d}{3} - (1-s)\frac{d^2}{4}\right] d^2\Big\}. \tag{A11d}$$

C_5 has not been determined. From the channel current the y-parameters can be obtained, which are of the following form

$$y_{11} = \frac{-(I_w)_{z=d} + (I_w)_{z=0}}{V_{sg,w}} = j\omega C_{sg} + \omega^2 C_{sg} \cdot \tau_i \tag{A12a}$$

$$y_{21} = \frac{(I_w)_{z=d}}{V_{sg,w}} = g_{m0} - j\omega g_{m0} \cdot \tau_t . \tag{A12b}$$

Not all values will be given, except g_{m0}. It is found

$$g_{m0} = -\frac{1}{R_0}\frac{i_0}{6(1-s)}C_1 \tag{A12c}$$

$$= \frac{1-s}{R_0}\frac{1}{1 + \dfrac{6(1-s)^2(1-d)^2[s + (1-s)d]}{i_0}}. \tag{A12d}$$

This is essentially Shockley's value for g_{m0} multiplied with a degradation factor. If drift saturation is not important, hence $d = 1$, the degradation factor is unity and Shockley's result is recovered. With increasing influence of the drift saturation, d goes to zero and also g_{m0} approaches zero. In Fig. 15, g_{m0} is plotted as a function of the saturation parameter W_s/W_0. This result was obtained by taking d from Fig. 14 and inserting it into Eq. (A12d). For the other three circuit elements C_{sg}, τ_i and τ_t, only the values in the limits of no drift saturation ($d = 1$) and strong drift saturation ($d = 0$) will be given.

No drift saturation ($d = 1$):

$$g_{m0} = \frac{1}{R_0}(1-s)$$

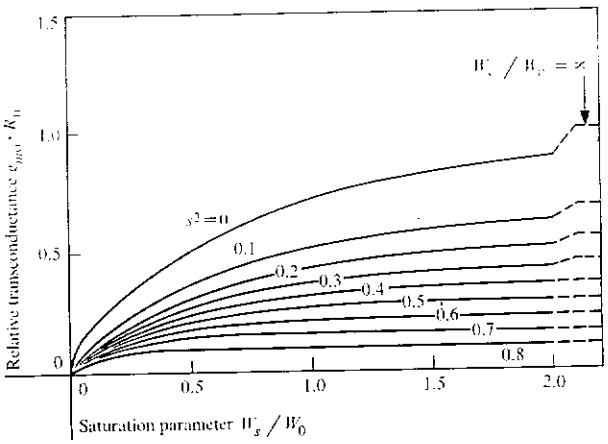
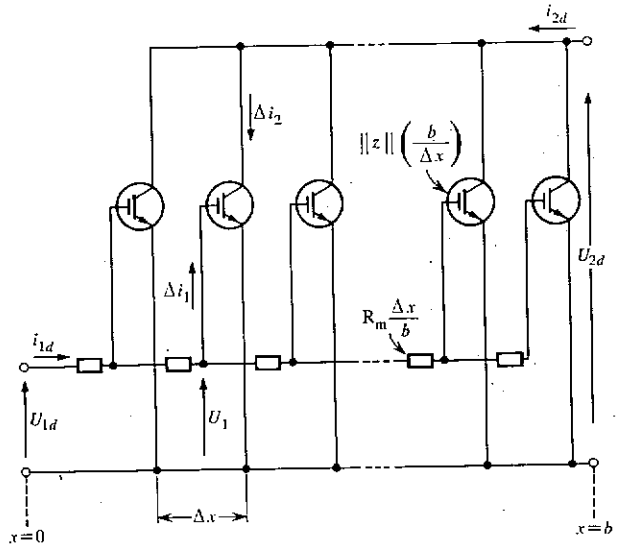


Figure 15 Normalized transconductance $g_{m0} \cdot R_0$ as a function of the saturation parameter W_s/W_0 with the normalized gate-bias $s^2 = -V_{sg,0}/W_0$ as a parameter.

Figure 16 Equivalent circuit of the gate transmission line. R_m is the metallization resistance which is distributed along the gate with width b.



$$C_{sg} = C_0 \frac{3(1+s)}{(1+2s)^2}$$

$$\tau_t = R_0 C_0 \frac{9}{35} \frac{3 + 15s + 10s^2}{(1-s)(1+2s)^3}$$

$$\tau_i = R_0 C_0 \frac{3}{70} \frac{7 + 56s + 75s^2 + 30s^3}{(1-s)(1+s)(1+2s)^2}.$$

Strong drift saturation ($d = 0$):

$$g_{m0} = 0$$

$$C_{sg} = C_0 \frac{1}{s}$$

$$\tau_t = R_0 C_0 \frac{(1-s)}{2s}$$

$$\tau_i = R_0 C_0 \frac{(1-s)}{3s}.$$

As follows from these formulas the only quantity strongly varying with d is the transconductance. The other quantities vary for a given and not too small s ($s \gtrsim 0.1$) by about a factor of 2. The circuit elements for negligible drift saturation ($d = 1$) are in agreement with values in the literature.[27]

Appendix B: The influence of the distributed resistance of the gate metallization

Because the resistance of the gate metallization is distributed, the gate has to be considered as a transmission line, a schematic drawing of which is shown in Fig. 16. It is assumed that connections to the gate are made at the left end, whereas the right end is open-circuited. The metallization resistance measured from one end to the other is R_m and the gate-width is b. At source and drain the metallization resistance is so low that the transmission-line character can be neglected there. The z-parameters are used because it turns out that the results are simplest with them. For a piece dx of the transmission line, the following differential equations can be derived from Fig. 16:

$$U_1 = -bz_{11} \frac{di_1}{dx} + bz_{12} \frac{di_2}{dx} \tag{B1a}$$

$$\frac{dU_1}{dx} = -\frac{R_m}{b}(i_{1d} - i_1) \tag{B1b}$$

$$U_2 = bz_{21} \frac{di_1}{dx} + bz_{22} \frac{di_2}{dx} \tag{B1c}$$

$$U_2 = U_{2d} = \text{const.} \tag{B1d}$$

Here i_1 is the current to the gates, counted from $x = 0$ the current in the gate line is $i_{1d} - i_1$.

From (B1a) with the aid of (B1b) and (B1c) U_1 and i_2 can be eliminated:

$$-\frac{d^2 i_1}{dx^2} = (i_{1d} - i_1) \frac{R_m}{b^2} \frac{z_{22}}{z_{11}z_{22} - z_{12}z_{21}}$$

$$= (i_{1d} - i_1) \frac{R_m y_{11}}{b^2}.$$

The solution for i_1 is, after the boundary condition $i_1 = 0$ at $x = 0$ and $i_1 = i_{1d}$ at $x = b$ have been taken into account,

$$i_1 = i_{1d}[1 - \cosh(kx) + \coth(kb) \cdot \sinh(kx)] \tag{B2a}$$

with the equation for the propagation constant k

$$k^2 b^2 = R_m \cdot y_{11}. \tag{B2b}$$

For U_1 it is found, if (B2a) is inserted in (B1a) and (B1c),

$$U_1 = i_{1d} \frac{kb}{y_{11}} [\coth(kb) \cosh(kx) - \sinh(kx)] + \frac{z_{12}}{z_{22}} U_2. \tag{B2c}$$

In a similar way for i_2 one gets, if (B2a) is inserted into (B2c) and the boundary condition $i_2 = 0$ at $x = 0$ is used,

$$i_2 = \frac{U_2 x}{b z_{22}} + \frac{z_{21}}{z_{22}}\, i_{1d}[\cosh(kx) - 1 - \coth(kb)\cdot\sinh(kx)]. \tag{B3}$$

At $x = b$, $i_2 = i_{2d}$, therefore, from (B3),

$$U_{2d} = z_{21} i_{1d} + z_{22} i_{2d}. \tag{B4a}$$

This equation means that in the distributed system the parameters z_{21} and z_{22} are unchanged. Now the value of U_2 can be inserted into (B2c). If the boundary condition $U_1 = U_{1d}$ is considered at $x = 0$ one finds

$$U_{1d} = i_{1d}\frac{kb}{y_{11}}\left[\coth(kb) + \frac{z_{12}z_{21}}{z_{22}}\right] + z_{12} i_{2d}. \tag{B4b}$$

From this equation it follows that the value of z_{12} remains unaltered, however, the open-circuit input impedance z_{11d} of the distributed system is changed,

$$z_{11d} = \frac{kb}{y_{11}}\coth(kb) + \frac{z_{12}z_{21}}{z_{22}}. \tag{B5a}$$

In the whole operating frequency range of our transistors, $|y_{11}| \ll 1/R_m$ holds, therefore an expansion of coth (kb) is possible. The first two series terms yield

$$z_{11d} = z_{11} + \frac{R_m}{3} + \cdots. \tag{B5b}$$

Accordingly, the distributed gate-metallization resistance behaves approximately as if a resistor $R_g = R_m/3$ were connected to the input of the transistor proper.

The resistance R_m is proportional to the gate-width b, whereas z_{11} is proportional to $1/b$. Therefore, the ratio R_m/z_{11} which is a measure of the influence of R_m goes like b^2. This means that a decrease in gate-width leads to a rapid decrease of the influence of the gate-metallization resistance.

Appendix C: Approximate equations for the *y*-parameters and the power gain

In this Appendix approximate expressions are derived for the *y*-parameters, the maximum stable gain MSG, the maximum available gain MAG, the unilateral gain U and the stability factor k from the equivalent circuit of Fig. 9. As follows from this figure and Appendix A, the *y*-parameters of the intrinsic transistor are approximately

$$y_{11i} = j\omega(C_{sg} + C_{dg}) + \omega^2 C_{sg}\cdot\tau_i \tag{C1a}$$

$$y_{12i} = -j\omega C_{dg} \tag{C1b}$$

$$y_{21i} = g_{m0} - j\omega(g_{m0}\tau_i + C_{dg}) \tag{C1c}$$

$$y_{22i} = G_d + j\omega C_{dg}. \tag{C1d}$$

Now the source-gate series resistance R_s and the effective gate-metallization resistance R_g will be incorporated. This is best done by converting the matrix $||y_i||$ of the intrinsic transistor to the impedance matrix $||z_i||$. As follows from Appendix B and the literature[29] the *z*-matrix of the combination is given by adding R_g and R_s to $||z_i||$,

$$||z|| = ||z_i|| + R_s\begin{Vmatrix}1 & 1\\ 1 & 1\end{Vmatrix} + R_g\begin{Vmatrix}1 & 0\\ 0 & 0\end{Vmatrix}. \tag{C2a}$$

This *z*-matrix is back-transformed to the *y*-matrix. The result is

$$||y|| = \frac{||y_i|| + R_s\,\Delta y_i\begin{Vmatrix}1 & -1\\ -1 & 1\end{Vmatrix} + R_g\,\Delta y_i\begin{Vmatrix}0 & 0\\ 0 & 1\end{Vmatrix}}{1 + R_s\,\Sigma y_i + R_g(y_{11i} + R_s\,\Delta y_i)} \tag{C2b}$$

with

$$\Delta y_i = y_{11i}\cdot y_{22i} - y_{12i}\cdot y_{21i} \tag{C2c}$$

$$\Sigma y_i = y_{11i} + y_{12i} + y_{21i} + y_{22i}. \tag{C2d}$$

With the values in Table 1 it can be shown that for our transistors the term $R_s\Delta y_i$ in the bracket in the denominator is small compared to y_{11i}, hence it will be neglected. In a next step the numerator and denominator of (C2b) are divided by the feedback factor

$$1 + R_s(g_{m0} + G_d) \approx 1 + R_s g_{m0}. \tag{C3a}$$

With the abbreviations

$$x^* = \frac{x}{1 + R_s(g_{m0} + G_d)} \tag{C3b}$$

and

$$R_s\Sigma' y_i = R_s\Sigma y_i - R_s(g_{m0} + G_d) \tag{C3c}$$

one obtains

$$||y|| = \frac{||y_i^*|| + R_s\Delta^* y_i\begin{Vmatrix}1 & -1\\ -1 & 1\end{Vmatrix} + R_g\Delta^* y_i\begin{Vmatrix}0 & 0\\ 0 & 1\end{Vmatrix}}{1 + R_s\Sigma' y_i^* + R_g y_{11i}^*}. \tag{C3d}$$

For our transistors the two terms containing R_s and R_g in the numerator are small compared to 1, moreover the second and the third terms in the denominator are small compared to $||y_i^*||$. Therefore an expansion is made which to lowest order yields

$$\begin{aligned}||y|| \approx\ & ||y_i^*|| \\ & + R_s\left[\Delta^* y_i\begin{Vmatrix}1 & -1\\ -1 & 1\end{Vmatrix} - \Sigma' y_i^*\,||y_i^*||\right] \\ & + R_g\left[\Delta^* y_i\begin{Vmatrix}0 & 0\\ 0 & 1\end{Vmatrix} - R_g y_{11i}^*\,||y_i^*||\right].\end{aligned} \tag{C4}$$

Equations (Cla-d) can now be inserted into (C4). Because of $R_s G_d \ll 1$, $C_{dg} \ll C_{sg}$ and $R_s g_{m0} \ll 1$, some of the smaller terms at least in higher-order expressions can be neglected. The gate-pad admittance $y_L(\omega)$ and the source-drain capacitance C_{sd} are now incorporated. If the following time-constants are introduced,

$$\tau_i = R_i\cdot C_{sg} \qquad \tau_s = R_s C_{sg} \qquad \tau_g = R_g C_{sg}, \tag{C5a}$$

then

$$y_{11} \approx j\omega(C_{sg}^* + C_{dg}) + \omega^2 C_{sg}^*(\tau_i + \tau_s^* + \tau_g^*) + y_L(\omega) \tag{C5b}$$

$$y_{12} \approx -j\omega C_{dg} - \omega^2 C_{sg}^*\tau_g^* \tag{C5c}$$

$$y_{21} \approx g_{m0}^* - j\omega[C_{dg} + g_{m0}^*(\tau_i + \tau_s^* + \tau_g^*)] \tag{C5d}$$

$$y_{22} \approx G_d^* + j\omega(C_{dg} + C_{sd}). \tag{C5e}$$

Only two orders in ω have been taken into account in each of the y-parameters. It is evident that the extrinsic elements R_s and R_g add to the input loss and to the phase-shift of y_{21}.

As the first gain-parameter, the maximum stable gain is calculated.[15] To lowest order in ω,

$$\mathrm{MSG} = \left|\frac{y_{21}}{y_{12}}\right| \approx \frac{g_{m0}^*}{\omega C_{dg}} \qquad (k \leq 1) \tag{C6}$$

is obtained.

The stability factor k is given by[18]

$$k = \frac{2\ \mathrm{Re}\ y_{11} \cdot \mathrm{Re}\ y_{22} - \mathrm{Re}\ (y_{12} \cdot y_{21})}{|y_{12}| \cdot |y_{21}|}. \tag{C7a}$$

Only a rough approximation will be derived. To this end, the gate-pad admittance $y_L(\omega)$ is replaced by $1/R_L$ which is valid above approximately 1 GHz. Moreover, the feedback-factor $1 + R_s(g_{m0} + G_d)$ is neglected, which is a reasonable approximation because this factor is only slightly larger than one, and as a more accurate investigation revealed drop-outs in many terms anyway. In addition $|y_{21}|$ is approximated by g_{m0}. If only the lowest order of ω is considered

$$k = \frac{2G_d}{\omega R_L C_{dg} g_{m0}} + \omega \frac{2C_{sg}G_d(\tau_i + \tau_s + \tau_g) + C_{dg}[C_{dg} + g_{m0}(\tau_i + \tau_s + 2\tau_g)]}{C_{dg} g_{m0}}$$

$$= \frac{k_1}{\omega} + \omega k_2. \tag{C7b}$$

For simplicity the maximum available gain MAG will be calculated only near the frequency limit of the transistor. We have[18]

$$\mathrm{MAG} = \left|\frac{y_{21}}{y_{12}}\right| \frac{1}{k + \sqrt{k^2 - 1}}. \tag{C8a}$$

If $k \gtrsim 2$ which holds at sufficiently high frequencies,

$$\mathrm{MAG} \approx \left|\frac{y_{21}}{y_{12}}\right| \frac{1}{2k} \qquad (k \gtrsim 2) \tag{C8b}$$

is obtained. At high frequencies, the gate-pad losses are not of much influence, hence they will be neglected. If only the lowest order in ω is taken into account,

$$\mathrm{MAG} \approx \left(\frac{\omega_{max}}{\omega}\right)^2 \tag{C8c}$$

with

$$\omega_{max} \approx g_{m0} / \{4C_{sg}G_d(\tau_i + \tau_s + \tau_g) + 2C_{dg}[C_{dg} + g_{m0}(\tau_i + \tau_s + 2\tau_g)]\}^{1/2}. \tag{C8d}$$

The unilateral gain U is given by[17]

$$U = \frac{|y_{21} - y_{12}|^2}{4(\mathrm{Re}\ y_{11} \cdot \mathrm{Re}\ y_{22} - \mathrm{Re}\ y_{12} \cdot \mathrm{Re}\ y_{21})}. \tag{C9a}$$

If the same assumptions are made as for MAG, one obtains

$$U \approx \left(\frac{\omega_u}{\omega}\right)^2 \tag{C9b}$$

with

$$\omega_u = \frac{g_{m0}}{[4C_{sg}G_d(\tau_i + \tau_s + \tau_g) + 4C_{dg}g_{m0}\tau_g]^{1/2}}. \tag{C9c}$$

As follows from these equations MSG has a 3 dB drop per octave, whereas MAG and U show a 6 dB drop. MAG and U have unity gain at the maximum frequencies of oscillation ω_{max} and ω_u. The frequency ω_u is slightly larger than ω_{max}. If the extrinsic elements R_s and R_g are set to zero, then the unilateral gain U reduces to an expression which has already been given in the literature.[22] As is clear from the derivation, many approximations have been made, therefore one cannot expect these formulas to be accurate, but because all the important elements of the equivalent circuit are incorporated, these equations are quite helpful in transistor design. With appropriate changes they should also be valid for other types of FET's.

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