Materials Science Forum Vols. 556-557 (2007) pp 895-900
online at http://www.scientific.net

Progress on the Development of 10 kV 4H-SiC PiN Diodes for High Current/High Voltage Power Handling Applications

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Keywords: PiN diode, bipolar power device, V_F drift, reverse recovery.

Abstract. The development of 4H-SiC PiN diodes capable of blocking to greater than 10 kV while having current ratings of 20 A at 100 A/cm^2 is continuing in earnest. V_F instability of these diodes continues to be a roadblock, but progress is being made, and a 20 A/10 kV 4H-SiC PiN diode wafer with an overall device yield of 40% has been fabricated. The latest device characteristics are discussed, along with details of approaches in improving the reverse recovery characteristics of these diodes to satisfy the requirements needed for implementation into high voltage inverter modules capable of switching at up to 20 kHz.

Introduction

Progress continues on the development of a commercially viable process for the manufacture of 4H-SiC PiN diodes capable of blocking in excess of 10 kV with forward current ratings of 20 A at a forward voltage (V_F) of less than 4.25 V at room temperature. In particular, large gains have been made in eliminating V_F drift (the irreversible increase in V_F that can occur with time during forward current injection), but not without compromising the reverse blocking characteristics of the diodes [1,2]. Basal plane dislocations (BPD) present in the active layers of PiN diodes have been shown to nucleate stacking faults (SF) during bipolar forward current injection, which then attenuate current flow through the faulted areas and cause V_F drift [3]. We are continuing to refine epitaxial growth techniques that reduce the density of BPDs that propagate from the substrate into the epitaxial layers during growth, thus providing V_F stability, while not compromising reverse blocking yields. In this study, we report on the latest 20 A/10 kV 4H-SiC PiN diodes that have been manufactured employing the latest refinements in BPD reduction epitaxial growth processes and optimized device fabrication technology to achieve the best combination of forward voltage, reverse blocking, and V_F drift yields. We also describe details of approaches to decrease the stored charge during diode reverse recovery so that they can be implemented with 4H-SiC DMOSFETs in high voltage, high frequency inverters capable of switching at frequencies up to 20 kHz.

Device Fabrication and Testing

The first step in 4H-SiC PiN diode fabrication consists of growing device epitaxial layers on n-type 4H-SiC substrates. The substrates employed in these devices were high quality 3 inch N-doped 4H-SiC substrates with micropipe densities of less than 2 micropipes/cm^2 that were cut at an 8° incline to the [0001] crystal plane. In order to promote the turning of substrate BPDs into threading edge dislocations (which are benign with respect to V_F drift) during epitaxy, the substrate surfaces were subjected to one of two different etch processes prior to epitaxy [4]. In the first method, the substrates were etched in a molten KOH bath to selectively etch BPDs that intersect the substrate surface. Due to the geometry of the BPD etch pits, during the early stages of epitaxial growth, the BPDs are forced to turn into threading edge dislocations (TEDs). After growing several μm of n^+ 4H-SiC on the etched substrate surface, this semi-sacrificial BPD conversion epitaxial layer was

polished smooth for subsequent device epitaxy, being sure not to polish through the original epitaxy/substrate interface. Alternatively, in the second method of BPD to TED conversion, rather than selectively etching in a KOH bath, a hexagonal pattern was etched into the substrate surface with a reactive ion etch. During the early stages of epitaxy, 4H-SiC growth on the sidewalls of the hexagonal template forces any BPD that would otherwise continue to extend along the basal plane to turn into a TED.

Following substrate preparation, device layers consisting of an n^+ buffer layer, a thick n^- drift layer, and a thin p^+ injection layer were grown in a single epitaxial growth run. The n^- drift layers were doped 2 x 10^{14} cm^{-3} with nitrogen, and layers from 100 to 130 μm thick were investigated. Doping of the p^+ injection layers ranged from 1 x 10^{17} cm^{-3} to 8 x 10^{18} cm^{-3} so that the effects of forward charge injection on the reverse recovery characteristics of the diodes could be examined. A reactive ion etch down into the n^- drift layer was employed to isolate individual diodes on wafer. The mesas measured 4.51 mm x 4.51 mm for an active area of 0.2 cm^2, which is designed for 20 A forward current at 100 A/cm^2. The diodes were terminated with either an aluminum-implanted guard ring termination or a boron-implanted multi-zone junction termination extension (JTE), and a nitrogen channel stop was implanted around the chip periphery. Following activation at 1650°C, the diodes were passivated with a thick deposited SiO_2 film. Windows were then opened in the oxide and Ti/Al contacts were deposited on the mesa anodes, while a Ni contact was deposited on the cathode. The wafers were then annealed at 1000°C in Ar to form ohmic contacts. Thick Au layers were then deposited on the anodes and cathodes for current spreading, die attach, and wire bonding. Figure 1 shows a schematic cross-section through the 10 kV 4H-SiC PiN diodes.

Wafer Yield

Following wafer fabrication, all diodes on wafer were tested for forward voltage (V_F < 4.25 V at J_F = 100 A/cm^2) and reverse blocking (J_R < 0.2 mA/cm^2 at V_R = 10 kV) yield. V_F drift yield was examined by subjecting all diodes that passed the reverse blocking criteria to a 30 minute DC stress at 100 A/cm^2 and comparing the pre- and post-stress V_F. Any diode showing ΔV_F < 0.1 V passed the V_F drift criteria. Table I shows the yield statistics for the best 20 A/10 kV wafer fabricated to date. This wafer employed the hex etch BPD reduction technique, had an n^- drift layer thickness of 100 μm, was terminated with the multi-zone JTE, and had a p-injection layer doping of 1 x 10^{18} cm^{-3}. This particular wafer showed an excellent reverse blocking yield of 72.4%. A consequence of the relatively low p-injection layer doping is that the initial V_F yield was 86.2%. For comparison, we typically fabricate PiN diodes with an injection layer doping of 8 x 10^{18} cm^{-3} and achieve 100% V_F yield.

Table I. Wafer-level yield statistics of best yielding 20 A/10 kV 4H-SiC PiN diode wafer.

Yield Criteria	Specification	Yield
V_F	V_F < 4.25 V at J_F = 100 A/cm^2	86.2%
I_R	I_R < 0.76 μA at V_R = 10 kV	72.4%
V_F Drift	ΔV_F < 0.1 V during 30 min DC stress at J_F = 100 A/cm^2	54.8%
Total Yield		39.7%

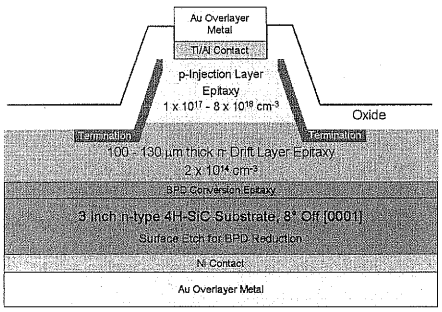

Fig. 1. Schematic cross-section of 10 kV 4H-SiC PiN Diode.

A major yield limitation continues to be V_F drift, as this particular wafer exhibited a V_F drift yield of 54.8%. This single wafer V_F drift yield was anomalously high for the hex etch low-BPD technique, showing a higher drift yield than the overall average of 40.1%. The KOH etch low-BPD technique shows a better average V_F drift yield of 51.3%. Figure 2 shows a histogram of the magnitude of V_F drift, separated into KOH etch or hex etch conversion processes, and compares these BPD conversion processes with die fabricated on a 4H-SiC wafer that included no BPD reduction process. The first bin in the histogram ($\Delta V_F < 0.1$ V) represents yielding diodes. Even though the selective KOH etch process provides the better V_F drift stability, further work remains to be done to bring the yields up to a level that is more amenable to a commercial process. Regardless, the benefits of either method of BPD density reduction is clear from Fig. 2. The BPD to TED conversion must be made more efficient, however, and further investigations of the epitaxial growth conditions that give us the most efficient conversion are under way.

DC Current-Voltage Characteristics

Individual diodes were mounted in custom designed high voltage packages capable of blocking in excess of 13 kV. Figure 3 shows the temperature dependent forward and reverse current-voltage (I-V) characteristics of a 20 A/10 kV from the best yielding wafer that has been fabricated, as described above. As shown in Fig. 3a, at room temperature the diode had a V_F of 3.87 V at 20 A (100 A/cm^2), which decreased to 3.60 V at 200°C. The differential resistance remains fairly constant with temperature, since the increase in substrate resistance with temperature is offset by the increase in minority carrier lifetime. A small drop in differential resistance with temperature was evident, possibly caused by an increase in dopant ionization at the higher temperatures. The most significant contribution to the drop in V_F with temperature results from the bandgap lowering that accompanies a temperature increase. Figure 3b shows that at 10 kV at room temperature the diode exhibited a reverse leakage current of less than 200 nA. Furthermore, the diode showed a very consistent, sharp breakdown at 11.5 kV. With an increase in temperature to 200°C the leakage current at 10 kV increased slightly, though only to 250 nA, and the breakdown voltage shifted out to greater than 13 kV, suggesting that these diodes exhibit stable avalanche breakdown.

A comparison of the reverse I-V characteristics of five diodes with the multi-zone JTE termination and five diodes with the guard ring termination are shown in Fig. 4. All 10 diodes were fabricated on wafers with 100 μm thick n$^-$ drift layers grown on substrates prepared with the hex etch low-BPD process, and the p-injection layers were doped at 1 x 10^{18} cm^{-3}. The guard ring-terminated diodes showed a higher, but softer breakdown than the multi-zone JTE-terminated diodes. However, the leakage currents at 10 kV of the guard ring-terminated diodes are slightly higher than those of the JTE-terminated diodes and early leakage appears to be more prevalent. Furthermore, wafer-level reverse blocking yield was also significantly higher in the JTE-terminated diodes, as shown in Table II, which compares three sets of companion wafers. The epitaxial layers of the two wafers in each set of companion wafers were grown simultaneously, with one wafer from each set fabricated with diodes terminated with the JTE and the other wafer fabricated with diodes terminated with guard rings. Among the three sets of companion wafers, the reverse blocking yield of the wafers with diodes terminated with the

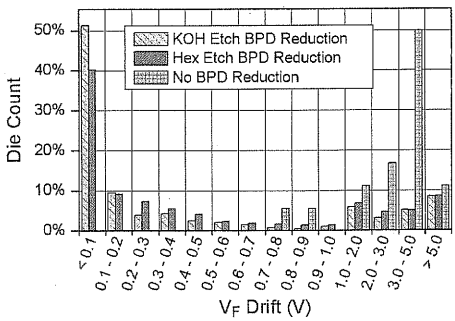

Fig. 2. Histogram of V_F drift for all fabricated die, separated into KOH Etch, Hex Etch, or no BPD reduction processes. First bin (< 0.1 V) indicates V_F drift yielding diodes.

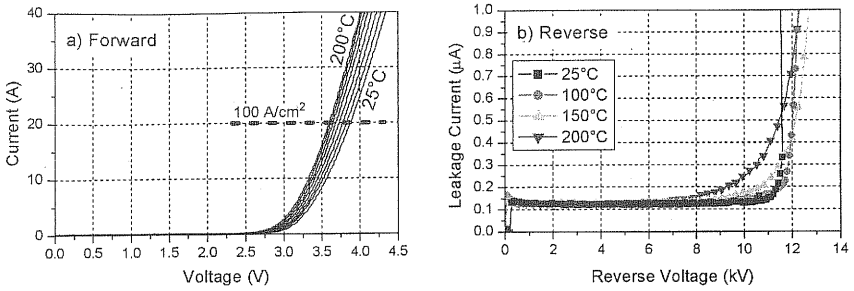

Fig. 3. a) Forward I-V characteristics at 25°C to 200°C (at 25°C intervals) and b) Reverse I-V characteristics (at 25°C, 100°C, 150°C, and 200°C) of a 20 A/10 kV 4H-SiC PiN diode with 100 μm thick n^- drift layer and multi-zone JTE termination.

JTE was 35% to 135% greater than that of their respective companion wafers with diodes terminated with guard rings.

Switching Characteristics

Our primary application drive for the development of the 10 kV 4H-SiC PiN diode is to pair with 4H-SiC DMOSFETs in 4H-SiC inverter modules capable of switching at 20 kHz. Of great concern for the successful development of these modules is the reverse recovery characteristics of the PiN diode, because the charge stored in the PiN diode during reverse recovery flows back through the DMOSFET while the DMOSFET remains at high potential. Thus, the power dissipated in the DMOSFET can be extremely high during the switching transients if the PiN diode stored charge is too great. The initial objectives of the 10 kV PiN diode development program was to improve die yields, but as we begin to refine the manufacturing process to improve die yields we are beginning more application driven development by examining ways to reduce the PiN diode stored charge during reverse recovery.

A simple method to decrease the stored charge is to limit the charge injection into the drift layer during forward conduction, which was accomplished by reducing the p-injection layer doping density down to 1 x 10^{17} cm^{-3}. Selected 4H-SiC PiN diodes, all with 100 μm thick n^- drift layers grown with the hex etch BPD reduction process and grown with p-injection layers doped at 1 x 10^{17} cm^{-3}, 1 x 10^{18} cm^{-3}, or 8 x 10^{18} cm^{-3}, were switched with an inductive load from a forward current of 20 A to a reverse voltage of -2000 V. A 5 A/10 kV 4H-SiC DMOSFET [5] (overdriven to 20 A) was used as the switch, and the slew rate of the diode in the circuit was 250 A/μs. Figure 5 compares the reverse recovery transients of three 4H-SiC PiN diodes with the three different p-injection layer dopings. The peak reverse current, reverse recovery time, and stored charge all dropped with decreasing injection layer doping, as is expected due to the decrease in charge injection during the forward state that accompanies the reduced p-injection layer doping. Table III summarizes the reverse recovery characteristics of these three diodes. The reverse recovery time dropped by 20% by reducing the anode doping density from 8 x 10^{18} to 1 x 10^{17} cm^{-3}. Perhaps more importantly, the stored charge dropped by 36%, reaching 1.43 μC in the diode with an anode doping of 1 x 10^{17} cm^{-3}. These gains in reverse recovery, however, come at the cost of increased V_F due the lower charge injection during the on-state, as shown in Table III. This trade-off is manageable, though, as V_F increased from 3.74 V to only 4.13 V with nearly two orders of magnitude reduction in p-injection layer doping.

Further reductions in charge storage are required beyond what gains have been made by reducing the injection layer doping. Unfortunately, the injection layer doping cannot be reduced much below 1 x 10^{17} cm^{-3} because the p-injection layer would need to be grown thicker to tolerate the wider depletion in the anode under reverse bias. Isolation of the diode mesas would then require a deeper

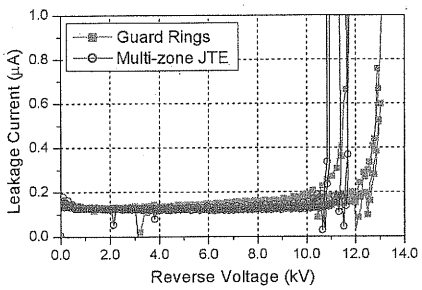

Fig. 4. Comparison of the Reverse I-V characteristics of 20 A/10 kV 4H-SiC PiN diodes employing guard ring (closed squares) or multi-zone JTE (open circles) terminations.

Table II. Reverse blocking yield comparison of diodes terminated with multi-zone JTE or with guard rings.

Epitaxial Run	Blocking Yield Multi-Zone JTE	Blocking Yield Guard Rings
A	51.7%	22.4%
B	72.4%	53.5%
C	70.7%	50.0%

etch that may not be feasible with current technology. Therefore, other methods of decreasing the charge storage are being investigated. The n^- drift layer thickness plays a large role in how quickly charge is removed from the drift layer during reverse recovery. Figure 6 shows the stored charge as a function of n^- drift layer thickness ranging from 100 to 130 μm for diodes with a p-injection layer doping of 8 x 10^{18} cm^{-3}. The diodes with p-injection layer doping of 1 x 10^{18} and 1 x 10^{17} cm^{-3} have also been added to Fig. 6 for reference, along with trend lines based on the data for the diodes with an injection layer doping of 8 x 10^{18} cm^{-3}. Based on these data and trend line assumptions, if an injection layer doping of 1 x 10^{17} cm^{-3} is employed and the n^- drift layer thickness is reduced to 90 μm, we may be able to achieve a reverse recovery charge of less than 1 μC. Of course, any reduction in the drift layer thickness could potentially reduce the blocking capabilities, so we must balance this blocking voltage/switching speed trade-off as we refine the structure of these diodes. We are currently investigating alternative means of reducing injected and stored charge, including examining local minority carrier lifetime control in the epitaxial films, cathode injection control layers, and diode structures that can further help control charge injection.

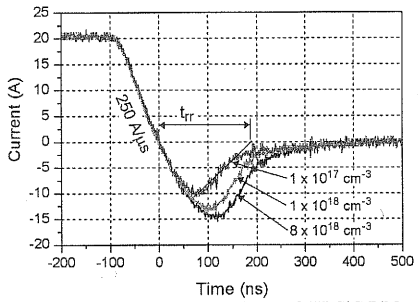

Fig. 5. Reverse recovery transients of 4H-SiC PiN diodes with 100 mm thick n^- drift layers and p-injection dopings of 1 x 10^{17}, 1 x 10^{18}, or 8 x 10^{18} cm^{-3}.

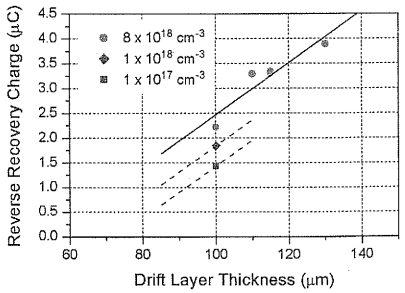

Fig. 6. Reverse recovery charge as a function of n^- drift layer thickness.

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Table III. Reverse recovery characteristics of 20 A/10 kV 4H-SiC PiN diodes.

Anode Doping (cm^{-3})	Peak Reverse Current (A)	Reverse Recovery Time (ns)	Stored Charge (μC)	Forward Voltage (V)
1×10^{17}	10.0	195	1.43	4.13
1×10^{18}	13.0	220	1.84	3.91
8×10^{18}	14.8	245	2.22	3.74

Summary

Development is continuing on 4H-SiC PiN diodes that block in excess of 10 kV and conduct up to 20 A. Reverse blocking yield on a hero wafer with diodes consisting of a 100 μm thick n^- drift layer was 72.4%. V_F drift continues to be the most significant yield limiter, as only 54.8% of the diodes passed the V_F drift criteria, but refinements of the BPD reduction epitaxial growth processes are continuing, which help to optimize V_F drift yields. 20 A/10 kV 4H-SiC PiN diodes with V_F of less than 3.9 V at 100 A/cm^2, reverse breakdown at greater than 11.5 kV, and reverse leakage currents of less than 200 nA at 10 kV were demonstrated. For high frequency inverter modules, reverse recovery time and stored charge are too high, but we are making progress on reducing these parameters to satisfy the stringent requirements of 20 kHz switching.

Acknowledgements

This work was supported by Sharon Beermann-Curtin of DARPA through contract N00014-05-C-0202 monitored by Dr. Harry Dietrich of the Office of Naval Research.

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