SILICON SOLAR CELLS WITH INTEGRAL BYPASS DIODES

M. A. GREEN, E. GAUJA and W. WITHAYACHAMNANKUL*

Solar Photovoltaic Laboratory, School of Electrical Engineering, University of New South Wales, Kensington 2033 (Australia)

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Summary

Field experience has brought to light undesirable features of the operation of solar cell arrays due fundamentally to mismatch in the output of individual cells. These difficulties can be avoided if bypass diodes are connected across cells or groups of cells.

A new technique is described for integrating bypass diodes into the solar cell structure with minimal additional cell processing. After fabrication the cell can be interconnected in the same manner as conventional cells. Experimental results are described verifying proposed processing sequences and system performance of the cells.

1. Introduction

Recent large field installations of solar cells such as the 60 kW array field at Mount Laguna [1] dramatically illustrate the types of problem which can arise in large photovoltaic systems because of mismatch in the output of individual cells. This mismatch may be due to the physical differences between cells or cell starting materials arising during normal processing, it may be due to cell cracking or aging or it may be due to external events such as cell shadowing.

Two types of problem are apparent. The first is related to the fact that the current output of series-connected solar cells is determined by the output of the worst cell in the series connection. This not only gives rise to a "mismatch loss" when cells are connected [2] but also gives rise to the well-known susceptibility of solar cell arrays to partial shading. The effect of shadowing a single cell, *e.g.* by a leaf or a bird dropping, is greatly multiplied throughout the array. In the worst cases the power loss due to shading a single cell is multiplied by the number of series-connected cells in the array. For large power arrays in which there are parallel connections of cells, this

*Present address: Department of Electrical Engineering, Prince of Sonkla University, Thailand.

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unpredictable power reduction is not desirable. For smaller arrays with few or no parallel connections, one leaf could cause the system output to drop to a fraction of rated power, eventually resulting in system failure.

A more serious problem can arise if a section of an array is operated at a low output voltage. This occurs in some array voltage regulation schemes [3] and is likely to occur when maintenance is being carried out on any reasonably sized array. Sections of the array will be shorted out for the safety of the maintenance crew. A low output cell in such cases becomes reverse biased and, in the worst case, can have the maximum power-generating capability of the section held at low voltage dissipated in it [2, 3]. The resultant heating can damage the encapsulation or crack cells, thereby causing module failure. Field failures due to this effect are well documented. Some manufacturers now specify "safe operating regions" for their modules [3].

The previous difficulties can be avoided by connecting bypass diodes across subelements of the array [2 - 4]. From the point of view of optimum performance the ideal subelement is the individual cell. However, this would not be cost effective with discrete bypass diodes. With discrete devices the subelement chosen would most probably be the maximum number of series-connected cells which could be short circuited without overheating a low output cell. This value lies in the range 10 - 15 [2] and tends to decrease as cell efficiencies increase.

A diode simply integrated into the structure of individual cells using the techniques to be described [5] not only would increase the tolerance to mismatch above that of such a connection of discrete devices but also would provide simpler module assembly and a higher level of reliability because of fewer interconnections.

2. Integration approach

Several techniques have been proposed in the past for integrating a bypass diode into the solar cell structure [6 - 9], primarily in connection with a similar need arising in space arrays. These techniques suffer from the disadvantage of requiring at least one extra connection per cell and at least two without specially designed interconnections.

The basic integration scheme used in the devices described in the present paper is shown in Fig. 1(a). A diode in reverse polarity to the bulk of the solar cell is isolated from it essentially by the lateral resistance of the substrate. An approximate equivalent circuit of the structure when illuminated is shown in Fig. 1(b). Not only is a bypass diode added to the normal cell equivalent circuit, but a parasitic resistance R_s in series with it and a parasitic shunt resistance R_{sh} are also introduced.

The shunt resistance introduces additional power loss when the cell is operating normally whereas the series resistance does so when the bypass diode is being used. Additionally the area of the cell required for the bypass

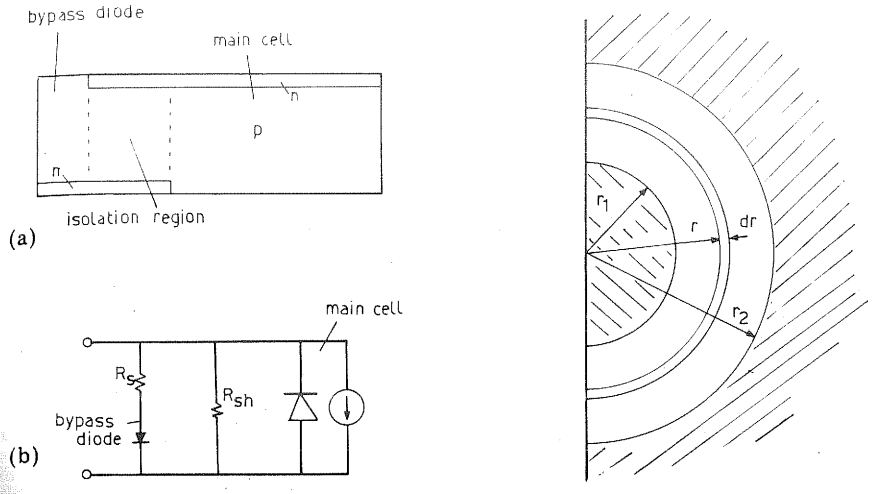

Fig. 1. Schematic diagrams showing the approach used to integrate the bypass diode: (a) a cross section of a cell showing back-to-back diodes and the resistive isolation region; (b) a lumped equivalent circuit.

Fig. 2. Semicircular integrated bypass diode geometry.

diode is wasted, as is some of the area of the isolation region. The bypass diode geometry is selected to minimize these losses. For cells representative of present technology, the losses can be kept insignificantly small. For example, for cells 10 cm in diameter the combined loss due to these effects can be kept to less than 3% of the total cell output.

3. Design of the bypass diode

The optimum geometry of the bypass diode depends on the details of the particular cell design since it is possible to locate the bypass diode under bus-bars or contact pads. This reduces the active area of the cell used by the diode.

However, a good general purpose geometry for the diode is the semicircular shape shown in Fig. 2. In Appendix A this geometry is analysed without giving any credit for the location of the diode under the normal top metallization of the cell. Hence the results obtained are worse than those that can be achieved in practice.

The three steps in the design of the bypass diode are as follows.

(i) The parameters of the substrate to be used for the cells should be determined. The important parameters are the substrate area A, thickness t and electrical resistivity ρ.

(ii) The performance required for the bypass diode when it is conducting (*i.e.* when the cell is shaded) should be defined. The parameter that can be controlled is its series resistance R_s. The characteristic resistance R_{ch} of the cell [10] is defined as its open-circuit voltage V_{oc} divided by its short-

circuit current I_{sc} under normal operation: $R_{ch} = V_{oc}/I_{sc}$. A parameter x can be defined as R_s/R_{ch}. The maximum power dissipated in the bypass diode (when conducting) is then approximately $1 + x$ times that generated by an unshaded cell.

If x is selected to be too large, it will negate the advantage of having bypass diodes across individual cells. As the selection of a large x will reduce the design area of the bypass diode as well as the power dissipated in it, this could ultimately lead to overheating problems. However, if x is selected to be too small, the bypass diode will consume an inordinate amount of cell area. Reasonable design values are thought to lie in the range 0.2 - 1.0. In this range the good lateral thermal conductivity of the silicon ensures that the temperature at the bypass diode does not rise dangerously above that of the rest of the cell.

Selecting x in this range allows the area required for the bypass diode to be found. For the semicircular bypass diode the radius r_1 is given by

$$r_1 = \left(\frac{2t\rho A J_{sc}}{\pi x V_{oc}}\right)^{1/2} \tag{1}$$

where J_{sc} is the short-circuit current density, and A, t and ρ are the area, thickness and resistivity of the substrate respectively.

(iii) The width of the isolation region around the edge of the bypass diode should be selected. This width determines the parasitic shunt resistance of the cell. Again there is an optimum value for minimum loss, since not all the carriers generated by sunlight in this region contribute to the output current of the cell. This is discussed further in Appendix A. For the semicircular bypass diode the optimum value of the radius r_2 in Fig. 2 is given implicitly by

$$2z^2 \ln z - z^2 + 1 \approx \frac{4tV_{oc}}{\rho r_1^2 J_{sc}} \tag{2}$$

where $z = r_2/r_1$ (Appendix A). The corresponding total fractional power loss FL introduced by the bypass diode when the cell is in the generating mode is given by

$$FL = \pi r_2^2/2A \tag{3}$$

This is just the ratio of the area occupied by the bypass diode and the isolation region to the total cell area.

Designs for cell areas corresponding to circular cells 5 and 10 cm in diameter are given as a function of substrate resistivity in Figs. 3 and 4. Important features are that, the thinner the cell and the larger the cell area, the smaller is the fractional power loss created by the bypass diode. This is precisely the direction in which present technology is evolving. For a cell 5 cm in diameter the fractional loss is less than 0.07 for all substrate resistivities in the range 2 - 9 Ω cm. For cells 10 cm in diameter the corresponding loss is 0.04 for resistivities in the range 0.5 - 7 Ω cm.

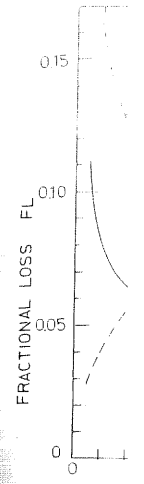

Fig. 3. Opt
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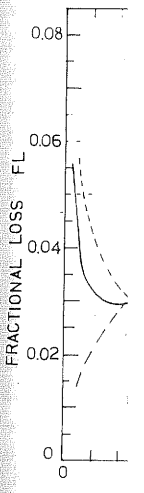

Fig. 4. Opti
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4. Processi

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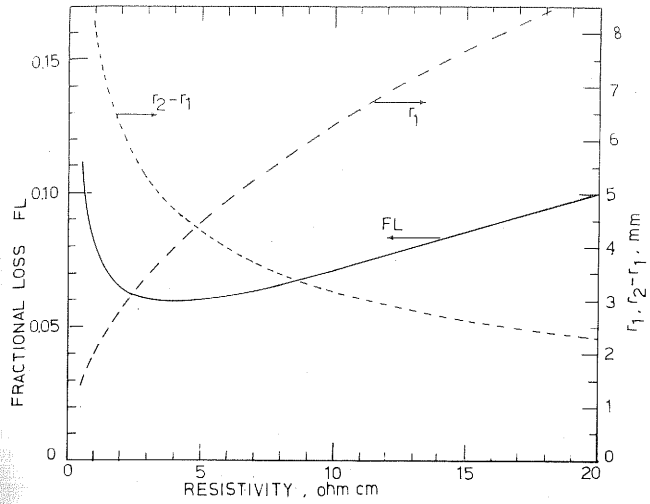


Fig. 3. Optimum parameters for the design of semicircular bypass diodes for cells 5 cm in diameter for different substrate resistivities. The cell parameters are t = 300 μm, x = 0.5 and V_{oc}/J_{sc} = 19 Ω cm^2.

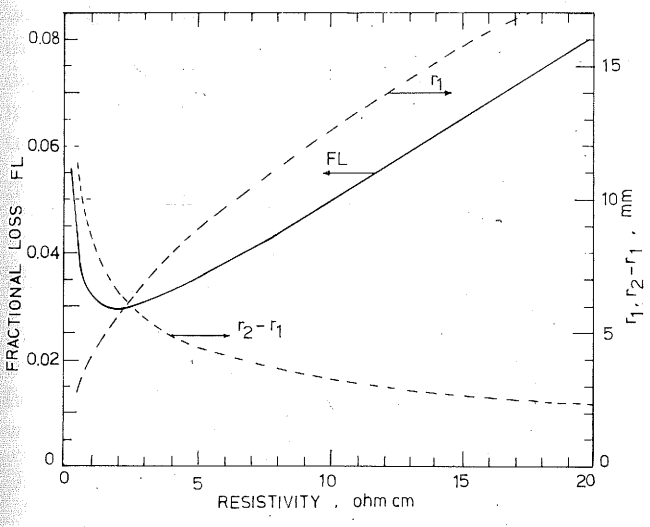


Fig. 4. Optimum parameters for the design of semicircular bypass diodes for cells 10 cm in diameter for different substrate resistivities. The other cell parameters are given in Fig. 3.

4. Processing approaches

There are a variety of different processing approaches to the production of the integrated bypass diode. The incorporation of the diode requires extra processing at some stage of cell manufacture. This means that the cost per initial peak-watt-generating capability will be higher than for cells without

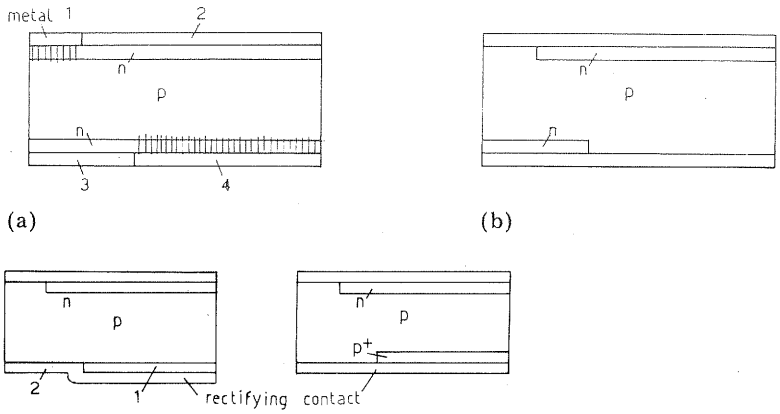


Fig. 5. Schematic diagrams showing three different types of approach to producing the bypass diode: (a) junction shorting; (b) junction definition; (c) rectifying metal–semiconductor contacts.

this feature but not dramatically so. A study of the costs of present processing steps used to fabricate cells as well as of the processing sequences projected for the future [11] indicates that it should always be possible to incorporate the diode with an increase in the module cost per peak watt of between 3 and 10%. The cost per unit energy delivered in an operating system will be lower for the reasons previously outlined.

Three processing approaches are shown in Fig. 5. In the first, the "junction-shorting" approach (Fig. 5(a)), use is made of junctions formed on both sides of the cell as in the normal gaseous diffusion process. In regions 1 and 4 the metallic regions are heated to sufficiently high temperatures to allow them to short through the junctions in these areas. These regions could be deposited and heated prior to regions 2 and 3 as for the experimental devices described later. Alternatively, a more sophisticated approach would be to use localized heating, *e.g.* by laser or electron beam pulsing, to define the four areas. If the sheet resistivity of the diffused layer is much less than the resistivity of the substrate divided by its thickness, metallization in region 3 is not required.

The second approach is the "junction definition" approach (Fig. 5(b)). In this approach, junctions are present only in desired regions. This can be accomplished by using diffusion masking or by selective etching after diffusion using, for example, a screen-printed mask. The third approach (Fig. 5(c)) uses the rectifying properties of metal–semiconductor contacts rather than p–n junctions to create the bypass diode.

The choice between these processes or variations of them depends on the details of the particular baseline process for producing cells which is desired to be modified to incorporate the bypass diode.

It should be noted that there is no shorting of front to back contacts in any of the schemes of Fig. 5, apart from through the shunt resistance pro-

vided by the isolation region. The p–n junctions in the isolation region (or the rectifying metal–semiconductor contacts in Fig. 5(c)) prevent any shorting route apart from laterally through this region. An examination of the lumped equivalent circuits in Figs. A1(b) and A1(c) clarifies this point.

5. Experimental results

Experimental devices were fabricated using techniques as used in conventional silicon solar cell processing. The processing steps were as follows: (i) a chemical etch and clean of the silicon wafer; (ii) junction diffusion from a $POCl_3$ source (at 850 °C for 45 min); (iii) removal of the diffusion oxide and edge junction; (iv) vacuum evaporation of aluminium on selected areas of the top and rear of the cells; (v) alloying at 850 °C (for 5 min) to short through the junctions; (vi) chemical removal of the oxides grown during the alloying step; (vii) vacuum evaporation of the contacts to the top and rear of the cells; (viii) contact sintering (at 400 °C for 2 min); (ix) vacuum evaporation of an antireflection (AR) coating.

A sketch of the front and back of a completed device is shown in Fig. 6. The semicircular regions indicate where the bypass diode is located. The cells were fabricated on boron-doped wafers of nominal resistivity 1 Ω cm, diameter 5 cm, thickness 280 μm and orientation (100). The bypass diode design was non-optimal for these parameters with r_1 = 3 mm and r_2 = 10.5 mm. The bypass diode was included at the wide end of the tapering bus-bar to minimize active area loss.

The dark current–voltage characteristics of device BD3 are shown in Fig. 7, clearly demonstrating the "back-to-back diode" characteristics of the device. Some series resistance is apparent in the reverse characteristics and shunt resistance is apparent at low current levels. The output characteristic under illumination of the device is compared with that of a control device C6 without the bypass diode in Fig. 8. Both devices had no AR coating. This control device was processed similarly except that step (iv) above was modified so that aluminium was evaporated over the entire rear of the wafer, with none evaporated on top. The small difference in short-circuit current is

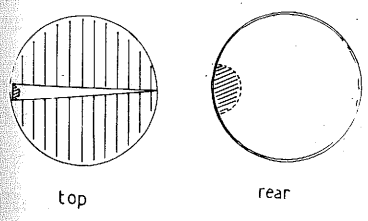
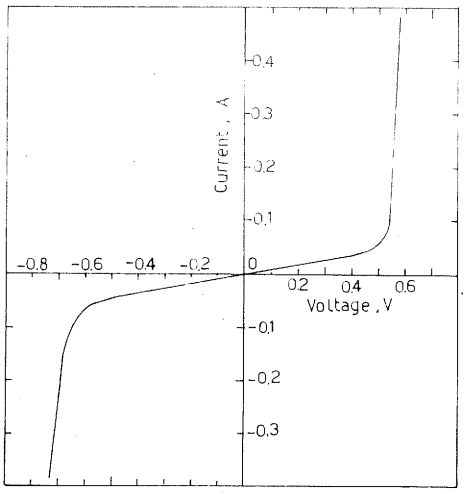


Fig. 6. Sketch of p–n junction solar cells as fabricated using the junction-shorting approach. The shaded regions indicate the location of the bypass diode. At the top of the cell the junction is shorted by the metallization in this region, whereas at the rear of the cell this is the region where the junction is *not* shorted.



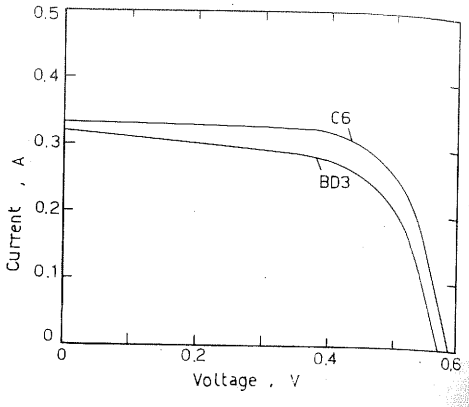


Fig. 7. Dark current–voltage characteristics of solar cell BD3 fabricated with the structure of Fig. 6.

Fig. 8. The output characteristics of BD3 under simulated terrestrial illumination of 80 mW cm^{-2} intensity compared with a control device C6 processed similarly but without the bypass diode.

not definitely attributable entirely to the bypass diode, although the decreased shunt resistance certainly is. The performance of device C6 is typical of that observed for p–n junction cells of conservative design prior to deposition of the AR coating. The loss in output associated with the bypass diode was about 19% compared with less than 6% for an optimized design on a wafer of this size.

Device BD3 was then completed by depositing an AR coating and was connected in series with a commercial module containing 18 series-connected cells of a similar size. The performance of this series connection was tested under tungsten illumination of uncalibrated intensity. Figure 9 shows the results.

With no cells shaded the module plus the extra cell had an output characteristic as shown by the full curve labelled "full output". With most of *one* of the cells in the commercial module shaded the output dropped dramatically to the dotted curve labelled "normal cell shaded". With the cell with the bypass diode *completely* shaded the original curve shifted to the left by about 1 V to the second full curve. With the bypass diode *partially* shaded the curves switched from one to the other of the full curves as the bypass diode became operational.

6. Summarizing remarks

Experimental techniques for integrating bypass diodes into conventional silicon solar cells were demonstrated. Cells with the integrated bypass diode are shown to increase the tolerance to shadowing of series-connected

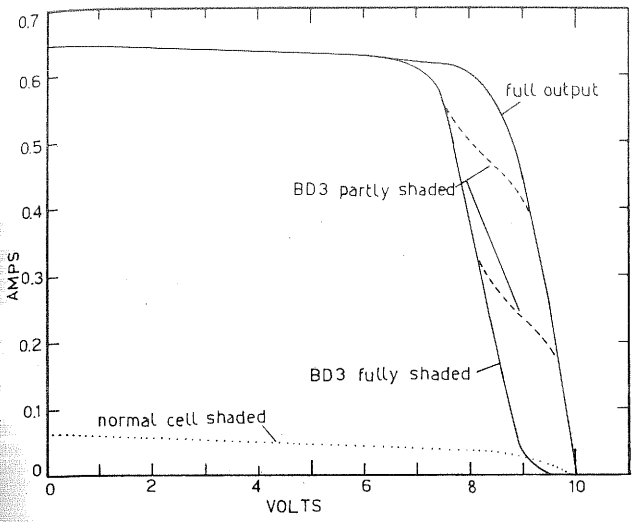


Fig. 9. Output of a circuit consisting of 18 conventional solar cells connected in series together with cell BD3 which has an integrated bypass diode. With one of the conventional cells shaded the output is low. With BD3 shaded the output power of the series connection remains high.

cells. The bypass diodes will also reduce mismatch losses and eliminate "hot spot" problems arising from mismatch.

Techniques were developed for designing bypass diodes for any particular solar cell structure. Cells representative of present technology including a well-designed bypass diode should cause a fractional reduction in output power of less than 0.04. Since the current output of series-connected cells without the bypass diode is that of the worst cell, power loss at the module level will be reduced below this. Life cycle energy output will be higher than a comparable system without bypass diodes.

Acknowledgments

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Appendix A

Design of semicircular bypass diodes

Defining the characteristic resistance R_{ch} of a solar cell as V_{oc}/I_{sc}, the series resistance R_s of the bypass diode is selected as some fraction x of this resistance. This gives the radius required for the bypass diode as

$$r_1 = \left(\frac{2t\rho A J_{sc}}{\pi x V_{oc}} \right)^{1/2} \tag{A1}$$

To select the width of the isolation region, the trade-off between loss of power due to the shunt resistance introduced by this region and the loss of some of the power-generating capabilities of this area has to be examined. A lumped equivalent circuit of the cell is shown in Fig. A1(b). At short circuit, voltages across the diodes will be small. They will be non-conducting and can be replaced by open circuits to give the equivalent circuit of Fig. A1(c). Of the current introduced at node i, that flowing to the left is lost. The current labelled ΣI_r is also lost. This component generally will be much smaller than the ΣI_f component (less than 10%). It can be minimized, if desired, by keeping the area of the rear p–n junction and its metallization in the isolation region to a minimum, leaving the remainder of the rear of this region a suitably passivated surface.

It should be noted that a voltage will build up as the centre of the isolation region is approached. If this becomes large enough to forward bias the diodes in the equivalent circuit at this location, a "dead region" will occur here [A1]. For well-designed devices this will not be a problem unless the substrate resistivity is very low (below about 0.2 Ω cm).

To calculate the major loss component I_2, let us consider Fig. 2. The resistance to current generated at radius r flowing towards the bypass diode is

$$R_L = \frac{\rho \ln(r/r_1)}{\pi t} \tag{A2}$$

whereas that to carriers in the opposite direction is

$$R_R = \frac{\rho \ln(r_2/r)}{\pi t} \tag{A3}$$

Hence the fraction of current generated at radius r which is lost is

$$f = \frac{\ln(r_2/r)}{\ln(r_2/r_1)} \tag{A4}$$

The current generated at radius r in the incremental area shown is

$$I(r) = J_{sc}\pi r \, dr \tag{A5}$$

Hence component I_2 is given by

$$I_2 = \int_{r_1}^{r_2} \frac{\ln(r_2/r)}{\ln(r_2/r_1)} J_{sc}\pi r \, dr \tag{A6}$$

$$= \frac{J_{sc}\pi {r_2}^2}{\ln(r_2/r_1)} \int_{r_1/r_2}^{1} (-x \ln x) \, dx \tag{A7}$$

$$= \frac{J_{sc}\pi {r_2}^2}{\ln(r_2/r_1)} \{\tfrac{1}{4}(x^2 - 2x^2 \ln x)|_{r_1/r_2}^{1}\} \tag{A8}$$

$$= \frac{J_{sc}\pi {r_1}^2}{4}\left(\frac{z^2}{\ln z} - \frac{1}{\ln z} - 2\right) \tag{A9}$$

where $z = r_2/r_1$.

A reasonable approximation for the power loss PL introduced by the isolation region is then

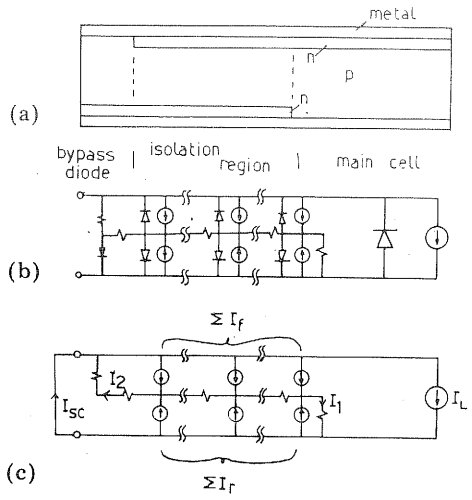
$$PL = \frac{V_m J_m \pi {r_1}^2}{4}\left(\frac{z^2}{\ln z} - \frac{1}{\ln z} - 2\right) + \frac{{V_m}^2 \pi t}{\rho \ln z} \tag{A10}$$

where V_m and J_m are the voltage and current density at the maximum power point. The second term on the right-hand side approximates the power loss due to the parasitic shunt resistance. Differentiating with respect to z gives the following implicit equation for its optimum value:

$$2z^2 \ln z - z^2 + 1 = \frac{4tV_m}{\rho {r_1}^2 J_m} \approx \frac{4tV_{oc}}{\rho {r_1}^2 J_{sc}} \tag{A11}$$

The corresponding expression for the total minimum fractional power loss FL_{min} including that due to the area occupied by the bypass diode is

$$FL_{min} = \pi {r_2}^2 / 2A \tag{A12}$$



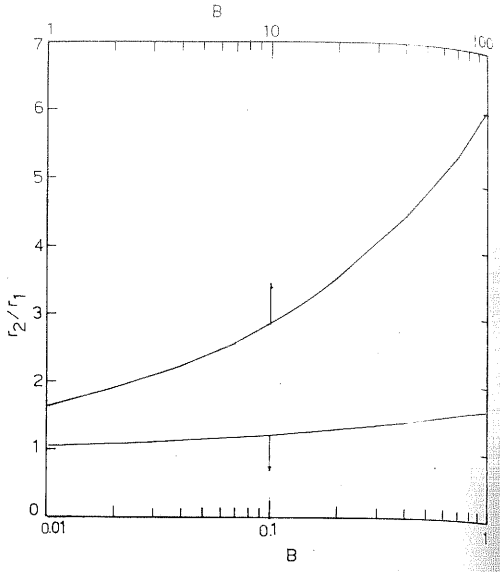


Fig. A1. (a) Physical structure of a device with an integrated bypass diode; (b) the corresponding equivalent circuit; (c) the equivalent circuit at short circuit.

Fig. A2. Plot allowing the optimum bypass diode design.

This is just the ratio of the area enclosed by the bypass diode and isolation region to the total diode area. The same result has been found for all other bypass diode geometries studied to date when the design is optimal [A1].

For the semicircular diode the optimum design is found by iteratively solving eqn. (A11) using the Newton–Raphson iteration for $z = r_2/r_1$:

$$z_{i+1} = \frac{2z_i^2 \ln z_i + z_i^2 + B}{4z_i \ln z_i} \qquad \text{(A13)}$$

where B is $4tV_m/\rho r_1^2 J_m$. A plot of optimum z *versus* B is given in Fig. A2. The same optimum is obtained for circular and quarter-circular bypass diode geometries, although r_1 will be divided or multiplied respectively by $2^{1/2}$ for the same value of x. The power loss at optimum design will be multiplied or divided respectively by $2^{1/2}$.

Reference to Appendix A

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