FRONT-END INTEGRATION EFFECTS ON GATE OXIDE QUALITY

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ABSTRACT

In this paper, the impact of several front-end processing steps (up to gate oxidation) on gate oxide integrity (GOI) is evaluated. In PBL isolation processing, the use of as-deposited amorphous silicon (a-Si), subsequently annealed during nitride deposition, results in better structural and electrical properties compared to as-deposited polysilicon or as-deposited a-Si with an extra anneal step prior to nitride deposition. Thicker or dual sacrificial schemes exhibit improved gate oxide low voltage breakdown and charge-to-breakdown. Dilute RCA chemistries during pre-gate cleaning produce equal or better surfaces for gate oxidation than the conventional non-dilute RCA with less chemical usage. As gate oxides are scaled below 100Å, lowering gate oxidation temperature is proven to result in far better gate oxide quality than maintaining process temperatures at or above 900°C and diluting oxygen in either argon or nitrogen.

INTRODUCTION

Gate oxide integrity in semiconductor MOS devices depends on many of the processing steps in IC fabrication [1-3]. In order to isolate the effect of each step on GOI, this paper focuses on the front-end processes only.

Poly-Buffered LOCOS (PBL) for active region formation has been studied in terms of pad oxide, polysilicon, and nitride layer thicknesses on bird's beak reduction and electrical performance [4]. The added poly layer is also known to reduce the stress from the nitride during high temperature oxidation [5]. The annealed amorphous silicon films have demonstrated much improved film qualities in terms of grain size and interface smoothness. However, very little information has been published on using an as-deposited amorphous silicon layer for the buffered layer to replace polysilicon.

Sacrificial oxide has been used to eliminate silicon nitride spots or ribbons caused by the reaction of NH_3 and H_2O during field oxide growth [6,7]. High temperatures (~1000°C) are normally used for sacrificial oxidation; however, the optimum thickness of this oxide and its effects on gate oxides below 100Å has not been fully investigated.

Pre-gate cleaning is one of the most critical preceding gate oxidation. Full RCA (H_2SO_4:H_2O_2, dilute HF, NH_4OH:H_2O_2:H_2O (SC-1), and HCl:H_2O_2:H_2O (SC-2)) has been used traditionally for active regions in order to obtain particle and metallic free surface passivated with a chemical oxide. It has been found that dilute SC-1 and SC-2 have equal or better particle and metal removal efficiency [8,9]. However, very little information on the extended bath lifetime for dilute chemistries and the correponding gate oxide yield, which are important for manufacturing and cost of ownership (CoO) has been found in the literature.

As silicon device dimension are reduced the demand for gate oxides with thicknesses well below 100Å has escalated from a development interest to a manufacturing necessity. While in the past it has been possible to scale oxide thickness simply by decreasing the oxidation time of standard processes, this approach is now reaching its manufacturing limits; typical oxidation times for oxides formed by this conventional appoach are now falling well under 10 minutes. In order to achieve slower growth rates, low temperature (<900°C) and dilute oxidation have been proposed. However, these oxides need to be characterized to see whether they exhibit comparable dielectric strength compared to high temperature and nondilute oxidations.

In this paper, we demonstrate that gate oxide properties can be improved by using a-Si instead of polysilicon buffer layers in PBL; by increasing the thickness of a sacrificial oxide or using double sacrificial oxide layers; by using dilute chemistries for pre-gate cleans; and by

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reducing oxidation temperatures and increasing HCl flows during gate oxide processing when gate oxides are scaled below 100Å.

EXPERIMENT

N^+ poly-gated MOS capacitors with 105Å gate oxides were used for this study. Several experiments relating to the PBL stack, and the final wet etch processes were performed to evaluate their impact on gate oxide yield. Split lots for studying poly and amorphous silicon films with a thickness of 550Å in the ox/poly(amorphous)/nitride stack were processed at 625°C, 220mT and 550°C, 350mT. Transmission Electron Microscope (TEM) was used to evaluate grain size. After 6750Å field oxidation, the patterned PBL stack was etched from the active area down to bare Si.

After PBL stack removal, 400Å, 600Å, and dual 600/150Å sacrificial oxides were grown at 1000°C and then removed in 10:1 BOE with 30% overetch. Pre-gate cleans were performed using full RCA in a wet bench with traditional and dilute SC-1, (having $NH_4OH:H_2O_2:H_2O$ ratios of 1:1:5 and 0.05:1:5, respectively). The SC-1 and SC-2 baths had been used for production lots for 8 hours prior to this experiment.

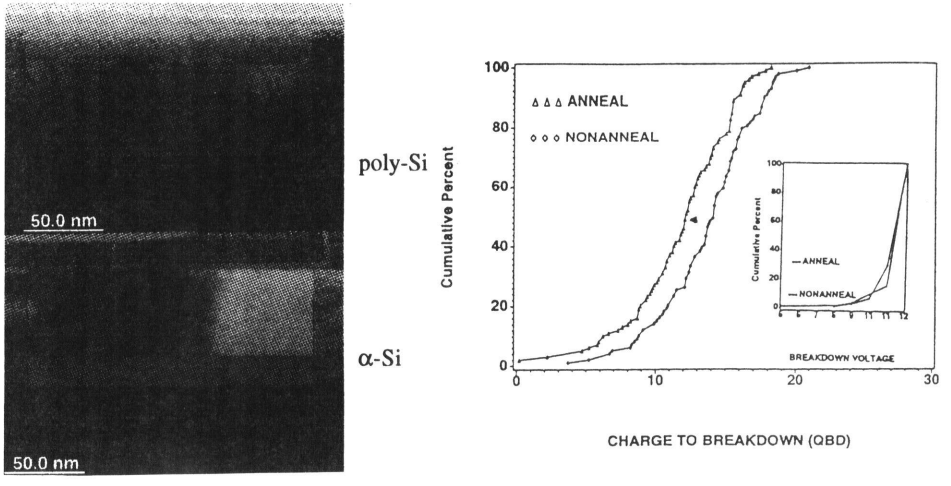
Gate oxides were grown in a horizontal furnace. Dilute oxidations was performed at either 900°C or 950°C using 10% and 50% O_2 diluted in either nitrogen or argon. In addition, these oxidations were performed with and without additional HCl (up to 4%). A frequently used two step oxidation cycle [10] consisting of 900°C 10% O_2 + 4% HCl followed by a 30 minute inert anneal at 1050°C, and by a final oxidation step at 900°C in 10% O_2 + 4% HCl, was also included for completeness. Low temperature oxidation was performed at 800°C and 850°C in a non-dilute dry O_2 ambient. When HCl was utilized, it was introduced several minutes after the commencement of oxidation in dry O_2. Both the dilute and low temperature approaches were compared against the historical 900°C non-dilute oxidation utilizing 3% HCl. All oxides received a conventional RCA clean prior to growth, and inert post-oxidation anneal.

For electrical evaluations, oxide thickness was targeted at 105Å for most of the experiments except for the sacrificial oxide evaluations, which used 90Å gates. Time-zero breakdown and charge-to-breakdown were measured as experimental outputs. Time-zero breakdown was monitored by measuring current during voltage ramping, with the breakdown voltage being defined at 1mA of current. Charge-to-breakdown was measured in accelerated fashion using a current ramp method stepping 0.1A/cm^2 at 125°C with 50 steps per decade at 2 second per step. Electron and hole trapping were studied by injecting a constant current of 0.1A/cm^2 from the substrate at room temperature. The capacitors investigated had an area of 0.1cm^2 and 0.001cm^2 and included minimal (area capacitors) or extensive (0.0025 cm) contact were with isolation edges (edge-intensive) capacitors.

RESULTS and DISCUSSION

Fig. 1(a) and (b) are TEM micrographs of as-deposited poly and as-deposited amorphous silicon films followed by nitride deposition. The as-deposited poly silicon film had a grain size approximately equal the film thickness, which is typical for grain growth in thin films (Fig. 1a). However, the as-deposited amorphous silicon film, recrystallized during nitride deposition (Fig. 1a), had grains much larger than the film thickness (some of the grains appear to be at least 1μm in size). More striking in Fig. 1 is that both interfaces of the recrystallized film are much smoother than in the poly silicon film. Based on this result, poly was replaced by amorphous silicon for PBL stack. The argument was then whether the immediate anneal would be necessary following amorphous silicon deposition. Fig. 1(b) shows the percent cumulative time-zero breakdown and charge-to-breakdown plots from split lots with and without immediate anneal prior to nitride deposition, indicating that statistically higher gate oxide yield can be obtained for area capacitors without the immediate anneal. Similar results were observed for field edge-intensive capacitors. The reduction in voltage breakdown for both area and edge capacitors indicate that poly films annealed during nitride deposition have fewer defects and better resistance to edge stress. This may

be attributed to several factors. First, larger grains tend to have better resistance for the acid to go through pad oxide during nitride and poly wet etch to pit the silicon surface and the edge of the active area. Second, as-deposited amorphous silicon film may reduce the stress better during PBL formation and hence less thinning at bird's beak during gate oxide formation.



(a) (b)

Fig. 1 (a) TEM micrographs of and, (b) gate oxide performance of as-deposited poly and as-deposited amorphous annealed during nitride deposition.

400 and 600Å single and double 600Å/150Å sacrificial oxide approaches were evaluated as potential means of improving gate oxide integrity, particularly for edge-intensive structures. Fig. 2 shows that both 600Å single and dual sacrificical oxides are found to significantly improve the edge-intensive charge-to-breakdown, with the double sacrificial process producing the greatest improvement on 90Å gates. Several factors are believed to contribute to the higher performance of the thicker or dual sacrificial oxides. Exposure to higher temperature for longer periods of time is believed to relax isolation stress more effectively. The resulting reduction in exposure time of bare silicon to BOE or HF during a constant sacrificial oxide etch may additionally minimize surface roughening [11]. Overall, these results are consistent with the notion that reducing isolation stress, initial roughening, and contamination levels are key factors to improving gate oxide performance.

Pre-gate clean was evaluated using full RCA clean in which dilute SC-1 (0.05:1:5) was compared to the traditional 1:1:5 SC-1. The main function of SC-1 in full RCA is to remove particles; thus particle removal efficiency was also evaluated using both ratios. There was no significant difference in particle removal efficiency, though the dilute SC-1 exhibited slightly better performance. Fig. 3 shows the breakdown voltages of large area capacitors ($0.1cm^2$); note that particles would have the greatest influence on large capacitor yield. The Q_{BD} plot was inserted as a gate oxide quality check. As can be seen, lesser lower breakdowns were obtained using RCA pre-gate clean with dilute SC-1 for large capacitors, indicating less defect densities. Similar results have been reported elsewhere [12]. However, no bath lifetime has been reported which is important for production and cost of ownership (CoO). The results shown in Fig. 3 came from the wafers that were run at an 8 hour bath lifetime for both SC-1 and SC-2 with longer H2SO4:H2O2 and dilute HF (50:1). This indicates that longer bath lifetimes, up to 8 hours do not have any detrimental effect on the silicon surface. In fact, lower ammonia concentration results in lower metal deposition

on the wafers due to its lower PH values. SC-1 and SC-2 can be eliminated with higher yield if high grade HF is used or modified with Cl concentration to prevent copper and particle deposition.

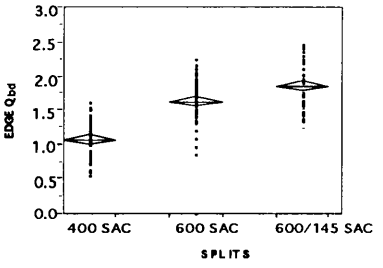


Fig. 2 Effects of scrificial oxidation scheme on the edge-intensive charge-to-breakdown of 90Å gate oxides grown at 850°C using 10% HCl

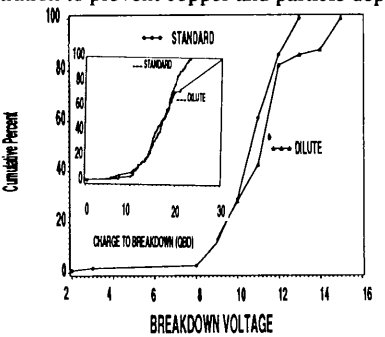


Fig. 3 Cumulative plot of breakdown voltage and charge-to-breakdown using dilute and non-dilute SC-1 during pre-gate clean.

Fig. 4 illustrates the Q_{BD} results obtained for area capactiors at 800°C utilizing 0% and 6% HCl, 850°C with 0%, 6%, and 10% HCl, and lastly, 900°C with 3% HCl as a control. The processes without HCl showed some degradation compared to the control, while Q_{BD} is slightly improved when HCl is introduced. The amount of HCl required depends on the oxidation temperature; 800°C processing shows much improved but lower Q_{BD} even up to 10% HCl compared to the control while 850°C shows comparable Q_{BD} up to 6% HCl. Edge-intensive capacitors demonstrate similar results. The same trends were replicated when utilizing 90Å oxides grown at temperatures lower than 900°C. These results indicate that a processing temperature of 850°C provides the best <100Å gate oxide properties in terms of charge-to-breakdown. The results further demostrates that HCl can benefit gate oxide integrity. The beneficial effects of HCl include impurity gettering and enhanced oxide stress relaxation [13], which can in turn lead to reduced gate oxide thinning. We also found that HCl can degrade edge-intensive Q_{BD} if it is introduced prior to the initial dry oxide. It is suspected that HCl interacts with isolation edges stress-related chlorine roughening or etching of active silicon [1]. Growing an initial dry oxide prior to introducing HCl can prevent chlorine etching along bird's-beaks by forming a protective film.

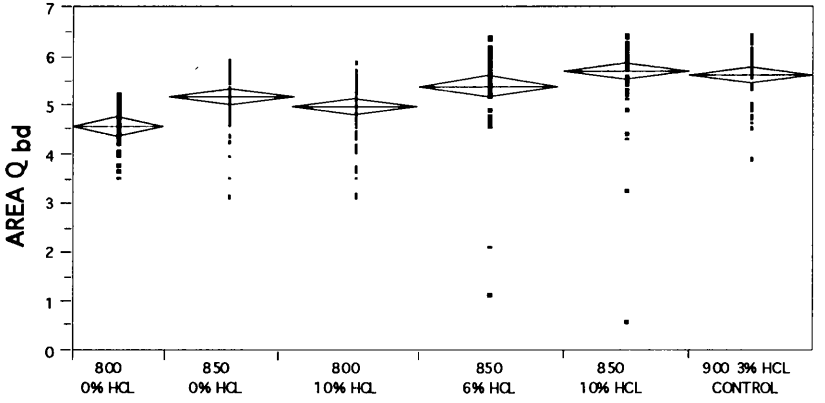


Fig. 4 Charge to breakdown for late 0-10% HCl 105Å gate oxides grown at 800°C and 850°C. Also shown for reference are the Qbd results from a 900°C, 3% HCl control oxide.

Fig. 5 (a) shows the area Q_{BD} data obtained from dilute, control, and two-step cycles at 900°C using argon as oxidation diluent and inert anneal. In this case, 4% HCl (with respect to oxygen flow) was added to all splits. Similar results were observed using nitrogen. It can be seen that argon and nitrogen cause severe Q_{BD} degradation in one-step dilute oxidation. However, the two-step oxidation sequence is found to compare remarkably well to the control cycle in spite of the use of inert-gas dilution during growth. It should be mentioned that severe degradation for dilute oxidation without HCl was observed as well.

We have seen that low temperature oxidation yields comparable results to the control when HCl is used. HCl greatly enhances the Q_{BD} of non-dilute oxides. However, it does not appear that the addition of HCl in dilute oxidation makes any difference in terms of charge-to-breakdown. To further understand the mechanisms responsible for the observed Q_{BD} degradation in the HCl-free dilute and non-dilute splits, electron and hole trapping and interface state density tests were performed. Fig. 5(b) shows typical voltage vs. time curves, under substrate injection conditions, obtained from several splits exhibiting degradation with respect to the control. It is clear that HCl plays a significant role in reducing oxide electron traps since the 900°C non-dilute cycle differs from the control only in the use of HCl during growth. Outside of the use of HCl, no significant differences in the electron trapping were observed; hence electron trapping can be ruled out as a possible explanation for degraded Q_{BD} during dilute cycles. The same scenario was applied to interface state generation using stressed CV, but no relationship has been found between degraded Q_{BD} and Dit.

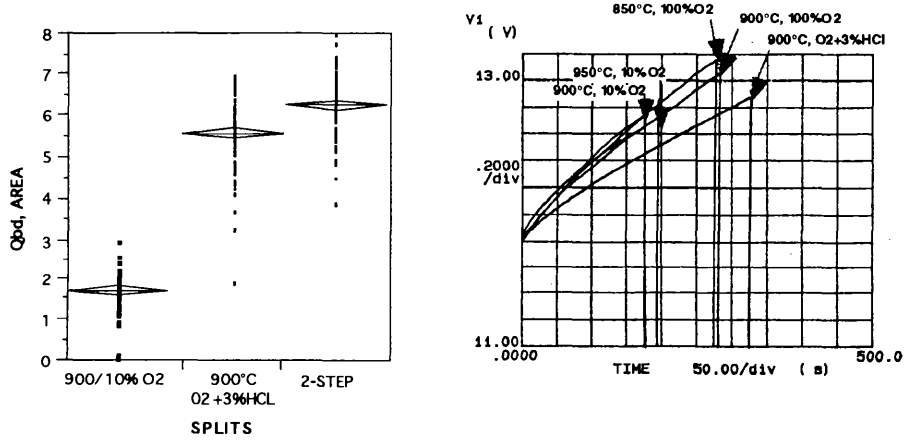


Fig. 5 (a) Charge-to-breakdown distributions obtained from area-intensive capacitors comparing oxide grown in argon-diluted ambients using one or two-step processing. 4% HCl was used in all splits; (b) voltage vs. time trapping rate curves continued to the point of dielectric breakdown, depicted by a sudden drop in voltage.

From the thorough electrical characterization described above it thus appears that inert-gas dilution leads to weaker oxides without affecting either interface states or bulk electron traps. These data suggest that either a localized defect within the bulk of the oxide or a pronounced interfacial

asperity may be triggering premature breakdowns. Other workers have published high-resolution TEM micrographs showing that inert-gas diluted oxidations lead to severe surface roughness [9] and that this roughness can be dramatically reduced by use of a two-step oxidation cycles. Our study confirms that two-step oxidation cycles eliminate the Q_{BD} degradation problem seen with one-step dilute oxidations, implying that the damage caused by dilute oxidations can indeed be healed.

Decreasing oxidation temperature is hence confirmed to be a viable means of attaining much slower oxidation rates with no sacrifice in dielectric strength. Low temperature oxidations also have the advantage of improving uniformity and dramatically reducing overall thermal budget. Thermal budget in particular is becoming an important requirement for future device application, due to an increasing number of critical implants preceding gate formation.

CONCLUSIONS

Several critical front-end steps including PBL, sacrificial oxides, pre-gate clean, and gate oxidation were addressed in this paper. As-deposited amorphous silicon films without an extra anneal step immediately after the deposition demonstrate better gate oxide yield compared to as-deposited polysilicon. Sacrificial oxidation schemes have a significant effect on gate oxide time-zero and charge-to-breakdown performance. Thicker single or dual sacrificial oxides show much improved charge-to-breakdown for edge-intensive, as well as area-intensive capacitors. Full RCA pre-gate clean using dilute SC-1 illustrates equal or slightly higher yield for both large capacitors and charge-to-breakdown when the bath lifetime reaches 8 hours. Low temperature oxidation (<850°C) in pure oxygen with some amount of HCl (3-10% of total flow) is an encouraging means of manufacturably scaling thermal oxides below 100Å.

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