Materials Science Forum Vols. 527-529 (2006) pp 1549-1552
online at http://www.scientific.net

Direct Electrical Characteristics of GaN Nanowire Field Effect Transistor (FET) without Assistance of E-beam Lithography (EBL)

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Keywords: Gallium Nitride, Nanowires, Field Effect Transistor, E-beam Lithography,

Abstract. We report on simple techniques for extracting the electrical properties of 1-dimensional semiconductor nanowires using standard ultraviolet (UV) photo-lithography instead of e-beam lithography (EBL), which is a commonly used technique for the fabrication of nanoscale electrical devices. For electrical transport measurement the gallium nitride nanowires (GaN NWs) were prepared by a horizontal hot-wall chemical vapor deposition (CVD) with metallic Ga and NH_3 gas for Ga and N sources, and GaN nanowire field effect transistor (FET) structures on a 8×8 mm^2 silicon wafer were fabricated by ordinary 2-mask photo-lithography processes. The estimated carrier mobility from the gate-modulation characteristics is on the order of 60 ~ 70 $cm^2/V{\cdot}s$. We found that our approach is a powerful and simple technique to extract the electrical properties of semiconductor nanowires. The material characteristics of GaN nanowires are also discussed.

Introduction

One dimension semiconductor nanowires provide a good system to investigate the dependence of electrical and thermal transport or mechanical properties on dimensionality and size reduction or quantum confinement effects [1, 2]. They are interesting building blocks for the fabrication of various devices on a nanoscale range due to their superior properties, such as the capability of doping modulation and the selectivity of carriers, to those of the carbon nanotube (CNT). They can be easily grown by various techniques: laser-assisted catalytic growth, chemical vapor deposition (CVD), hydride vapor phase epitaxy (HVPE) and metal-organic CVD [1-5]. Most nano-devices using these 1D semiconductor nanowires such as silicon, silicon carbide, gallium nitride, zinc oxide, tin oxide, and germanium are fabricated by conventional e-beam lithography (EBL) and ion-beam lithography (IBL). However, these techniques entail too much time and cost. Rapid, straightforward, and handy electrical measurements are always required for improving the material properties, based on feedback of the information on 1D semiconductor nanowires devices. For our study, we used gallium nitride nanowires (GaN NWs) due to their superior potential properties such as high break down field strength, high thermal conductivity, high saturation drift velocity, and excellent physical and chemical stability. Here, we demonstrate a simple technique for extracting the electrical properties of 1D semiconductor nanowires using a standard ultraviolet (UV) photo-lithography instead of e-beam lithography.

Experimental Details

For the experiment, the gallium nitride nanowires (GaN NWs) were prepared by a horizontal hot-wall chemical vapor deposition (CVD). C-plane sapphire wafers (2"~ piece) were used as substrates for GaN NW growth. Ni (2 nm) was deposited on the substrates by sputtering. The substrates were placed in the region of uniform temperature in the quartz tube reactor. Gallium (Ga) and nitrogen (N) components were supplied to the substrate by using metallic Ga and NH_3 gas. As a rule, the system was heated up to 900 °C under a flow of NH_3 at a rate of 20 sccm and maintained for 6 hrs, and then cooled down to room temperature. For the electrical transport measurements, the GaN NWs were dispersed onto the surface of a patterned silicon substrate which was prepared by ordinary UV photo-lithography processes for the electrical leads and where the underlying conducting Si wafer was used as the large-area gate in the FET structure as shown in Fig. 1. Fig. 1 (a) shows our mask layout (8×8 mm^2) for GaN nanowire patterning on the SiO_2/Si wafer. Source and drain electrodes were also defined by UV photo-lithography, not EBL processes, and then Ti/Au (30nm/100nm) were deposited successively on the electrode area by e-beam evaporation. To obtain stable electrical contacts, rapid thermal annealing was performed at 750 °C for 60 s in N_2 ambient. The electrical transport properties of the nanowires were investigated using three probe schemes consisting of source, drain, and back-gate in FET device structures.

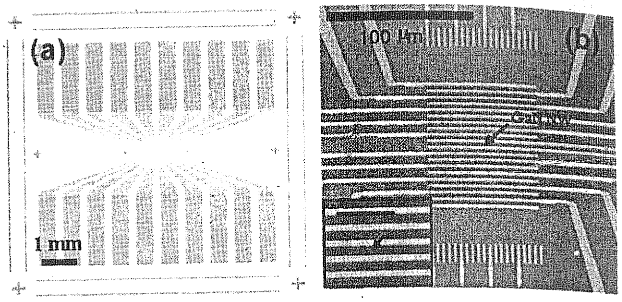

Fig. 1. (a) Mask layout (8×8 mm^2) for photo-lithography (2 mask processes) (b) SEM images of GaN nanowires patterned on SiO_2/Si wafer. Inset shows enlarged images of single GaN NW (scale bar: 20μm). Arrow indicates single GaN NW.

Results and Discussions

Fig. 2 shows scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of GaN NWs prepared on the substrate under metallic Ga-NH_3 system. The GaN NWs were distributed over the entire area of the substrate and have diameters in the range of < 100 nm and lengths of several to hundred μm. These GaN NWs were dispersed on transmission electron microscopy (TEM) grids for additional structural and compositional analysis. Fig. 2 (c) and (d) shows TEM images of a single GaN NW. High-resolution TEM observation and selected area electron diffraction (SAED) analysis, recorded along the [001]

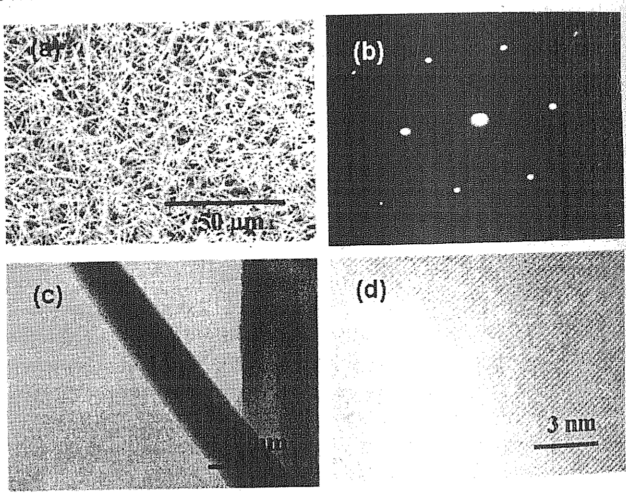

Fig. 2. (a) Scanning electron microscopy (SEM) image of GaN nanowires grown on sapphire substrate. (b) Selected area electron diffraction (SAED) along [001]. (c) Typical TEM image of a single GaN nanowire. (d) High-resolution TEM image of a GaN nanowire.

zone axis, showed that the NWs have wurtzite structures as shown in Fig. 2 (b) and (d). Fig. 3 (a) shows that the X-ray powder diffraction pattern of the GaN NWs was indexed to a hexagonal based wurtzite structure with lattice constants a =0.319 nm and c=0.519 nm. Photoluminescence (PL) of GaN NWs was collected to determine their optical properties. Fig. 3(b) shows a typical PL spectrum from GaN NWs measured at room temperature. The samples were excited with a He-Cd CW laser (wavelength of 325 nm) as excitation source. PL emission peaks were observed at the center wavelengths of 374 nm (3.32 eV in photon energy). Fig. 4 (a) shows a single GaN nanowire on a Si wafer for electrical transport measurement. Fig. 4 (b) and (c) show the current-voltage (I_D-V_{SD}) characteristics of a CVD GaN NW at different gate voltages (from +30V to -10V with 10V step) and the drain current (I_D) as a function of the gate voltage (-20V to +20V) for the GaN nanowire. The current versus source-drain voltage and gate voltage were measured. The nanowire conductance increases for V_G greater than zero and decreases for V_G less than zero, indicating that these nanowires have n-type dopants. From many bulk GaN studies [5,6], this n-type behavior of as-grown un-doped GaN nanowires is due to the contribution of nitrogen vacancies or oxygen impurities and some metal impurities incorporated during the processes. In addition, we have investigated the carrier concentration and carrier mobility in n-type GaN nanowires. In order to estimate the carrier concentration we should calculate the capacitance, $C \approx \pi\varepsilon_0\varepsilon L/\ln(2h/r)$ where h is the dielectric thickness, L is the length, and r is the radius of nanowire with a quasi-circular cross-section approximation. The electron carrier density ($n_e = Q/e\pi r^2 L$) is estimated to be $\sim 10^{19}$ cm^{-3}. The carrier mobility (μ) for our nanowires is on the order of 60~70 $cm^2/V\cdot s$ from the transconductance of the GaN nanowire back-gated FET.

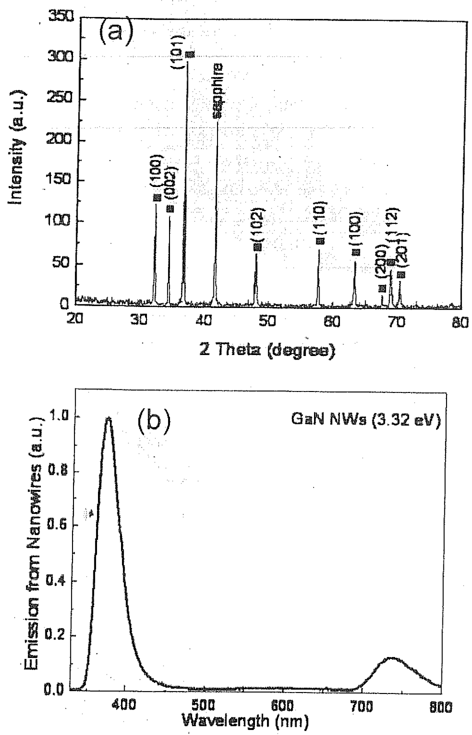

Fig. 3. (a) X-ray diffraction spectrum of GaN nanowires. (b) PL spectra of GaN nanowires excited with the 325 nm line of a He-Cd CW laser at room temperature.

Conclusion

In conclusion, we successfully demonstrated a novel and expedient approach which is a powerful technique for extracting the electrical properties of semiconductor nanowires because the measurement can be performed in the whole wafer and can fabricate large amount of semiconductor nanowires devices on the whole wafer.

Acknowledgment

This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD) (KRF-2004-041-C00118)

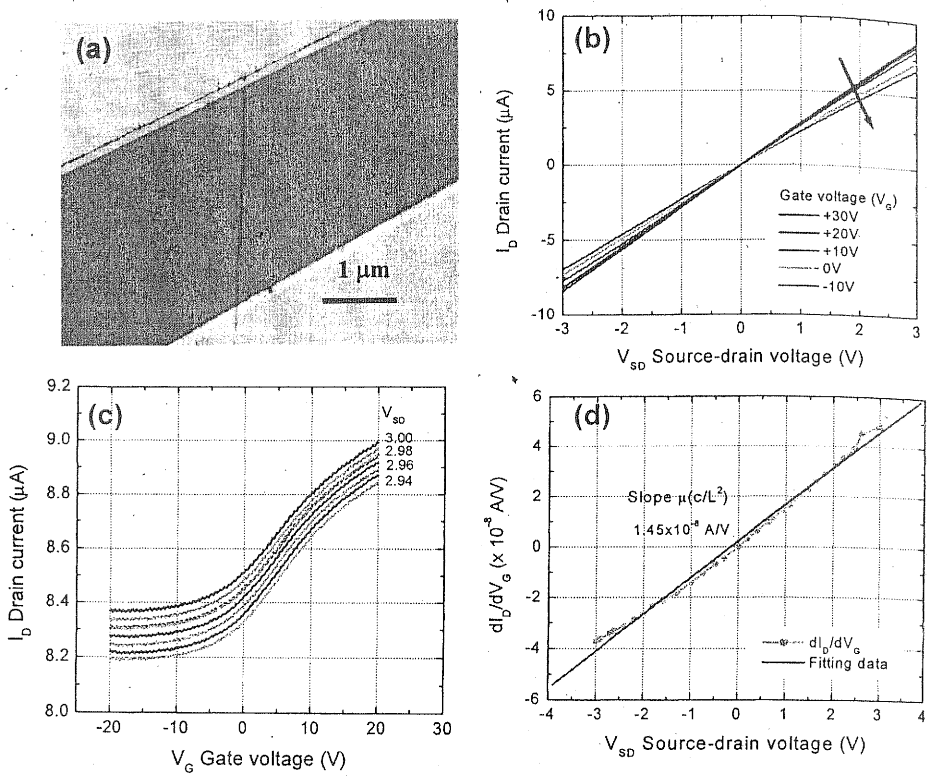

Fig. 4. (a) SEM image of single GaN nanowire, (b) Gate voltage dependent I_D-V_{SD} data recorded on single GaN nanowire (80 nm radius, 3.1 µm length) shown in Fig. 3(a). (c) Drain current (I_D) as a function of the gate voltage (V_G) at different source-drain voltage (V_{SD}). (d) dI_D/dV_G as a function of source-drain voltage (V_{SD}) for estimating the mobility and carrier concentration.

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