SILICON-ON-INSULATOR: A HIGH PERFORMANCE APPROACH TO ULSI TECHNOLOGY

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Silicon-on-insulator MOSFET'S are of three types: partially depleted, fully depleted, and accumulation mode devices. Two-dimensional numerical modeling has been used to explore the physics of these devices, especially the reduced short channel effects, and the operating differences between them. Experimental data is presented for circuits fabricated with these devices. Fully depleted CMOS circuits with 1μm effective gate lengths, operating at 5V, showed stage delays of 58ps and speed power products of 1.5fJ.

INTRODUCTION

Over the past several years, much work has gone into the perfection of silicon-on-insulator (SOI) substrates for high performance circuit applications. The benefits of SOI for a high performance ULSI CMOS technology include low parasitic capacitance, complete device isolation, and greatly reduced short channel effects compared to bulk technology. In this paper we will show how beneficial SOI technology can be in improving short channel and two-dimensional effects in submicron devices.

There are three principal thin film transistor (TFT) structures that can be realized on SOI substrates. These are the partially depleted (PD) TFT, the fully depleted (FD) TFT, and the accumulation mode (AM) TFT which has previously been used in silicon-on-sapphire technology, a subset of SOI, to gain enhanced performance (1). These three devices will be discussed and their performance assessed both experimentally and using the 2-D device simulator PISCES (2).

SUBSTRATE PREPARATION

The substrates used in this work were prepared by the Separation by IMplantation of OXygen (SIMOX) technique (3). The starting material was N- or P-type <100> silicon with a resistivity ranging from 4 to 10 Ω-cm. The oxygen implant was carried out on an EATON NV-200 high current implanter into bare silicon with a dose of 1.5×10^{18} O^+/cm^2 at an energy of 200 keV. During the implant, the wafers were maintained at an elevated temperature of approximately 550 to 600°C (4).

After implantation, the wafers were coated with a 3000Å thick chemical vapor deposited SiO_2 layer, required to protect the silicon

surface from reaction with the ambient during the high temperature anneal. The implanted wafers were then given a 1350°C 6 hour anneal in N_2 to remove any residual oxygen and crystalline defects in the SOI film. Finally ,the SiO_2 protective cap was stripped to produce the finished SOI substrates.

Figure 1 shows transmission electron micrographs (TEM'S) of the as-implanted and fully annealed SOI substrates. For the energy and dose parameters used in this work, the buried oxide thickness was 3500Å with a silicon film thickness of 1600Å. The residual defect density was found to be sensitive to the implantation conditions used in the SIMOX process (4). The threading dislocation densities were measured by plan view TEM and were found to be as low as $8\times10^5/cm^2$ using this technique.

DEVICE FABRICATION

CMOS devices were fabricated on the SOI substrates in a modified 1.5μm process. The SOI silicon films were first thinned by a wet oxidation process to a desired starting thickness, chosen so that the final thickness of the channel region of the finished device could be varied from 500 to 1000Å. A LOCOS process was then used to define the device well and oxidize away the silicon film down to the buried oxide layer, thus providing complete dielectric isolation of the devices. This process resulted in an effective field oxide of 6000Å. The surface was cleaned using a wet pre-gate oxidation and strip followed by a 200Å gate oxidation.

Threshold adjust implants of boron and phosphorous were carried out into the appropriate device wells. In the case of the P-channel AM transistors, there was no threshold adjust to the film, to ensure that the device would be normally off. Undoped amorphous silicon was then deposited to a thickness of 2500Å and patterned. The S/D implants, done with As^+ and BF_2^+, were used to simultaneously dope the silicon gate electrode associated with each enhancement mode transistor. This procedure resulted in an N^+ gate on the N-channel transistor and a P^+ gate on the P-channel transistor. For the wafers with AM P-channel transistors, in situ doped N^+ polysilicon was used for both gates. The SOI wafers were then given a rapid thermal anneal to activate the implants and to increase the grain size in the polycrystalline silicon gate electrodes. Further optimization of the source/drain junction formation process should be possible as we have found that lateral diffusion of dopants seems to be somewhat enhanced compared to that found in bulk technology, probably because the buried oxide and the surrounding field oxide are excellent diffusion barriers to the most commonly used dopants.

To remove the lateral N^+/P^+ diode that existed between the gate electrodes, and to reduce the resistance in the very thin S/D regions, a $TiSi_2$ salicidation was used (5). A side wall spacer (SWS) was formed

and then 300Å of Ti was deposited. In some cases, the resulting salicide encroached under the SWS leaving a very short heavily doped S/D junction. The thickness of the salicided S/D regions was as little as 580Å for the 1000Å devices. The remainder of the process was indistinguishable from bulk processing, using Al/1%Si interconnect to wire the circuits. Figure 2 shows a TEM cross section of a thin film SOI MOSFET with salicided gate and source/drain regions. Careful examination of the source/drain region of this micrograph shows a change of contrast in the silicon under the SWS. This contrast change can be attributed to a mass difference between the material under the gate and the silicon out in the source/drain region.

EXPERIMENTAL RESULTS

Threshold voltage - For a TFT in which the silicon film thickness is greater than the gate induced space charge layer, there will be a charge neutral region within the silicon film. If this is the case, then it is expected that the threshold characteristics of this device will be similar to those of a bulk transistor with the threshold voltage described by the classic relation (6):

$$V_T = V_{FB} + 2\phi_B - Q_D/C_{ox}, \qquad (1)$$

where V_{FB} is the flat band voltage, ϕ_B is the bulk (substrate) potential, Q_D is the space charge density in the depletion region, and C_{ox} is the gate oxide capacitance.

For thin films that are fully depleted, the doping concentration must be much greater than that of the silicon substrate in order to overcome the ϕ_{ms} term in Eq. 1. The back interface of the silicon film is assumed to be at or very near flat band with respect to the substrate, since the majority of the band bending due to the substrate/silicon film work function difference will appear in the lightly doped substrate. If the silicon film thickness is less than that of the gate induced depletion layer, there will be no neutral region in the film. Under these conditions, the silicon film is fully depleted. The depletion charge is no longer determined by the total band bending at the front surface of the film but is now limited by the thickness of the silicon film and the charge on the buried oxide. The threshold voltage of the fully depleted silicon film should therefore be smaller than that of a comparable bulk or partially depleted device.

Threshold voltage for the fully depleted case is then:

$$V_T = (1+\alpha)(V_{FB} + 2\phi_B) - qN_At_{Si}/\alpha C_{ox} - qN_At_{Si}/2C_{Si}, \qquad (2)$$

where $\alpha = C_{box}C_{Si}/C_{ox}(C_{box}+C_{Si})$, C_{box} is the capacitance of the buried oxide, C_{Si} is the capacitance of the fully depleted silicon film, N_A is the acceptor concentration, and t_{Si} is the silicon film thickness.

Since α is small, the threshold voltage varies approximately linearly with the film thickness for a fixed and uniform doping. Figure 3 shows the results of PISCES simulations on long channel devices and, as expected, the threshold voltage of the thin film decreases as the film thickness is reduced. In the limit of the film thickness tending to zero, the threshold voltage of the film is independent of the film doping (7).

The fabrication of an N-channel enhancement mode device in the thin film using N^+ poly gates can pose some problems as shown in Figure 4. The N^+ gate of an N-channel enhancement mode device will tend to cause the surface of the channel to invert, thus turning the device on. To increase the threshold to a usable value, the channel doping may be increased through implantation.

The P-channel enhancement mode device, on the other hand, will have its surface accumulated by an N^+ gate, resulting in a large negative threshold. To increase this threshold voltage and make it symmetric to the N-channel device, the surface doping concentration must be compensated to some degree making the device very susceptible to short channel effects, punch through, and threshold voltage instabilities. However, if instead of an N^+ polysilicon gate, a P^+ gate is used, then symmetry is achieved, with the surface of the P-channel device inverted and turned on. To decrease the threshold voltage and turn the device off, the channel impurity concentration is simply adjusted to the appropriate level as in the N-channel device.

The second alternative to work function control for the P-channel transistor is the use of N^+ polysilicon to form an accumulation mode device. From Fig. 4, we see that the surface of a P-type lightly doped semiconductor is brought into inversion by the work function potential of the N^+ gate alone. If the impurity concentration and the film thickness are chosen such that the P-channel film is fully depleted when the bias on the gate is zero, the device will be off. As the bias is increased in a negative sense, the surface of the channel will become accumulated and current will now flow between the P^+ source and drain. The advantage of the AM device is that the channel impurity concentration required to set the threshold voltage is relatively low ($1\times10^{16}/cm^2$); therefore the mobility degradation due to ionized impurity scattering should be significantly reduced from that of the FD enhancement mode P-channel.

As the gate length is reduced below 1μm, short channel effects show up, such that the ability to control the channel current with the gate is degraded. In bulk devices the gate charge is partitioned between the inversion charge and the depletion space charge. As the dimensions are reduced, the space charge associated with the source and drain junctions starts to become comparable to the gate space charge and the threshold decreases. Figure 5a shows the effect of this charge sharing between bulk and thin film devices.

To study the threshold stability of thin film structures, fully depleted enhancement mode N- and P-channel devices were fabricated along with bulk transistors, processed without the use of an LDD drain structure. This procedure was followed to highlight the ease of fabrication of the SOI devices as the gate length is reduced to submicron values. The measured threshold voltages are shown in Figure 5b. The bulk devices have started to loose V_T control at gate lengths below 1.0μm while the SOI devices have not really started to show significant degradation at 0.5μm.

Subthreshold slope - The subthreshold slope of MOS devices is a figure of merit that describes the gate voltage swing required to change the drain current by one order of magnitude (8). If, for example, we have a device with a subthreshold swing of 90mV/decade and the standby current is to be 10^{-7} times the current at threshold, then the threshold voltage of the transistor must be at least 0.63 volts. By definition, the subthreshold slope is measured below the threshold voltage of the particular device when the semiconductor surface is in a state of weak inversion. The subthreshold slope is then defined by (8):

$$S = (kT/q)\ell n10\cdot(1+C_D/C_{ox}), \qquad (3)$$

where C_D is the depletion capacitance in the silicon at the onset of weak inversion. The subthreshold characteristics of a partially depleted thin film transistor will be similar to those of a bulk device because the maximum depletion capacitance associated with the surface potential will be supported by the silicon film. A thin film fully depleted transistor can, however, offer a significant reduction in S.

If the silicon film is fully depleted at the onset of weak inversion, then the capacitance associated with the depleted region will consist of the buried oxide capacitance in series with the depleted film capacitance. The capacitance due to the space charge layer in the substrate can be ignored. The subthreshold slope is now given for a FD silicon film as:

$$S = (kT/q)\ell n10\cdot(1+\alpha). \qquad (4)$$

If the film is sufficiently thin so that it is fully depleted well below threshold, then the value of S observed is indeed quite low, on the order of 62 to 70 mV/decade for N-channel and 68 to 75 mV/decade for P-channel devices. Subthreshold slopes as low as 29 mV/decade have been observed for volume inversion MOSFET's; however these devices would be difficult to operate in a circuit (9).

The subthreshold slope of an accumulation mode device can be examined in exactly the same fashion. When the accumulation mode device is off, the silicon film is completely depleted and no current can flow. To turn the device on, the gate is biased such that the surface potential is reduced toward flat band. As the surface

potential approaches V_{FB}, the space charge region no longer fully depletes the silicon film and the device starts to turn on. When flat band is reached, the entire volume of the silicon film is conducting and any further decrease in ϕ_S drives the surface into accumulation where the surface charge density will vary exponentially with ϕ_S. At flat band, the depletion capacitance is given as the Debye capacitance, and for the thin structure considered here the Debye length can be greater than the thickness of the silicon film. The Debye capacitance is therefore in series with the buried oxide capacitance and using eq. 4 a calculated value for S of 70.1 mV/decade is expected. The observed substhreshold slope was 67 mV/decade in P-channel accumulation mode devices with a threshold voltage of -1.15V.

Drain characteristics - Several authors have reported on the drain characteristics of thin film MOSFETS (10),(11),(12). It has been shown that the analytical expression for the drain current in the FD case can be simplified from that of an ideal bulk device, given by (8):

$$I_D = \mu_N C_{ox} \frac{W}{L}\left[(V_G - 2\phi_B - V_D/2)V_D - \frac{2(2\epsilon_{Si} q N_A)^{1/2}}{3\ C_{ox}} \cdot [(V_D+2\phi_B)^{3/2} - 2\phi_B^{3/2}]\right]. \quad (5)$$

The second term in Eq. 5 represents the depletion charge under the gate associated with the drain. In the case of a bulk device, the drain space charge region can expand out under the gate and down into the substrate to result in a considerable net charge. From Gauss's law and charge neutrality considerations, the charge on the gate must equal the total of the inversion layer charge and the space charge under the gate. The effect of this drain space charge region is to increase the bulk space charge in the substrate and to reduce the inversion layer charge as one moves from the source to the drain.

In a FD SOI film, the space charge under the gate is more or less constant, fixed by the film thickness. With less of the gate charge needed to support the substrate depletion layer, there should be more charge for the channel and a higher drain current. As well, the surface electric field will be reduced (13), resulting in less surface scattering of the channel carriers and a spreading out of the inversion layer into the bulk of the thin film. All of these factors should contribute to higher drive currents for FD MOSFET's.

Another aspect of the thin film devices that should not be overlooked is the reduction of the 2-dimensional effects found in the bulk. As the gate length is reduced, the potential distribution in a bulk device starts to depart from the gradual channel approximations used in the derivation of Eq. 5. In the thin SOI device, on the other hand, the silicon film is only 500 to 1000Å thick. If the gate length is 0.5μm long, then the SOI device is at least 5 times as long as it is thick and is still effectively a 1-dimensional structure. From

electrostatic considerations, having a thin film of high permittivity silicon on top of a low permittivity oxide causes the field from the drain to extend out into the oxide, thus keeping the potential lines in the silicon near the drain very planar and one-dimensional. An example of this effect is shown in Fig. 6. The two-dimensional aspect of the potential contours in the bulk device contrasts with the well-behaved contours near the drain of the SOI transistor.

If an analysis similar to that done for the bulk case is carried out on a FD SOI device, taking into account the buried oxide layer, the following expression for the drain current is found:

$$I_D = \mu_N C_{ox} \frac{W}{L}(V_G - V_T - (1+\alpha)V_D/2)V_D, \quad (6)$$

where α is defined as before. For the ideal case where the depletion charge is assumed constant, α is equal to 0. In the case of the SOI devices in question, α is 0.052. The significance of this departure from 0 represents the charge present on the buried oxide layer at the drain end of the device.

In order to see experimentally this reduction in charge and hence the increase in drive, the drain characteristics of a thin film device were compared to those of a bulk device. In this comparison, the devices had been processed simultaneously and were therefore biased relative to their threshold voltages. Fig. 7 shows that the drive of the SOI device is larger than that of the bulk device. Simulations using SUPREM3 show that the channel surface impurity concentration in both devices was $1\times10^{17}/cm^2$ (14). The mobility of carriers in the channel region is affected by ionized impurity scattering and the normal electric field (8). Since the first effect is common to both, the difference in current is due to the reduction of the normal electric field and surface scattering effects.

In the PD FET, the presence of the neutral region under the gate means that there is a larger lateral electric field in the silicon film. This field causes an increase in the weak avalanche generated hole-electron current at the drain. For an N-channel device, the holes generated near the drain are acted on by two fields. The gate field repels the holes to the lower silicon interface where they flow down the drain potential barrier to the point of lowest potential in the structure, in this case the neutral region. This charge collects here because of the barrier at the channel/source junction, thus raising the film potential. The result is a body bias effect as the drain voltage is increased and a shift in the threshold voltage causing a kink in the drain characteristics (15),(16).

In the case of the FD FET, there is no neutral region in the silicon film, hence no potential barrier at the source/channel junction. PISCES 2-D numerical modeling of the FD SOI FET shows a

reduction in the lateral electric field along the back of the SOI device. The barrier present in the PD transistor at the source is absent in the FD device. The results of the simulation are shown in Fig. 8, where the neutral region was simulated by biasing the back gate of the structure to -20V. Holes generated at the drain now flow down the potential gradient and out the source. The drain characteristics are no longer effected by the body bias effect because there is no charging of the silicon film. Figure 9 shows drain characteristics of a FD device similar to the device described in the above simulation. A back gate bias of -20V was applied such that a neutral region was formed and the device behaved as a PD transistor. Also shown is the substrate current of holes that is generated at the drain end of the device. In the case of the FD device, the onset of substrate current does not occur until the drain voltage was 1.5V larger than in the PD case. This improvement resulted in less oxide charging due to hot electrons in the FD FET.

The purpose of this paper was to demonstrate the superiority of fully depleted SOI devices over their bulk counterparts for use in ULSI circuits. Figure 10 shows the drain characteristics of a 0.4μm fully depleted N-channel SOI MOSFET. This device has a 200Å gate oxide and no LDD. It shows excellent drain characteristics with the exception of the apparent breakdown at large drain voltages. This increase in the drain current at moderate voltages, once the device is turned on, is not unique to such short channel devices only, but can be seen in long 1.5μm FD SOI transistors. This effect is due to impact ionization and carrier pair generation at the drain end of the FD SOI transistors. From Fig. 10, we see that the effect is most noticable when the gate bias is small and the device saturated. When the device is operated with large gate voltages, the current is confined to the upper half of the film where the lateral electric field is small. With small gate voltages however, the current will spread out towards the back interface of the film where the lateral electric field is the largest. The result is an increase in the impact ionization and the generation of hole-electron pairs within this region, and therefore an increase in the drain current. To confirm this conjecture, PISCES 2-D simulations of the channel current flow and generation rate contours were obtained. The results are shown in Fig. 11 and qualitatively agree with the drain characteristics shown in Fig. 10.

The operation of the AM MOSFET is somewhat different from that of the FD SOI MOSFET. In this device the semiconductor surface is brought into accumulation so that there is no depletion charge associated with the gate induced channel. An analysis to determine the I_D characteristics of the AM SOI device has resulted in the following expression for drain current:

$$I_D = \mu_N C_{ox} \frac{W}{L}(V_G - V_{Teff} - V_D/2)V_D, \qquad (9)$$

where $V_{Teff} = V_{FB} + \psi_s + qN_A t_{Si}/C_{ox}$. (10)

In the simplest model, ψ_s can be taken to be $-E_g/2+\phi_B$. Accumulation mode P-channel MOSFET's were fabricated to demonstrate their functionality and use in circuits. Because of the lower channel doping, they are expected to exhibit higher channel hole mobilities and therefore higher circuit performances. Figure 12 shows a 1μm long P-channel AM transistor fabricated in a 600Å thick SOI film. The device is well behaved and exhibits good saturation with off state currents of 43 fA/μm of width at V_{DS} = -5.0V.

The increase in hole mobility due to the reduction in impurity scattering can be seen from the g_m's of an accumulation mode and an enhancement mode device shown in Fig. 13. Here we see a 90% increase in the peak g_m of a 1μm AM transistor compared to the FD device. The g_m roll off due to the normal electric field is very pronounced in the AM device.

Circuit performance - Ring oscillators were fabricated with FD N- and P-channel devices. The transistors had 1μm effective channel lengths and fully salicided gate, source, and drain regions. The results of ring oscillator frequency vs. back gate bias are shown in Fig. 14. For the oscillator used, the minimum stage delay was 60ps at a supply voltage of 5V. The observed substrate bias effect arises from electrical decoupling of the substrate from the circuit. The substrate used in this case was N-type silicon; therefore as the substrate bias was made negative the surface of the substrate was accumulated and the speed was quite insensitive to bias. For positive bias, the silicon at the substrate surface started to deplete until inversion was reached, at which point the circuit coupling capacitance was a minimum and the oscillator speed a maximum.

Other circuits were fabricated as well. They included inverters, NAND and NOR gates, and J-K flip flops. All of the these circuits functioned as designed and showed no undesirable output characteristics.

CONCLUSIONS

Silicon-on-insulator devices will find increasing use in the ULSI technologies of the future. The ease of fabrication with which the devices can be pushed down into the submicron regime has been demonstrated. High quality devices with gate lengths as short as 0.4μm have been fabricated using a nominally 1.5μm technology. The one-dimensional character of the thin film transistor relieves the device designer of the problems that he will face when dealing with the two-dimensional nature of bulk devices.

The increase in the drive of these FD devices should produce faster circuits. Ring oscillators exhibited speed increases of 3 to 4

times those of the bulk. The ring oscillator represents, however, a situation with minimal interconnect loading of the circuit. In real circuits with appreciable interconnect loading, the ultimate speed improvement will probably be on the order of 2 times. Power consumption will also decrease significantly. With the availability of high quality low defect density SOI substrates, this technology should emerge as a clear winner for the ULSI era and Save Our Industry from the problems associated with the bulk alternative.

ACKNOWLEDGMENTS

We wish to thank Louise Weaver, Dave Mayer, and Rob Bruce for providing the TEM micrographs, and Vu Ho for valuable consultation on silicide formation.

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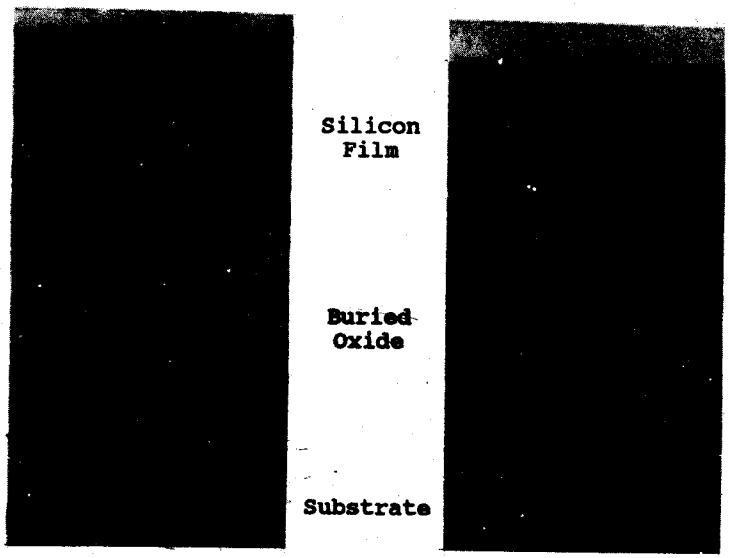


Figure 1. (a) Cross-sectional TEM micrograph of an as-implanted SOI substrate. The implant dose was 1.5×10^{18} O^+/cm^2 @ 150keV with the substrate held at 520°C during the implant. (b) Cross-sectional TEM of the same sample after being annealed at 1350°C for 6 hours in N_2. All precipitates have disappeared, the silicon film thickness has been reduced while the buried oxide layer thickness increased, and the dislocation density was found to be $\sim 8\times10^5/cm^2$.

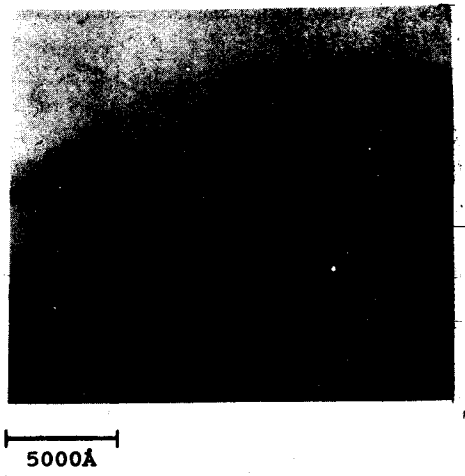


Figure 2. Cross-sectional TEM of a finished SOI thin film device. The gate oxide is 220Å and the silicon film thickness under the gate is 900Å. The complete salicidation of the source/drain region can also be seen.

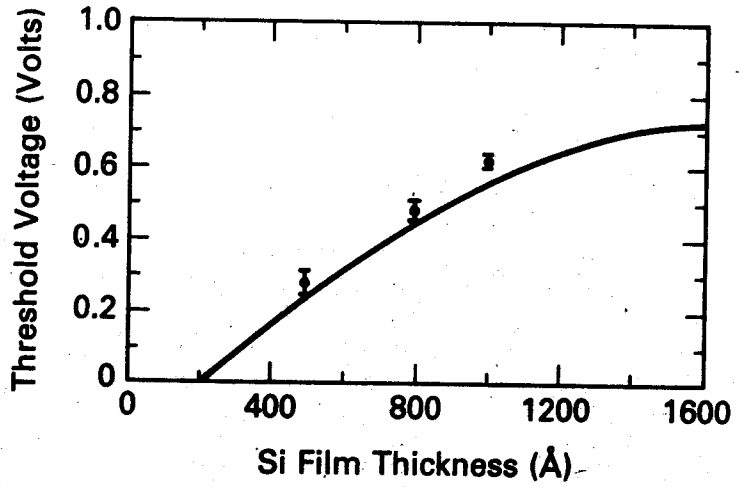


Figure 3. Simulated and measured threshold voltages of thin SOI devices. The devices had a 200Å gate oxide with N_A=8x10^{16}/cm^3 and the back gate bias was held at 0V.

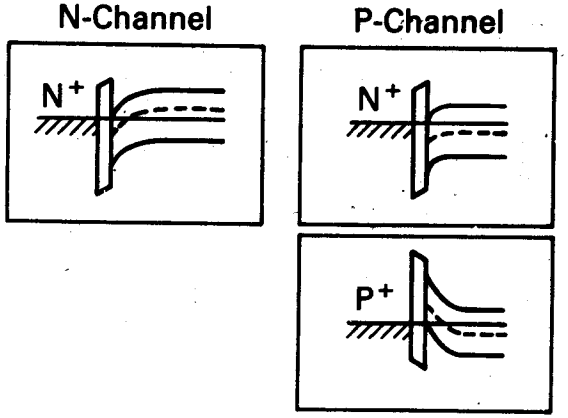
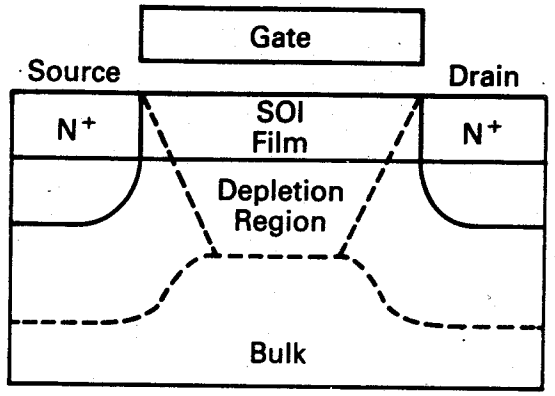
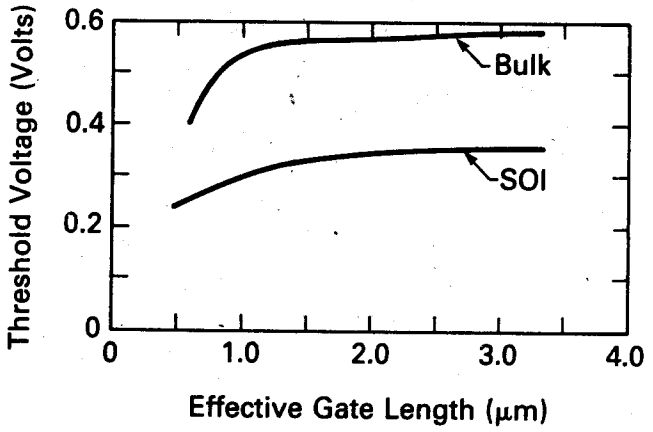


Figure 4 Band bending at the semiconductor surface due to differences in the work function of the gate.

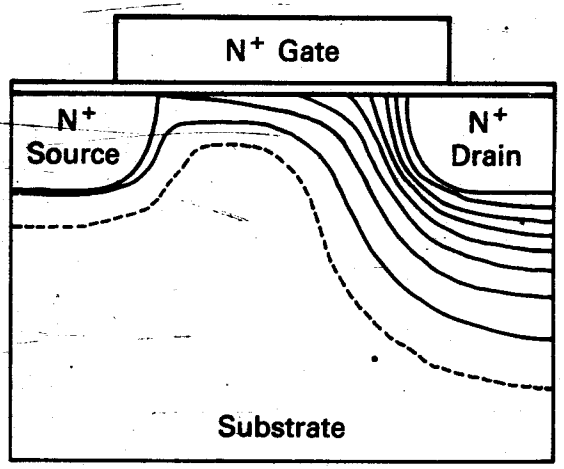


(a)

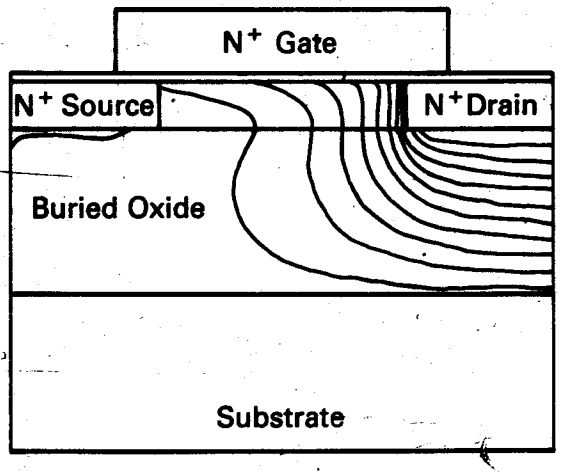


(b)

Figure 5. (a) Threshold instability due to charge sharing between the gate and the junctions in a bulk device. The thin silicon film of the SOI transistor reduces this effect. (b) The SOI FD transistors show a reduced short channel effect compared to bulk devices when the gate length is reduced below 1μm.



(a)



(b)

Figure 6. (a) PISCES simulation of equal potential contours in a 0.6μm bulk device. The 2-dimensional aspect of the potential near the drain is quite evident. (b) SOI simulation of a 1000Å thick silicon film. The potential contours are very planar near the drain but extend out under the channel in the buried oxide.

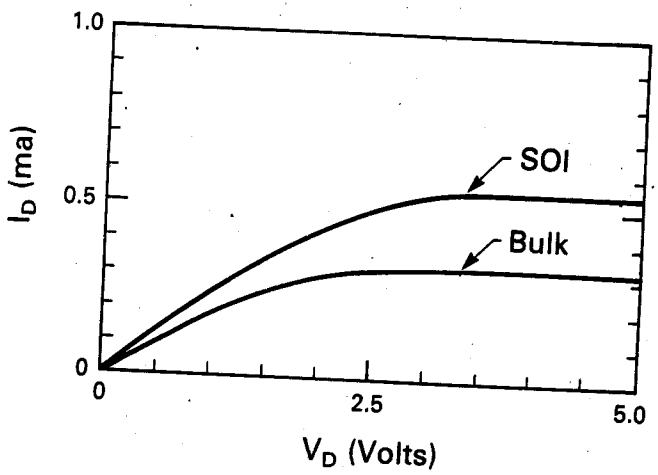


Figure 7. Increase in the drain current of a FD SOI device. To make the comparision, the bulk and SOI transistors were biased up with respect to their threshold voltages. The peak impurity concentrations in the channel regions of both devices were estimated to be ~$1\times10^{17}/cm^3$.

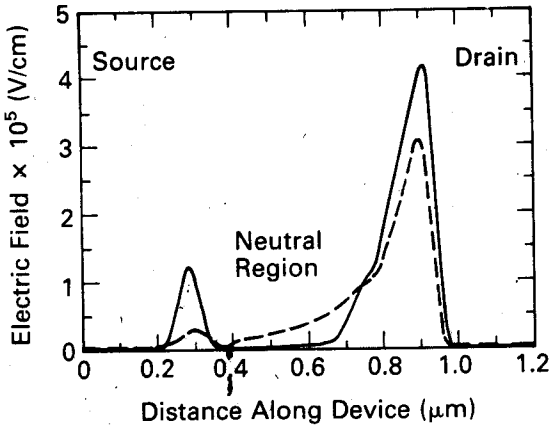


Figure 8. PISCES simulation showing the lateral electric field at the back of the SOI film for a FD and a PD device. The silicon film is 1000Å thick and normally fully depleted. The neutral region was generated with a back gate bias of -20V.

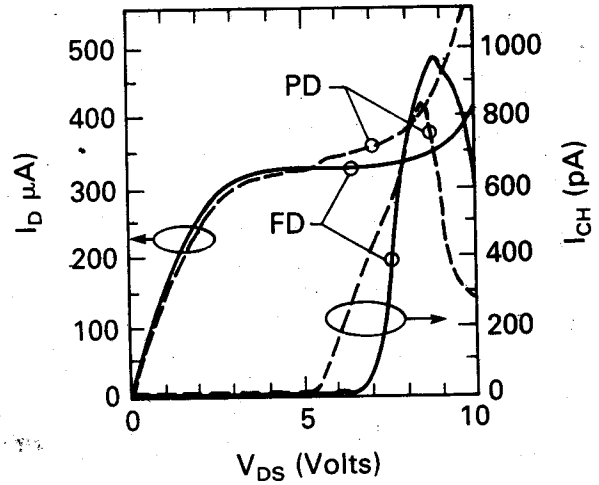


Figure 9. SOI device biased as a FD and a PD transistor to show the kink effect in the drain current (I_D) as well as the increase of the hole current (I_{CH}) due to impact ionization near the drain.

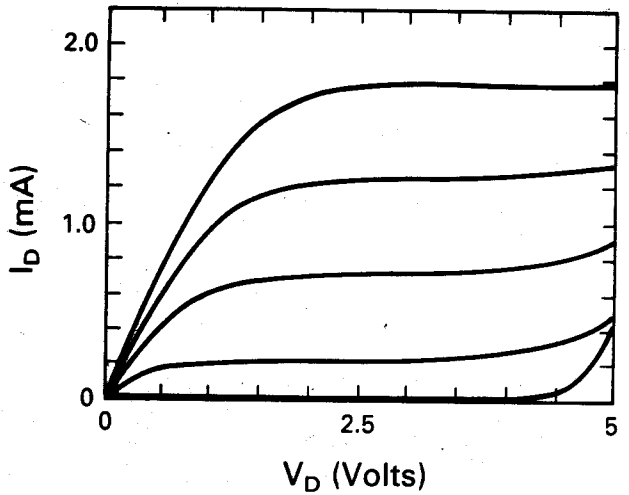


Figure 10. Drain characteristics of an N-channel FD thin film transistor with a gate length of 0.4μm. The silicon film thickness is 800Å and the gate voltage was varied from 0 to 5 volts.

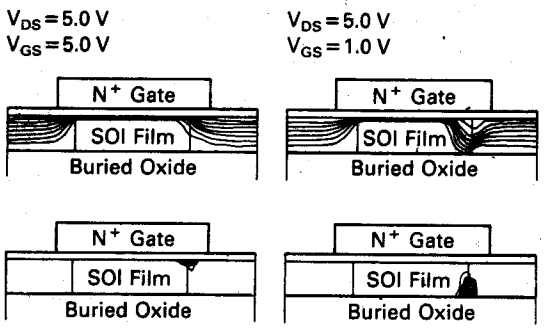


Figure 11. PISCES simulation of current flow (top) and electron-hole generation (bottom) in a thin film FD transistor. (a) The device is biased with V_G = 5.0 V and V_{DS} = 5.0 V. Peak hole-electron pair generation occurs at the gate oxide/silicon film interface. (b) The same device with the gate biased at 1.0 V. Here the current has spread out towards the lower oxide interface and a region of higher lateral electric field. The region of pair generation has also moved towards the back interface and the generation rate has increased.

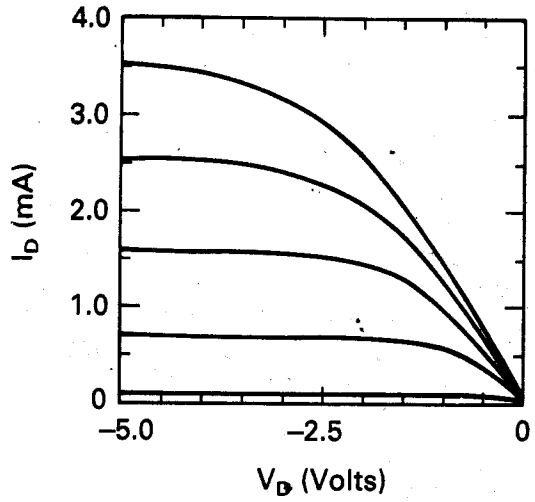


Figure 12. Drain saturation charasteristics of a 1.0μm AM P-channel transistor for gate voltages from 0 to -5 volts. The thickness of the silicon film was determined to be 600Å from C-V measurements.

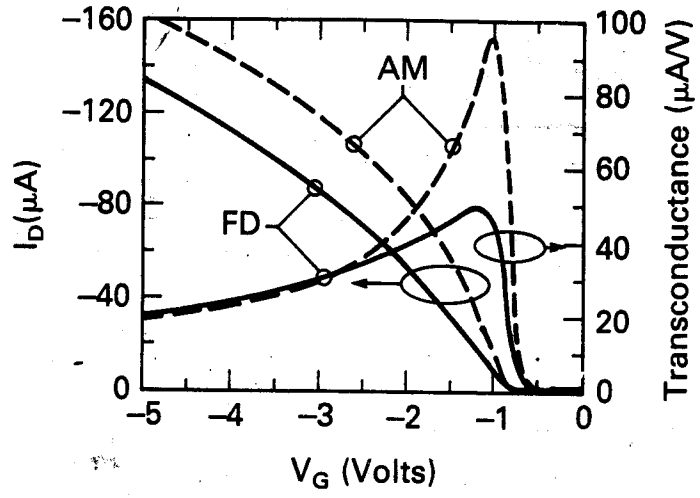


Figure 13. Transconductances for 1.0μm AM and FD mode thin film P-channel transistors. The AM mode device has a 90% increase in peak g_m over the FD mode device.

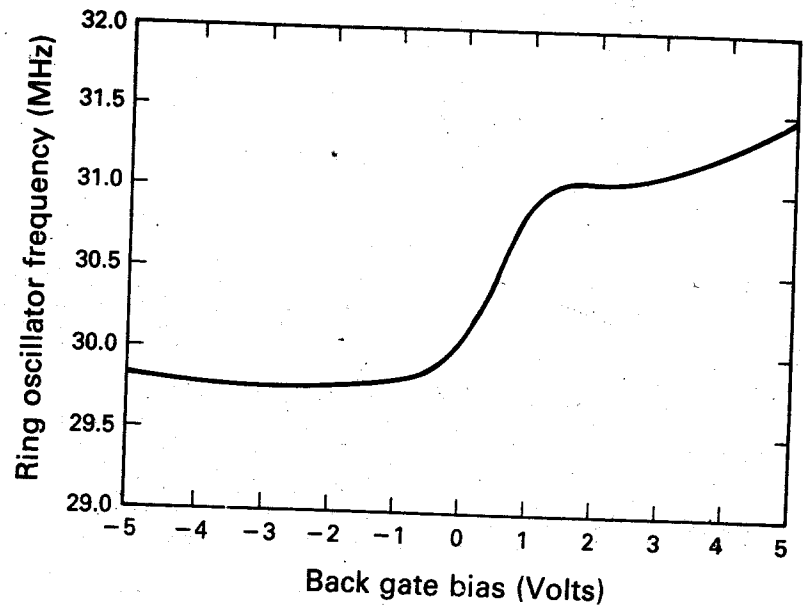


Figure 14. The effects of a back gate bias on the oscillating frequency of a lum CMOS SOI ring oscillator. The minimum stage delay was found to be 58 ps with V_{DS} = 5.0 V.

THIN-FILM SIMOX-CMOS TECHNOLOGY FOR ULSI APPLICATIONS

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The use of thin-film SOI, and more particularly SIMOX wafers, allows one to avoid numerous problems associated with deep-submicron CMOS technology. Utilization of such substrates facilitates processing and reduces or eliminates parasitic effects such as latch-up, short-channel threshold voltage roll-off and hot-electron degradation.

I: INTRODUCTION

Silicon-on-Insulator (SOI) technology offers significant advantages over bulk silicon technology once deep-submicron applications are considered. Traditionally, SOI technology has been considered as a replacement for Silicon-on-Sapphire (SOS) and Dielectric Isolation (DI) processes, both of which are primarily used for space and defense applications. Indeed, SOI MOSFETs offer good immunity to single-event upsets (SEU) and to gamma-ray induced photocurrents, owing to the small volume of silicon in which devices are made.[1] Because of the dielectric isolation between devices, latch-up is also ruled out. Operation at extreme temperatures is also facilitated by the absence of p- (or n-) well junctions, which are known to be the major source of leakage current under high temperature operation.[2]

There are various techniques which can be used to produce SOI material, each having its advantages and a preferred field of application. Apart from heteroepitaxial techniques such as SOS, laser and e-beam recrystallization of a polysilicon layer deposited in silica have been the first SOI-producing techniques, and are still used in applications where thermal budget is of great concern, and where thermal energy can only be deposited at the surface of a wafer. Japan is currently leading the way in such techniques, and impressive three-dimensional circuits have been demonstrated.[3,4] A larger molten area, and hence a higher throughput can be obtained when lamps or strip heaters are used to melt and recrystallize the silicon film.[5,6] Wafers produced by such Zone-Melting-Recrystallization (ZMR) techniques are commercially available. Other techniques, such as Full Isolation By POrous Silicon (FIPOS) and wafer bonding look promising in the field of bipolar or high-voltage dielectricaly isolated devices.[7,8]

II: THIN-FILM SIMOX

Separation by Implantation of OXygen (SIMOX), was invented by Izumi et al. of NTT, Japan, in 1976, and a 1K SRAM made in this material was demonstrated in 1982.[9] The technique is now used to produce radiation-hard 16K and 64K CMOS SRAMs by companies such as TI, Harris and Leti. Early SIMOX material contained dislocation densities as high as 1E9 cm-2, as well as oxide precipitates in the silicon film. Research efforts were concentrated on improving the quality of the material, and both implantation and post-implant annealing conditions were optimized.[10,11] Current SIMOX material can be commercially obtained with dislocations densities on the order of 1E3 cm-2, no oxide precipitates and a film thickness control better than 3 nm. The improvement of dislocation density has recently made fabrication of SIMOX bipolar circuits possible.[12]

One unique feature of SIMOX technology is that it can produce thin silicon films (100 nm) with good control of thickness uniformity (a few nanometers). By contrast, it is difficult to obtain uniformities better than several tens of nanometers with ZMR and bonding techniques. While it is easy to understand why good control of film thickness is desirable, it may not be obvious why the use of such thin films may be attractive.

III: CMOS PROCESSING IN THIN SIMOX FILMS

A cross-section of an MOS transistor fabricated in a 100 nm thick SIMOX film is presented in Figure 1. The device was not realized in state-of-the-art, low dislocation material. Because the thin-film nature of the film, S&D junction depth is self-limited to the thickness of the film in such a way that shallow juctions are easiliy obtained. Moreover, any possible reaction between silicide or metal contact to the junction will be stopped at the Si-buried oxide interface and will, therefore, create no leakage current. Junctions can also be silicided all the way down to the buried insulator.[13] Unlike in bulk technologies, where sophisticated isolation technologies must be used (trench, selective epi,...), submicron thin-film SOI (TFSOI) devices can still make use of well-established isolation techniques such as mesa or LOCOS. Indeed, in the case of LOCOS, the bird's beak encroachement is on the order of the the thickness of the grown oxide, which is only 100 nm in the case of a fully-recessed LOCOS grown from a 100 nm-thick Si film. Mask and process step counts are also reduced (there is no need for creating wells). In other words, one could say that part of the complexity of the front-end process has been simplified, and the price paid for it is the wafer engineering effort which has been spent to produce high-quality SOI wafers. Unlike SOS wafers, SIMOX wafers contain only silicon and SiO2, and are not transparent. They are compatible with standard CMOS processing lines.