The Insulated-Gate Field-Effect Transistor —A Bipolar Transistor in Disguise

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Abstract—Straightforward physical arguments show that when the IGFET specific gate capacitance is increased, such as by decreasing insulator thickness or by increasing the dielectric constant, device performance will change toward the low impedance, high transconductance characteristics uniquely typical of bipolar transistors. At relatively large specific capacitances, the characteristics become remarkably similar to those of bipolar transistors. The analysis shows that there is a fundamental trade-off between impedance level, transconductance, transconductance/current ratio, and power gain in IGFET's. The high input impedance uniquely typical of the IGFET stems from the gate–insulator capacitance and not from any unique behavior of field-effect action.

An explanation is given for the previously unexplained limiting value of **e/KT** experimentally observed for the transconductance/current ratio at low IGFET drain currents. Modification is suggested to correct existing IGFET theory, which incorrectly predicts unlimited increase in the transconductance/current ratio as the specific gate capacitance is increased.

The above results are derived from the behavior of the high/low dynamic junction that connects the source and channel, a junction that has the **e/KT** behavior of the emitter/base junction in the bipolar transistor, and whose presence and behavior seem to have been generally unappreciated. One interesting consequence of this junction is that it results in a dynamic control capacitance identical in form and magnitude to that of the diffusion capacitance in the bipolar transistor.

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Introduction

Although both the Insulated-Gate Field-Effect Transistor (IGFET) and the bipolar transistor operate on charge-control principles,[1,2] these devices are widely believed to be intrinsically different in the details of their operation.[3] On the one hand, the bipolar transistor is characterized as a device with a perfect e/kT control action that results in a high transconductance, a transconductance/current ratio that reaches the theoretical maximum value of e/kT, and a low input impedance that is caused in a large measure by the shunting action of a dynamic capacitance known as the diffusion capacitance. On the other hand, the IGFET is widely characterized as a device having a relatively low transconductance that is somewhat akin to that of a vacuum tube,[2] a transconductance/current ratio that is in practice well below the theoretical limit e/kT, and a relatively high imput impedance. Conventional IGFET theory,[3] however, does predict a transconductance/current ratio that approaches infinity as the gate-insulator capacitance is made arbitrarily large as, for example, by making the insulator thickness approach zero in value. This prediction seems intuitively incorrect. At least it is at marked variance with the behavior of other charge-control devices such as the bipolar transistor and vacuum tubes.[2-4]

The following analysis was inspired by three items. The first of these was the interesting experimental observation that field-effect transistors universally exhibit a transconductance/current ratio that closely approaches e/kT in value as their drain currents are decreased to low values.[5] As far as the author can tell, no detailed explanation of this unexpected result was ever given. The second item is the intuitively incorrect result predicted for the transconductance/current ratio by conventional IGFET theory. If it were true that this ratio approached infinity with decreasing gate-insulator thickness, the IGFET would be a most unusual device indeed![4] The third, and potentially most important item, is the extant implication that IGFET devices are restricted to relatively lower transconductances than bipolar transistors and thus suffer a basic speed disadvantage, particularly in digital integrated circuits[6] wherein load and stray capacitance driving capability must be considered in addition to the usual device measures of frequency performance, for example, the current gain cutoff frequency F_T.

IGFET Potential Distribution

Simple physical arguments added to the classical picture of IGFET behavior lead one to believe that the source–drain potential distribu-

tion existing within a few kT/e potential units of the silicon–insulator interface is as shown in Fig. 1. Here, the gate is biased to create an inversion channel and the device is operating in drain saturation. The point of particular interest in this paper is the potential barrier V_s that must exist in the source–channel interface region to balance the large charge-density difference across this interface. The many consequences of this will be described below.

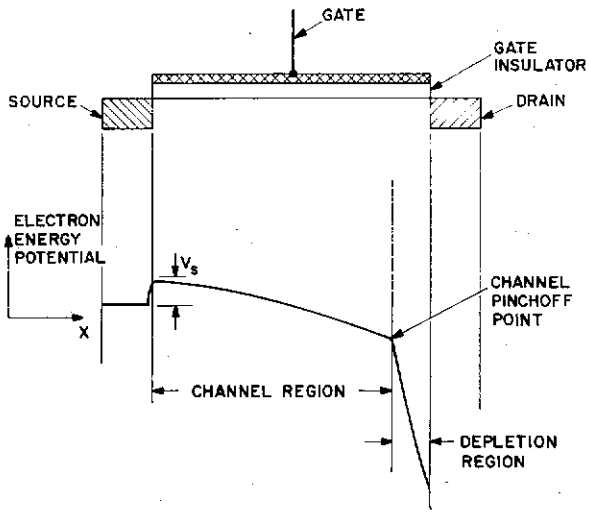

Fig. 1—General form of the source–drain potential distribution in an n-channel IGFET operating in drain saturation.

The potential decrease along the channel shown in Fig. 1 is due to the IR drop caused by the load current and channel resistance. The pinch-off point is reached when the net voltage across the gate insulator falls to zero. A depletion region exists between this point and the drain. The striking general similarity to the emitter–collector potential distribution in the typical bipolar transistor is to be noted. Similarities in the channel–drain region, such as the Early effect, have been noted elsewhere.[7] One presumes that other similarities exist, such as "channel widening", corresponding to bipolar base widening, and also a complex mixture of both field and diffusion flow in the channel,[8] as in the base of the bipolar device.

Let us now consider the small but important potential barrier V_s in more detail.[9] The charge density induced in the conducting channel of an IGFET is at least a few orders of magnitude smaller than the dopant charge density in the usual source electrode. Accordingly, just

as at the emitter–base junction in the bipolar transistor, the carrier densities across the source-channel interface can be connected by a Boltzmann relation:

$$\frac{n_c}{n_s} = \exp\left(\frac{-eV_s}{kT}\right). \qquad [1]$$

For an n-channel device n_c is the electron density on the channel side of the interface, n_s is the electron density on the source side, e is the electron charge, V_s is the previously noted barrier potential of Fig. 1, k is Boltzmann's constant, and T is the absolute temperature of the region in question. An analogous relation holds for p-channel devices. For our purposes Relation [1] will be considered meaningful down to one inversion channel depth, that is, a few kT/e potential units from the semiconductor–insulator surface interface. Since carrier densities in both the source and channel regions generally vary with depth from the surface interface, the potential V_s will in general vary with depth. This detail should not affect the general conclusions of this paper and for simplicity we shall assume a single average value of V_s.

A further detail to be noted is that the source–channel barrier is a high/low junction in contrast to the pn-junction at the emitter–base interface in the bipolar transistor. A high/low junction is more ohmic in behavior than a p-n junction and thus need not produce an offset effect near the origin of the I-V characteristic, as is typical of bipolar transistors but not of field effect devices.

Potential Distribution in the Input Circuit

In IGFET devices of conventional design, virtually all of the input voltage applied between the gate and source electrodes appears across the gate insulator. One electrode of the gate-insulator capacitor is the gate electrode, and if we neglect stray capacitances and edge effects, the other electrode is the conducting channel itself. This channel returns the circuit to the source through the previously cited high/low junction. Under both dc and ac operating conditions the potential V_s across this junction is in series with the voltage across the gate insulator and any IR drops that may appear in the input circuit. These resistive drops act in much the same way as the base and emitter series resistance in the input circuit of the bipolar transistor; the potential V_s acts in almost exactly the same way as the potential across the emitter-base junction. All mobile load-current carrying charges

that traverse the active region of the device must first climb a kT/e-type potential barrier to be "activated" for use in the load path.

If the device input voltage is increased to increase the inversion charge in the channel, the potential V_s must decrease according to Eq. [1] to account for the new charge-density ratio across the junction. A change in V_s of several kT/e potential units can account for a relatively large change in channel inversion charge and so is not normally noticed in the usual IGFET input circuit where the largest fraction of the input voltage is absorbed across the insulator. However, in the limit when the gate insulator capacitance is made large, such as by decreasing the insulator thickness or increasing the dielectric constant, the input voltage drop across this part of the circuit will approach zero and the entire input voltage will approach V_s except for any IR drops that may remain. The situation then becomes almost identical to that in the input circuit of the bipolar transistor.

The IGFET Control Capacitance

In the same manner that changes in base minority-carrier charge in the bipolar transistor can be associated with a change in the emitter-junction voltage, the changes in IGFET channel charge can be associated with changes in the potential V_s. This recognition, combined with the well-known definition of capacitance as a change in charge for a change in associated voltage, leads to what might be defined as a control capacitance C_c. In the following derivation Q_c is the total channel inversion charge:

$$C_c = \frac{dQ_c}{dV_s} = \frac{d}{dV_s}\left(\text{const. exp}\frac{eV_s}{kT}\right) \qquad [2]$$

$$= Q_c \frac{e}{kT}. \qquad [3]$$

The channel charge Q_c relates to n_c in Eq. [1] for the reasons shown in the Appendix. The capacitance C_c is the same in form and magnitude as the well-known diffusion capacitance that shunts the input of a bipolar transistor. Of the total device input voltage some fraction will appear across the high/low junction kT/e and thus across C_c which is effectively in series with the gate insulator capacitance. The fraction of the input voltage that appears across C_c can be viewed as the useful portion of the input voltage relative to the modulation of channel charge and drain current. The fraction of the input voltage

absorbed across the gate insulator capacitance is lost as far as charge modulation is concerned. The charge on both capacitances is equal since the capacitances are effectively in series.

Transconductance Relations

The drain current I is related to the channel charge Q_c by

$$I = \frac{Q_c}{\tau} \qquad [4]$$

where τ is the charge carrier transit time in the channel. This relation simply states that a charge Q_c is swept out into the drain each time period τ.

In the extreme limiting case of an infinitely large specific gate-insulator capacitance, all of the input voltage appears as V_s; none is lost across the insulator. At this hypothetical limit the transconductance g_m is given by

$$g_m = \frac{dI}{dV_g} = \frac{dI}{dV_s} = \frac{1}{\tau}\frac{dQ_c}{dV_s} = \frac{Q_c}{\tau}\frac{e}{kT}$$

or, by Eq. [4],

$$= I\frac{e}{kT}; \qquad [5]$$

the transconductance/current ratio is given by

$$\frac{g_m}{I} = \frac{e}{kT}. \qquad [6]$$

This new result for the limiting transconductance/current in IGFET's is consistent with that of other charge-control devices, such as the bipolar transistor and the grid-controlled vacuum tube. This new limit is to be compared with that predicted by classical IGFET theory

$$\frac{g_m}{I} = \frac{2}{V_g}, \qquad [7]$$

which is found in standard texts or can be straightforwardly derived from Eq. [24] in Appendix 1. Relation [7] predicts an unlimited range of values, in particular, ones that can be in excess of e/kT if V_g is made sufficiently small. This excursion can be achieved in principle by arbitarily increasing the value of the specific channel capacitance and decreasing V_g correspondingly to keep the channel charge constant, or Eq. [24] in the Appendix satisfied. In IGFET's of conventional design, V_g is of the order of a volt, and the incorrect limit result predicted by Eq. [7] does not come into question.

Generalized Transconductance and Input Impedance

Consider the general situation wherein the total gate input voltage V_g divides across the total gate insulator capacitance C_o ($= CL$ of Appendix 1) and the control capacitance C_c associated with V_s and the channel charge. For simplicity, we shall ignore stray capacitances at the channel ends and those arising from depletion layers between the channel and the underlying semiconductor body. Following the procedure in Eq. [5], the transconductance will then be

$$g_m = \mathrm{I}\,\frac{e}{kT}\,\frac{dV_s}{dV_g}. \qquad [8]$$

The derivative term can be evaluated by using the distribution of voltage across C_o and C_c,

$$V_s = V_g \frac{C_o}{C_o + C_c}, \qquad [9]$$

which gives

$$\frac{dV_s}{dV_g} = \frac{C_o}{C_o + C_c} - V_g C_o (C_o + C_c)^{-2} \frac{dC_c}{dV_g}. \qquad [10]$$

Substituting Eq. [4] into Eq. [3] and differentiating gives

$$\frac{dC_c}{dV_g} = \tau \frac{e}{kT} g_m. \qquad [11]$$

Use of Eq. [11] and several other simple substitutions in Eq. [10]

gives the final results:

$$g_m = \frac{e}{kT} I \left| \frac{C}{C_o +}$$

$$g_m = \frac{e}{2kT} I \frac{C_o}{C_o}$$

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$$g_m = \frac{e}{kT} I \left[\frac{C_o}{C_o + 2C_c} \right] \qquad [12]$$

$$g_m = \frac{e}{2kT} I \frac{C_o}{C_c} \qquad \text{for } C_o \ll C_c \qquad [13]$$

$$g_m = \frac{e}{kT} I \qquad \text{for } C_o \gg C_c \qquad [14]$$

$$g_m = \frac{e}{3kT} I \qquad \text{for } C_o = C_c. \qquad [15]$$

Relation [13] corresponds to the situation in IGFET's of conventional design. That this is indeed the case can be seen by using substitutions from Eq. [3] and from Eqs. [28] and [29] of the Appendix, which reduce Eq. [13] to

$$g_m = I \frac{3/2}{V_g}. \qquad [16]$$

Aside from the small difference in the numerical constant, this relation is identical to that derived from classical IGFET theory as typified by Eq. [7]. Note, also, that Eq. [13] can be written

$$\frac{1}{C_o} g_m = \frac{e}{2kT} \frac{I}{C_c} = \frac{1}{2} \frac{1}{\tau}, \qquad [17]$$

which shows that there is a basic trade-off in an IGFET between transconductance and input impedance as represented by $1/C_o$. High input impedance or dynamic voltage range capability results in low transconductance and vice versa.[2]

The condition represented in Eq. [14] is identical to that of a bipolar transistor[2] and is approached in an IGFET of conventional design at very low drain currents where C_c, as seen from

$$C_c = \frac{e}{kT} Q_c = \frac{e}{kT} I \tau, \qquad [18]$$

is relatively small. This result seems to be a reasonable explanation for the IGFET experimental observations noted earlier.[5] Condition [14] would be observed at higher drain currents if the specific insulator capacitance is increased. Numerical calculations based upon surface C-V data[10] seem consistent with the results noted above.

With respect to Eq. [15], there is a general physical argument to the effect that the parallel plate spacing must be approximately a Debye length for the gate capacitance to match the control capacitance. A similar type of argument shows that $C_u \approx C_c$ when the gate voltage is equal to kT/e. More generally, $C_c/C_o \cong V_g/(kT/e)$.

Frequency Capability

As the IGFET specific gate capacitance is increased to make the device approach the bipolar transistor earmark characteristics of high transconductance and low input impedance, the IGFET frequency capability will improve because of an improved ability to rapidly charge parasitic device and circuit capacitances.

The above conclusion as well as the effect on power gain can be seen from another viewpoint also. This viewpoint was developed in an earlier analysis based upon charge control considerations as well as upon solid-state material constraints.[12] The analysis showed in a very general manner that there are basic trade-offs between transistor power gain G_p, device input voltage dynamic range V_T, maximum allowable device output voltage V_m, and operating frequency f at which the foregoing parameters were defined. For either a bipolar or field-effect transistor at their ultimate performance limit,

$$(G_p V_T V_m)^{1/2} f = \frac{E v_s}{2\pi}. \qquad [19]$$

Here, the basic device material constraints are E, the dielectric breakdown field of the semiconductor, and v_s, the carrier saturation velocity. For a given value of V_m, G_p and f will be maximum when V_T is a minimum. The minimum attainable value of V_T is the kT/e characteristic of bipolar transistors. The value of V_T ($\cong V_g$) for IGFET's of conventional design is typically several volts. Accordingly, as V_T is decreased toward the kT/e value of bipolars by increasing the specific gate capacitance, IGFET power gain and frequency response characteristics will improve.

Other Effects

In accord with the classical picture of IGFET operation, the drain saturation voltage will tend to decrease with the gate input voltage as the specific input capacitance is increased. This can be seen from Eq. [24] of the Appendix, which shows that

$$V_g\ (=\text{drain saturation voltage}) = \sqrt{\frac{2LI}{\mu C}}. \qquad [20]$$

Accordingly, the drain saturation voltage will vary inversely with the square root of the gate insulation capacitance in the range represented by Eq. [13]. In the range near that described for Eq. [15], the behavior of the drain saturation voltage with gate-insulator capacitance is more complicated. At the hypothetical limit for V_g of kT/e, the drain saturation voltage would be of the order of kT/e. This, combined with the absence of the typical voltage offset of bipolar transistors, would put the current knee at a lower voltage than that seemingly possible with bipolar transistors.

The dynamic power consumption P_d of a digital circuit is given by the well-known relation

$$P_d = fCV^2 = fQV.$$

If we assume a given value of the operating frequency f and a given switched charge Q, then P_d will decrease with V, the operating voltage level. This level is directly related to the drain saturation voltage.

Junction Field-Effect Transistors

I have not considered in detail the reasons for the approach to e/kT limits for JFET's, which was also noted experimentally at low drain currents.[5] Crudely speaking, the reasons for this behavior would seem to be as sketched below.

The equivalent of the IGFET insulator capacitance in JFET's is the gate depletion capacitance. The carrier charge activation barrier is not at the channel-source electrode interface, as in the IGFET, but effectively exists around the edges of the channel where the channel joins to the gate depletion layer. As the gate voltage is decreased, the channel expands its dimensions, and total charge, by the thermal motion of majority carriers which climb a kT/e hill at the channel–depletion-layer interface. In other words, the location of

the channel edge moves outward toward, and is defined by, the potential surface at which the depletion layer retarding potential is of the order of kT/e units higher than that of the underlying channel.

If the channel current is very small, as would be the case for very small total channel charge, then the fraction of total channel charge that feels the kT/e barrier will be relatively large, and we should not be surprised to find g_m/I ratios approaching e/kT. To state it another way, which is analogous to the IGFET case, the channel control capacitance is relatively small compared to the depletion layer capacitance, which is in series with it. At large channel currents, the situation is reversed, and we should not expect to find kT/e results.

To maximize the drain current at which kT/e characteristics are evident, the device should have a very heavily doped, thin, channel. This would maximize the depletion layer capacitance, maximize the transconductance, and minimize the input impedance and dynamic input voltage range. Indeed, high performance JFET devices are fabricated in this manner.[13]

Analysis Limitations

The preceding analysis was intended as a demonstration of basic physical principles and consequent limits, rather than as a detailed analysis of any particular device under specific conditions of operation. For reasons of simplicity, the effects of stray capacitances, resistances, and frequency were neglected. As with bipolar transistors, these effects can almost certainly be expected to deter the attainment of the theoretical e/kT limit in commercially realizable devices. The kT/e limit, itself, should be inviolate.

Summary

The preceding analysis proposes that an IGFET can be viewed as a hypothetical bipolar transistor with a base that couples to the outside world through a series capacitance, the gate-insulator capacitance. The bipolar device is unusual in that it has no dc base current, that is, it has an alpha identically equal to unity, and has no dc net leakage current. If the series capacitance is increased sufficiently, the IGFET performance takes on the distinguishing characteristics of the bipolar device.

To Warner's statement[6] "It is noteworthy that attainable g_m in the MOSFET is tied directly to the state-of-the-art, whereas g_m in the bipolar device is essentially fixed by nature," I would add, "But the MOSFET state-of-the-art leads toward precisely the same natural limit!"

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Acknowledgment

It is a pleasure to acknowledge stimulating and helpful discussions with D. O. North, W. Bosenberg, R. Williams, K. H. Zaininger, and D. P. Kennedy.

Appendix 1—Channel Charge Relations

The following derivation closely parallels conventional derivations that take into account the variation of voltage along the channel length of the gate capacitance due to the resistive voltage drop along the channel. Relationships are developed between applied gate voltage, physical gate capacitance, channel charge, potential drops along the channel, and the channel current. Particular attention in the following derivation is given to the relationship between total channel charge and the charge density conditions at the source end of the channel. These need to be related to justify Eqs. [2] and [3] of the text.

The inversion charge $Q(x)$ per unit length of the channel at the point x units from the source is

$$Q(x) = C\,[V_g - V(x)], \qquad [21]$$

where C is the gate-insulator capacitance per unit length of the channel, V_g is the applied gate voltage (which is assumed totally across the gate capacitance), and $V(x)$ is the voltage drop at the point (x) due to the resistive drop along the channel associated with the flow of the load current I. The differential drop dV per differential length dx of the channel at the point x is

$$dV = \frac{I}{\sigma(x)} = \frac{I\,dx}{\mu Q(x)} \qquad [22]$$

where $\sigma(x)$ is the channel conductivity at the point x, and μ is the charge-carrier mobility, which is assumed constant along the channel. This assumption should have no effect on our final conclusions over a rather wide range of behavior of μ.

Substituting Eq. [21] into [22] and integrating the voltage between the limits 0 and V, and the distance over the limits 0 and x, we get

$$V^2 - 2V_g V + \frac{2I}{\mu C}x = 0. \qquad [23]$$

For the pinch-off condition, $V = V_g$ at the drain end of the channel where $x = L$. In consequence Eq. [23] yields:

$$\frac{2I}{\mu C} = \frac{V_g^2}{L}. \qquad [24]$$

This shows several well-known relations that apply at channel pinch-off.

Inserting Eq. [24] into [23] and solving for V we get

$$V = V_g \pm V_g \sqrt{1 - \frac{x}{L}} \qquad [25]$$

The positive sign is spurious and will hereafter be dropped. Eq. [25] gives the potential drop along the channel under pinch-off conditions.

For conditions below pinch-off, Eq. [25] becomes

$$V = V_g - V_g \sqrt{1 - \frac{bx}{L}} \qquad [26]$$

where b expresses the ratio of the actual current I to the pinch-off value at a given value V_g of the applied gate voltage. Eq. [26] states that V never rises to a magnitude V_g unless pinch-off occurs, that is, unless $b = 1$. It is interesting to note that under non-pinch-off conditions, there will be a low/high junction at the channel/drain interface in addition to the high/low junction at the source/channel interface. The junction voltage at the drain end of the channel will be the larger of the two, because the channel charge density is lower at this end.

Inserting Eq. [25] into [21] we obtain the expression for the inversion charge $Q(x)$ per unit length of the channel at any point x along the channel:

$$Q(x) = CV_g \sqrt{1 - \frac{x}{L}} \qquad [27]$$

At the source end of the channel $x = 0$, and

$$Q(x) = Q(0) = CV_g. \qquad [28]$$

The total inversion charge Q_c in the channel is obtained by integrating Eq. [27] over the length of the channel:

$$Q_c = 2/3\, LQ(0). \qquad [29]$$

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To relate $Q(0)$ to the channel volume charge density n_c adjacent to the source, and hence to Eq. [1] of the text, we make use of a previously derived semiconductor surface relation[14] that links the inversion charge density n_c with the surface potential ψ, the distance x from the surface into the material's interior, the intrinsic carrier density n_i, the doping density n_A of the background material, the minority carrier charge density n_o in the background material, and the intrinsic Debye length $\mathcal{L}$:

$$n_c = \frac{n_o}{\left[\left(\frac{n_i}{n_A}\right)^{1/2} \frac{x}{2\mathcal{L}} + \exp\left\{\frac{-e\psi_o}{2kT}\right\}\right]^2} \qquad [30]$$

An analogous thermal equilibrium relation applies to p-channel devices.

The potential at the semiconductor surface is ψ_o. Eq. [30] is only valid in the inversion layer. Terms involving the fixed dopant charge and the majority carrier charge were dropped. We now integrate the relation

$$Q(0) = W \int_0^x n_c dx, \qquad [31]$$

wherein W is the lateral gate width. We obtain

$$Q(0) = \frac{2W\mathcal{L}n}{\left(\frac{n_i}{n_A}\right)^{1/2}}, \qquad [32]$$

wherein $n = n_o \exp\{e\psi_o/(2kT)\}$ is the inversion charge density at the semiconductor surface adjacent to the source. The integration was carried out to a depth x into the material sufficient to include the majority of the inversion charge.

Eq. [32] is the desired relation. It shows that the channel volume charge density adjacent to the source is directly proportional to $Q(0)$ and hence to the total channel charge Q_c (Eq. [29]).

Relation [32] is quite general. It is not affected by the inclusion of nonthermal equilibrium conditions into Eq. [30], as for example,

by including the effect of the load current IR voltage drop along the channel. The above relationship between the total charge in the channel and the channel charge density adjacent to the source is analogous to the familiar bipolar transistor relationship between total base charge and the base charge density adjacent to the emitter.

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[11] See, e.g., A. Rose, "An Analysis of the Gain-Bandwidth Limitations of Solid-State Triodes," **RCA Review,** Vol. 24, p. 627, Dec. 1963.
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[13] First brought to the author's attention by J. Moll.
[14] See Eq. 3.17, p. 38, of Reference (8).

Practical Use of

A. H. Sommer

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1. Introduction

In 1965, Scheer an white light sensit odes than had be

* The research Army Electronic S Night Vision Labor

† This paper a Phys. Conf. Ser. Bristol, England.