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A REVIEW OF THE THEORY AND TECHNOLOGY FOR OHMIC CONTACTS TO GROUP III–V COMPOUND SEMICONDUCTORS

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Abstract—The technology for ohmic contacts to group III–V compound semiconductors is reviewed in this paper. The basic principles of current transport in metal–semiconductor (Schottky barrier) contacts are presented first. The modes of current transport considered are thermionic emission over the barrier, and tunneling through the barrier due to thermionic-field or field emission. Special attention is devoted to the parameters of temperature and doping concentration which determine the dominant mode of conduction. As the primary mode of conduction changes from thermionic emission dominated to tunneling dominated, the current–voltage behavior of the contact changes from rectifying to ohmic in character. The experimental techniques for fabricating ohmic contacts to III–V compound semiconductors are then described. Contact problems as they pertain to specific device applications are considered. Finally, present difficulties with contacts to mixed III–V crystals are discussed.

1. INTRODUCTION

The rectifying metal–semiconductor point contact was discovered by Braun[1] in 1874, and during the past 100 yr these contacts have been used as rectifiers and photodetectors. Metal point contacts also served as the injectors and collectors for the first transistors, but as methods for fabricating *PN* junctions became available, metal–semiconductor contacts began to assume a subservient role as so-called "ohmic" contacts for transporting current into and out of *PN* junction devices. It soon became apparent that *PN* junction rectifiers were better behaved and more easily understood than the not too predictable nor reproducible metal–semiconductor rectifiers. At first, ohmic contact requirements for Si and Ge junction transistors were relatively simple, but the need for higher speed devices with their smaller and more complex geometries placed greater demands on the performance of ohmic contacts. New semiconducting materials such as GaAs, GaP, AlAs, and mixtures of these materials, and novel device structures such as light emitting diodes and bulk-effect oscillators also caused more problems for the ohmic contact technology.

In the 1930's, Schottky[2] developed the first acceptable theory of rectification for metal–semiconductor contacts. Today these rectifiers are often referred to as Schottky barrier diodes. Other names are surface barrier diodes and hot-carrier diodes. Since about 1960, Schottky diodes have been experiencing a renaissance of scientific interest due to at least three factors: (1) development of the planar process for bipolar and field-effect transistors which also led to development of reliable, reproducible, large-area, metal–semiconductor rectifiers, (2) the need for higher frequency devices that would be free from the inherent speed limitations associated with minority carrier storage in *PN* junction devices, and (3) the proposal of the metal–base transistor. Presently, Schottky barrier rectifiers satisfy a wide spectrum of commercial applications.

Unlike Schottky barrier rectifiers, the subject of metal–semiconductor ohmic contacts has experienced only mild scientific interest. Carefully organized attempts[3] to really understand ohmic contacts are relatively scarce in number when compared, for example, with the attention devoted to understanding *PN* junctions and semiconductor–oxide interfaces. This problem is due at least in part to the unexciting performance of a satisfactory ohmic contact and to the rather notorious history of metal–semiconductor interfaces. The importance of ohmic contacts did not go unnoticed of course, particularly in cases where the success of some device process suddenly became vitally dependent on the quality of the ohmic contact (e.g., the purple plague problem associated with Au wires bonded to Al–Si ohmic contacts). It is probably a fair assessment, however, that the ohmic contact technology has developed thus far more as a technical art than as a science.

The term ohmic contact does not necessarily imply a linear current–voltage characteristic. A metal–semiconductor contact has associated with it a space-charge region whose current–voltage behavior eventually becomes nonlinear as bias increases. Ideally, the contact resistance of the space-charge layer would be negligible relative to the bulk or spreading resistance of the semiconductor contacted by the metal, but this is rarely achieved in practice. From a practical point of view, a satisfactory ohmic contact is one that does not significantly perturb device performance. In other words, the contact is usually acceptable if it can supply the required current density with a voltage drop that is sufficiently small compared with the drop across the active region of the device, even though the current–voltage behavior of the contact may not be strictly linear.

In theory, the contact resistance can be completely defined if the operating parameters (temperature and bias) and physical parameters (contact area, impurity concent-

ration profile, barrier height, effective mass, and dielectric constant) are known. In practice, the contact resistance can be seriously affected by a number of other factors that influence conduction (e.g., interface layers due to oxide formation or contamination, surface damage, minority carrier injection, and energetically deep lying impurity levels or traps). Because of these complications the correlation of theory and experiiment is often difficult and, consequently, most studies of ohmic contacts usually consist of little more than an examination of processing techniques which lead to low impedance metal–semiconductor contacts.

In this review we will first present a qualitative description of current transport mechanisms in metal–semiconductor (Schottky barrier) contacts. Three modes of current transport will be considered: thermionic, thermionic-field, and field emission. The experimental techniques for fabricating ohmic contacts to group III–V compound semiconductors will then be described. Finally, contact problems as they pertain to specific device applications will be discussed.

THEORETICAL CONSIDERATIONS

Schottky barriers

Schottky's diffusion theory for rectification in metal–semiconductor contacts postulates the existence of a space charge region which gives rise to an electrostatic potential energy barrier[2]. The space charge region, which is depleted of mobile carriers, is situated in the semiconductor adjacent to the metal layer. Obviously, a thin layer of space charge with the opposite polarity must also exist in the metal at the interface to complete the charge dipole and maintain charge neutrality. When one assumes a uniform distribution of ionized impurities in the semiconductor, Poisson's equation yields the one-dimensional parabolic potential energy barrier shown in Fig. 1 and described by

$$\phi(x) = q^2Nx^2/2\epsilon_s\epsilon_0 \qquad (1)$$

for $0 \le x \le w$. In the semiconductor, N is the ionized donor concentration, ϵ_s the static dielectric constant, and ϵ_0 the permitivity of free space. The depletion layer width, w, is related to the energy band bending in the semiconductor depletion region, E_b, by

$$E_b = \phi_b - \phi_s - qV = q^2Nw^2/2\epsilon_s\epsilon_0, \qquad (2)$$

where ϕ_b is the barrier height, ϕ_s the position of the Fermi level relative to the conduction band edge, and V the applied forward bias. Throughout this paper energy is expressed in units of electron-volts.

Figure 1 shows a depletion layer Schottky barrier for an N-type semiconductor. Three other configurations are possible: a depletion layer barrier for P-type material, and accumulation layers ("negative" barrier heights) for N- or P-type material. Nearly all practical metal–semiconductor contacts result in depletion layer barriers.

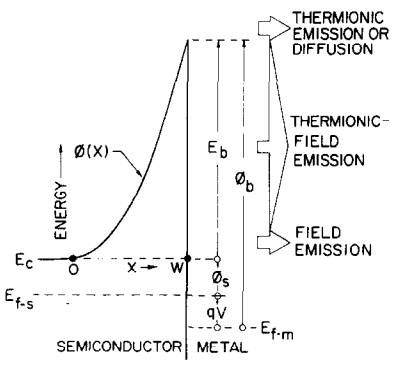

Fig. 1. Parabolic depletion layer type of potential energy barrier for an N-type semiconductor. Image force rounding of the barrier shape is neglected.

Barrier heights

To first approximation, the barrier height is a fixed constant of the two contact materials. It is the most important single feature of a metal–semiconductor contact and is analogous to the built-in or diffusion voltage of a PN junction. Like the group IV semiconductors Si and Ge, GaAs and most of the other group III–V compound semiconductors are highly covalent. It is an experimentally observed fact that for such materials the barrier height is approximately 2/3 of the band gap for N-type material and approximately 1/3 of the band gap for P-type material[4] (see Fig. 2). In other words, the barrier height for covalent semiconductors is essentially independent of the metal used. It was first proposed by Bardeen[5] that the influence of a high density of surface states pins the Fermi level at the interface, thus fixing the barrier height. For highly ionic materials such as most of the group II-VI compound semiconductors (e.g., ZnS and ZnO) and the transition-metal oxides (e.g., $KTaO_3$ and $KNbO_3$) the barrier height is strongly dependent on the work function of the metal (see Fig. 3). It has been proposed that these materials exhibit a low density of active surface states at

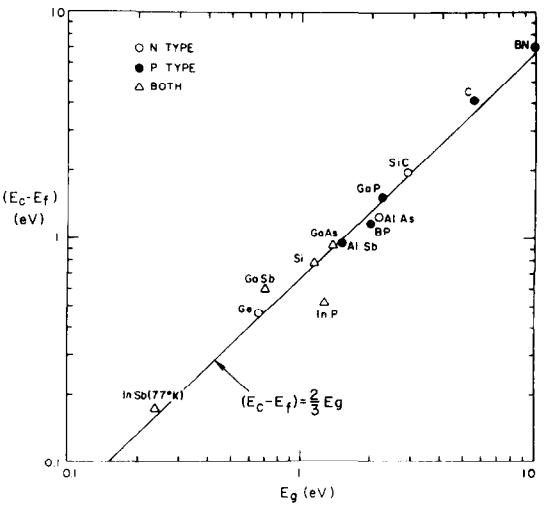

Fig. 2. Illustration of the two-thirds rule for barrier height pinning at the metal–semiconductor interface for Au contacts on various covalent semiconductors. The location of the Fermi level relative to the conduction band ($E_c - E_f$) at the interface is plotted vs energy gap E_g (from Ref. [4]).

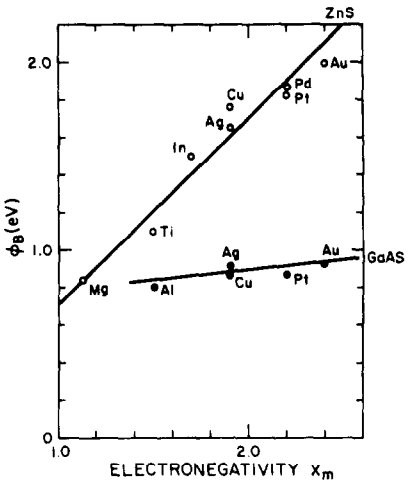

Fig. 3. Experimentally determined barrier heights for various metals on an ionic semiconductor (ZnS) and on a covalent semiconductor (GaAs) (from ref. [4]).

the interface and consequently the Fermi level is unpinned[6].

From the experimental relationship between the barrier height and the electronegativity of the metal, X_m, one can define a Fermi-level stabilization parameter, S, where $S \equiv d\phi_b/dX_m$ [6]. The relationship of S to the electronegativity difference between the species of a compound semiconductor, ΔX, is shown in Fig. 4. For mildly ionic materials with $\Delta X \approx 0{\cdot}8$, the use of a metal whose work gives a very small barrier (or even an accumulation layer) offers a simple method for making an ohmic contact. Examples are In or Ga on CdSe[7]. With more highly ionic semiconductors such as ZnS, however, a metal does not exist with a sufficiently small work function (i.e., sufficiently small electronegativity) to give a low barrier [7]. If thermionic emission over the barrier were the only possible conduction mechanism in metal–semiconductor systems, the number of semiconductors to which ohmic contacts could be made would be very limited.

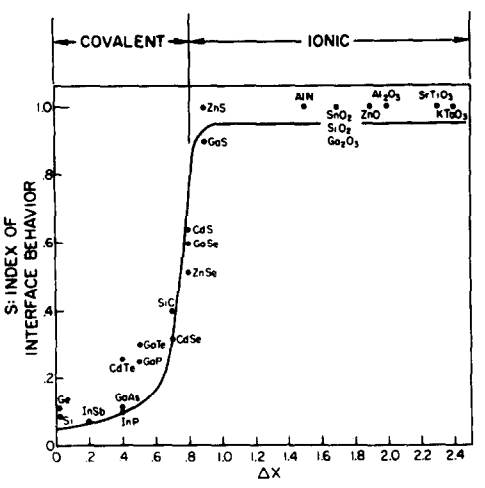

Fig. 4. Index of interface behavior, S, vs electronegativity difference, ΔX, between the species of a compound semiconductor (from ref. [6]).

Thermionic emission

A schematic representation of rectification due to thermionic emission of carriers over a Schottky barrier in an N-type semiconductor is shown in Fig. 5. Forward bias reduces the band bending, E_b, which is the height of the energy barrier experienced by mobile carriers in the semiconductor (see equation (1). Under reverse bias, however, the energy barrier for carriers in the metal, ϕ_b, remains essentially unchanged. Using Maxwell–Boltzmann statistics to describe the distributions of carriers that can be emitted over the barrier, we can relate the forward flux J_f and reverse flux J_r by

$$J_f = J_r \exp(qV/kT), \tag{3}$$

where

$$J_r \equiv A^*T^2 \exp(-q\phi_b/kT). \tag{4}$$

In equation (4), A^* is the appropriate Richardson constant for the semiconductor, k Boltzmann's constant and T the absolute temperature. The total current density J then yields the simple form of the diode equation

$$J = J_f - J_r = J_r[\exp(qV/kT) - 1]$$
$$= A^*T^2 \exp(-q\phi_b/kT)\,[\exp(qV/kT) - 1]. \tag{5}$$

From equation (5), which represents the ideal thermionic emission situation, the contact resistance at zero bias, R_c, is kT/qJ_r Ω-cm^2.

Bethe[8] first derived equation (5) for thermionic emission over the barrier. Schottky's diode equation [2] for diffusion over the barrier yields a bias dependent pre-exponential term different from A^*T^2. The thermionic emission diode equation above is valid for high electric fields across a narrow space charge region and barriers high compared to kT, which is the most commonly encountered situation in metal–semiconductor contacts. Both thermionic and diffusion theories yield the same direction for rectification.

In reality the shape of a metal–semiconductor potential barrier is not truly parabolic because charge carriers in the semiconductor are electrostatically attracted towards the metal surface by an induced mirror-image charge of opposite sign in the metal. The attractive image force changes the otherwise parabolic energy distribution of equation (1) to

$$\phi(x) = \frac{q^2Nx^2}{2\epsilon_s\epsilon_0} - \frac{q^2}{16\pi\epsilon_d\epsilon_0(w-x)}, \tag{6}$$

where ϵ_d is the relative dynamic (high frequency) dielectric constant of the semiconductor[9]. The effect of image force on the barrier shape is shown in Fig. 6. The lowering of the barrier due to image force is given by[10]

$$\Delta\phi = \left[\frac{q^2E_bN}{8\pi^2\epsilon_s\epsilon_d^2\epsilon_0^3}\right]^{1/4}. \tag{7}$$

From equation (7), the image force lowering equals the band bending, E_b, when

$$N_{\text{ideal}} = 1{\cdot}8 \times 10^{19}\,\epsilon_s\epsilon_d^2E_b^2\text{cm}^{-3}, \tag{8}$$

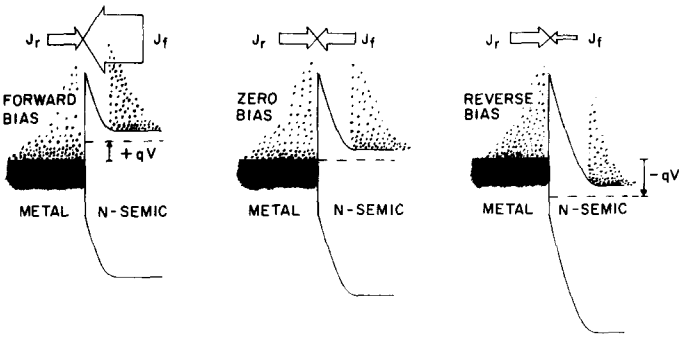

Fig. 5. Schematic representation of thermionic rectification in a Schottky barrier for forward, zero, and reverse applied bias conditions.

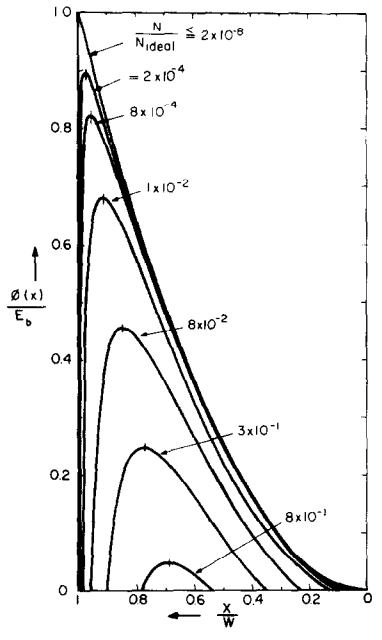

Fig. 6. Effect of image force on the shape of the potential barrier at a metal–semiconductor interface. $N_{ideal} = 3 \times 10^{22}$ cm^{-3} for N-type GaAs with a band bending $E_b = 1$ eV.

where E_b is expressed in units of eV. Equation (8) affords a means for obtaining an ideal (zero-barrier) ohmic contact (see Fig. 6). Unfortunately the impurity concentration indicated by equation (8) is well in excess of the solubility limit for impurities in known semiconductors. As an example, $N_{ideal} = 2{\cdot}7 \times 10^{22}$ cm^{-3} for GaAs with $E_b = 1$ eV. As the donor concentration is increased, barrier narrowing ($w \propto N^{-1/2}$) proceeds more rapidly than barrier lowering ($\Delta\phi \propto N^{1/4}$) and, consequently, as doping is increased conduction becomes dominated by quantum-mechanical tunneling through a narrowed barrier rather than by thermionic emission over a lowered barrier.

Because of image force lowering, the actual barrier height is $\phi_b - \Delta\phi$ where $\Delta\phi$ is bias dependent (see equations (2) and (7)). It is often desirable to remove all bias dependence from J_r (i.e., from the saturation current density) and this can be accomplished by introducing a diode ideality factor, n, where

$$J \propto \exp(qV/nkT) \tag{9}$$

when $qV/kT \geq 3\,kT$ (see equation 5)). In other words

$$n \equiv \frac{q}{kT}\left(\frac{dV}{d\ln J}\right), \tag{10}$$

and then it can be shown that

$$n_{\text{thermionic}} = \frac{1}{1-(\Delta\phi/4E_b)} \tag{11}$$

for pure thermionic emission[10]. For the flat band case where $\Delta\phi = E_b$, $n_{\text{thermionic}} = 1{\cdot}33$. In typical cases, however, the effect of image force on the value of n is much smaller (e.g., $n_{\text{thermionic}} \approx 1{\cdot}03$ for $N_{GaAs} = 10^{19}$ cm^{-3} with $E_b = 1$ eV).

Thermionic emission of carriers over the barrier gives rise to current rectification in metal-semiconductor diodes. In addition there are two other modes of current transport that involve quantum-mechanical tunnelling through the barrier (see Fig. 1). As the impurity concentration is increased, the width of the depletion layer is decreased (see equation (2)) and initially the barrier becomes thin enough that thermally excited carriers can tunnel through near the top of the barrier. This temperature dependent mode of current transport is referred to as thermionic-field emission or thermally-assisted tunneling. As the impurity concentration is increased even further the barrier finally becomes so thin that significant numbers of carriers can tunnel through even at the base of the barrier. This mode of current transport is called field emission tunneling and is temperature independent. Field emission is the preferred mode of current transport in metal–semiconductor ohmic contacts. The transition from thermionic (i.e., rectifying) to thermionic -field to field (i.e., ohmic) dominated conduction is schematically illustrated in Figs. 7 and 8. As impurity concentration increases, the magnitude of the current in the vicinity of zero bias is greatly increased, which strongly enhances the ohmic behavior of the metal–semiconductor contact.

Thermionic-field emission

In a theoretical analysis of thermionic-field emission[11, 12], kT/E_{00} was shown to be a measure of the importance of thermionic emission relative to thermionic-field tunneling, where $E_{00} = (qh/4\pi)\,(N/m^*\epsilon_s\epsilon_0)^{1/2}$ and

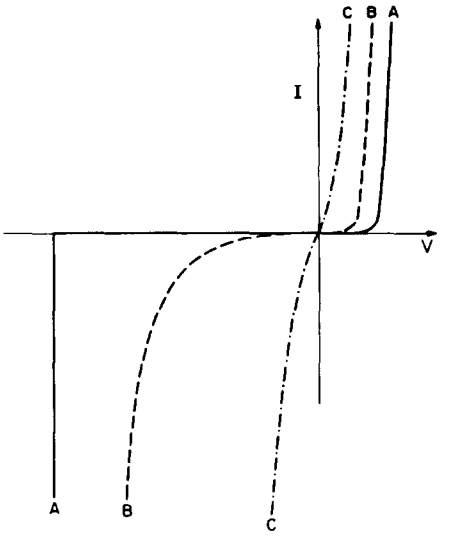

Fig. 7. Schematic illustration of the current–voltage relationship for a Schottky barrier contact (e.g., Au on *N*-type GaAs) for progressively higher carrier concentrations (from ref. [4]). (a) $N \leq 10^{17}\,cm^{-3}$; thermionic emission dominates. (b) $N \approx 10^{18}$–$10^{19}\,cm^{-3}$, thermionic-field tunneling dominates. (c) $N \geq 10^{19}\,cm^{-3}$, field emission tunneling dominates.

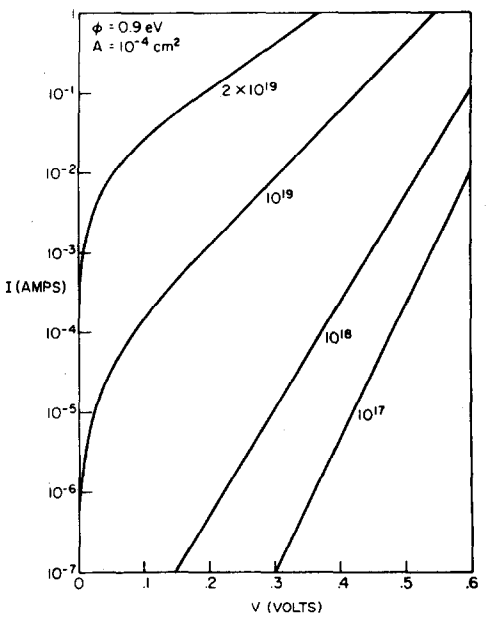

Fig. 8. Schematic semilogarithmic current vs forward bias relationship for a progression of carrier concentrations similar to those shown in Fig. 7 (from ref. [4]).

m^* is the effective mass of the majority carriers. Thus, kT/E_{00} is proportional to $T/\sqrt{N}$. As temperature increases, the fraction of current transported due to thermionic emission increases. On the other hand, when doping increases, the barrier width is reduced and thermionic-field emission tunnelling is enhanced. Figure 9 illustrates how the relative position of the maximum transmission through the barrier depends on kT/E_{00}. Note that for any given operating temperature the doping range

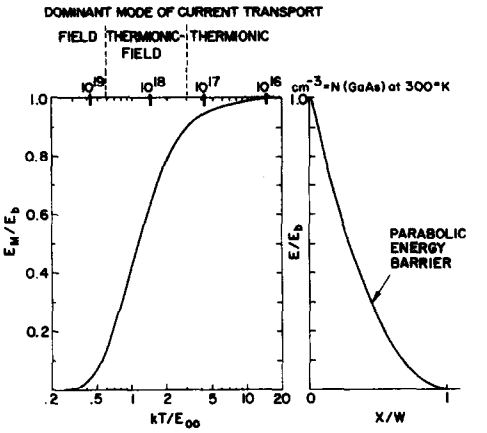

Fig. 9. Relative position of maximum transmission through or over a Schottky barrier vs the parameter kT/E_{00}. Note the narrow range of doping in *N*-type GaAs over which thermionic-field emission dominates conduction.

for thermionic-field dominated transmission is quite narrow.

The deviation of the diode n-value from unity may be used as a measure of the relative contribution of thermionic-field tunneling to conduction, as shown in Fig. 10. Effects of image force and edge leakage also cause the n-value to exceed unity, but even larger deviations of n from unity arise due to tunneling [9, 11, 12]. Since image force, interface layers, and tunneling effect carriers transported in either direction, the n-value should also appear in the reverse flux term that was neglected in equation (9). An appropriate form of the diode equation for both thermionic and thermionic-field emission is [9, 12, 13].

$$J = J_r\left\{\exp(qV/nkT) - \exp\left[\left(\frac{1}{n} - 1\right)qV/kT\right]\right\}. \quad (12)$$

When n equals unity, equation (12) reduces to the simple form of the diode equation given in equation (5). The

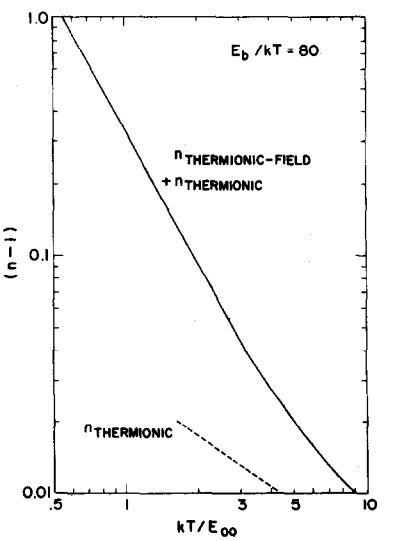

Fig. 10. Predicted deviation of diode n-value from unity vs the parameter kT/E_{00}.

current–voltage characteristic predicted by equation (12) is shown in Fig. 11. For $n > 2$ the diode conducts better under reverse bias. This "backward" diode action due to tunneling dominated conduction was first predicted by Wilson[13] and later confirmed by Stratton[14]. The barrier layer rectification theories of Schottky[2] and Bethe [8], which correctly predict the polarity of rectification for metals on lightly doped semiconductors, were long thought to be the only correct results. Since a unique value of n is associated with a given set of diode conditions (i.e. temperature, bias, and doping), Wilson's tunneling theory actually has a set of mutually exclusive conditions under which it applies. It is interesting to note that the Esaki PN-junction tunnel diode also conducts best under reverse bias because tunneling dominates conduction.

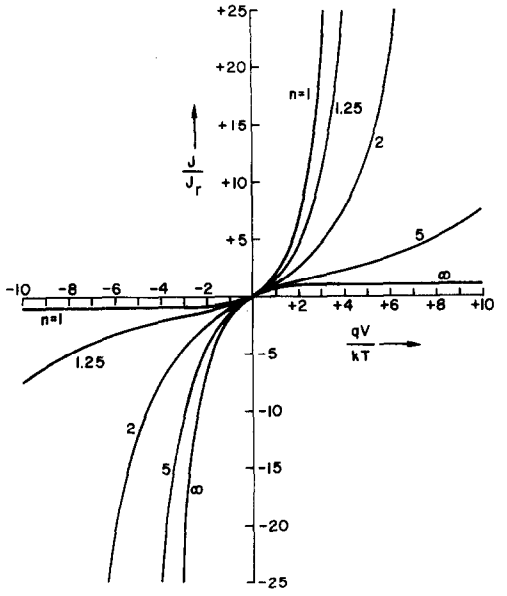

Fig. 11. Normalized current–voltage characteristic predicted by equation (12). As n exceeds 2 the direction of rectification reverses.

Field emission

As impurity concentration is increased, the dominant mode of conduction changes from thermionic to thermionic-field to field emission, and the exponential bias dependence of the current changes from qV/kT to qV/E_{00} [4, 14]. Since E_{00} is proportional to $\sqrt{N}$, the forward bias characteristics for field-emission-dominated conduction are strongly dependent on doping. Figure 12 shows the effect of doping on contact resistance when field-emission dominates conduction [4].

OHMIC CONTACTS TO III–V COMPOUND SEMICONDUCTORS

Highly doped surface layers

The most common method of producing an ohmic contact is to place a metal layer in contact with a region of very high doping. The objective is to achieve field-emission-dominated conduction so that the potential barrier will appear to be almost transparent to carrier flow. A highly doped surface layer may be obtained by:

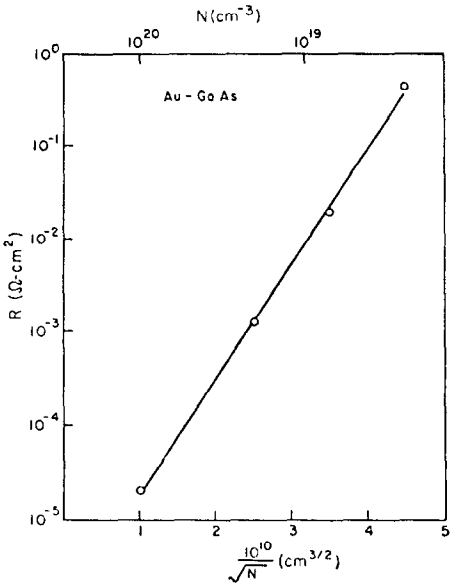

Fig. 12. Contact resistance of Au-Schottky barriers on N-type GaAs as a function of carrier concentration for field-emission dominated conduction (from ref. [4]).

alloy regrowth, in-diffusion of a dopant contained in the contact material, epitaxial regrowth (double epitaxy), shallow diffusion, or ion implantation. In the alloy regrowth technique the metal dissolves some of the semiconductor during heating. Upon cooling the semiconductor will come out of solution and regrow on the underlying crystal [7]. The regrown region will contain a substantial concentration of the metal which is thought to act as a dopant (e.g., Au for N-type GaAs)[15]. If lower alloying temperatures or higher doping levels are required it is often advantageous to utilize another dopant impurity in addition to the contact metal (e.g., Au–Ge for N-type GaAs and Au–Zn for P-type GaAs)[15, 18]. The role of Au (as well as that of Ge) in influencing the electrical conduction in contacts to N-type GaAs is still unclear.

An increasingly popular technique, especially for layered or bulk-effect devices, is to epitaxially grow a special contacting region of high doping on top of the active region. This is referred to as epitaxial regrowth or double epitaxy. A difficulty with epitaxial regrowth is that a high resistivity region sometimes occurs between the active region and the highly doped regrown layer.

A highly doped surface layer may also be fabricated using diffusion or ion implantation. With diffusion complications arise due to the required diffusion temperature which may be incompatible with the device fabrication process, and due to the depth of diffusion which may be incompatible with thin layered structures. The major problem with doping by ion implantation is in making the implanted species electrically active. For example, the required high concentration of $10^{19}\,cm^{-3}$ electrically active dopants in GaAs has not yet been achieved by ion implantation. Other problems with ion implantation are surface damage and high annealing temperatures.

For some device structures, contact problems arise if the

required level of high doping cannot be achieved. For example, the solubility limit for the dopant or the allowable alloying temperature, or both, may prevent sufficiently high doping. In such situations thermionic-field emission may contribute significantly to or even dominate the conduction process. The current–voltage characteristic of an evaporated Au–Ge contact on 10^{15} cm^{-3} N-type epitaxial GaAs is shown in Fig. 13. An alloying temperature of 400°C was necessary to produce an ohmic contact [15]. Note the similarity between Figs. 8 and 13.

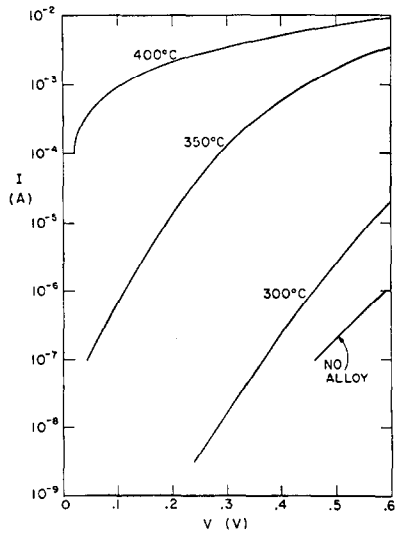

Fig. 13. Forward current–voltage characteristics of evaporated Au–Ge contacts on 10^{15} cm^{-3} epitaxial N-type GaAs for different alloying temperatures (from ref. [16]).

Fabrication techniques

The fabrication of an ohmic contact usually involves deposition of a metal or a mixture of metals which may also contain a dopant. Deposition is generally accompanied or followed by alloying on a hot stage or in a furnace. Alloying is usually performed in vacuum or in an inert atmosphere such as Ar or forming gas (85% N_2 and 15% H_2). The following methods of depositing metal layers onto semiconductors are used: evaporation, sputtering, plating, preformed contacts, pressure contacts, and soldering.

Evaporation and sputtering are the most widely used deposition techniques, and both techniques allow the contact to be alloyed during the deposition. If a resistance or RF induction heated source is used for evaporation, the evaporant must be evaporated to dryness. This insures correct stoichiometry for a multiconstituent contact material such as Au–Ge–Ni [17, 19, 20]. Recent results with Au–Ge contacts for N-type GaAs indicate that sputtering may give a lower contact resistance than evaporation [16]. This result was tentatively explained in terms of more uniform films obtained with sputtering. The possible beneficial influence of sputtering-induced surface damage on contact resistance will be discussed later.

Both electrolytic and electroless plating in a chemical solution are attractive deposition techniques because of their simplicity. An important property of electroless processes is their ability to deposit metals selectively. This property depends critically on the structure of the substrate which may be intentionally sensitized [21]. An example is the electroless deposition of Pd from a $PdCl_2$ solution for ohmic contacts to GaAs laser arrays [22]. Pd adheres to GaAs but not to protective Al_2O_3 layers on GaAs. Zn is then diffused through the Pd contact to form a P^+ region in the GaAs. A similar technique involving alloying through a contact was used to relieve alignment problems with the Schottky barrier FET developed at IBM Research in Zurich [23]. A common approach often used in research work is to alloy a preformed sphere or strip of the contact material to the semiconductor. An even simpler but less reliable technique is to use pressure contacts.

Ion implantation is generally undesirable for depositing metal layers because the rate of deposition is so low. On the other hand, ion implantation may provide a useful tool for studying the effect of surface damage on contact resistance. An old technique for obtaining ohmic contacts with Ge is to sandblast the surface and then solder on a contact. In a modern rendition of this approach, Ge substrates were bombarded with Ge ions and a metal contact was then applied [24]. In this case an ion implanter was used to induct a controlled amount of surface damage and no subsequent annealing or alloying was employed.

For most semiconductors the effect of surface damage on contact resistance and on ohmic contact formation is as yet unclear. Compared to evaporation, deposition by sputtering is suspected of causing a greater degree of surface damage. In addition, sputtering is often preceded by a beneficial back-sputter cleaning of the semiconductor surface (the so-called glow discharge cleaning). Using a transmission electron microscope, Anderson [25] observed that back-sputter cleaning tends to produce a polycrystalline surface layer, and that more extensive back-sputtering can even cause an amorphous layer. An unusual feature of ion implantation in Si is that if a continuous amorphous layer is formed, the epitaxial regrowth of this phase onto the underlying substrate can yield electrically active species which are uncompensated in concentrations far exceeding the ordinary solid solubility (e.g., of Sb and Bi in Si). This observation may have important implications for ohmic contacts and a study is underway to examine the effect of damage in GaAs due to As implantation [24].

Table 1 lists group III–V compound semiconductors with their more popular contact materials. In many cases the only information available was from research results (e.g., contacts suitable for Hall measurements) rather than development or production processes. For N-type GaAs, the most commercially important III–V semiconductor, a wide variety of materials have been examined. Two of the more reliable contact processes for N-type GaAs are Au–Ge and Au–Te [15, 16, 18]. The distribution coefficient for Si in GaAs is one order of magnitude greater than that of Ge [16], and one might anticipate that Au–Si would offer a lower resistance contact to N-type GaAs than Au–Ge, but thus far this has not proven to be the case.

Alloying problems

The wetting action of metallic compounds on GaAs is

Table 1. Ohmic contact technology for III–V compound semiconductors

III–V	E_g (eV)	Type	Contact material	Technique	Alloy temp (°C)	Application
AlN	5·9	semi-I	Si	Preform	1500–1800	Bistable R
		semi-I	Al, Al–In	Preform	1000	Bistable R
		semi-I	Mo, W	Sputter	500–1000	Bistable R
AlP	2·45	*N*	Ga–Ag	Preform	150	Hall meas.
AlAs	2·16	*N,P*	In–Te	Preform	160	Hall meas.
		N,P	Au	Preform	700	Hall meas.
		N,P	Au–Ge	Preform		Hall meas.
		N	Au–Sn	Preform		Hall meas.
GaN	3·5	semi-I	Al–In	Preform		Bistable R
GaP	2·31	*P*	Au–Zn(99:1)	Preform, evap.	700	LED
		P	Au–Ge	Preform	360	LED
		N	Au–Sn(62:38)	Preform	700	LED
		N	Au–Si(98:2)	Evap.	600	LED
GaAs	1·45	*P*	Au–Zn(99:1)	Electroless, evap.		LED
		P	In–Au(80:20)	Preform		LED
		N	Au–Ge(88:12)	Evap.	350–450	Gunn osc.
		N	In–Au(90:10)	Evap.	550	Gunn osc.
		N	Au–Si(94:6)	Evap.	300	Gunn osc.
		N	Au–Sn(90:10)	Evap.	350–700	Gunn osc.
		N	Au–Te(98:2)	Evap.	500	MESFET
GaSb	0·70	*P*	In	Preform		Hall meas.
		N	In	Preform		Hall meas.
InP	1·26	*P*	In	Preform	350–600	LED
		N	In, In–Te	Preform	350–600	LED
		N	Ag–Sn	Preform, evap.	600	Gunn osc.
InAs	0·35	*N*	In	Preform		Hall meas.
			Sn–Te(99:1)	Preform		Hall meas.
InSb	0·17	*N*	In	Preform		Hall meas.
		N	Sn–Te(99:1)	Preform		Hall meas.

low and the contact material tends to separate into islands. This adhesion problem is also called "mounding" or "balling-up". This difficulty can be alleviated by evaporating or co-evaporating a metal over lay such as Ni, Pt, or Au [19–21, 26, 27] which does not form a eutectic with the contact metal at temperatures below the alloying temperature. For *P*-type III–V's, Au–Zn is the most successful contact material due to the very high diffusion coefficient of Zn. When alloying a Au–Zn contact, however, care must be taken not to re-evaporate the Zn. A short heat pulse of moderate temperature (e.g., less than 450°C) generally works well.

A satisfactory ohmic contact to both *N* and *P*-type group III–V materials is often provided by In[28]. It has been suggested[29] that for Sb and As based III–V semiconductors, In may form an InSb or InAs layer upon alloying. Since the band gaps of these two compounds are relatively low (see Table 1) the resultant small gap to wide gap heterojunction may serve as a ohmic contact. Although this proposal is certainly feasible, there is thus far no direct evidence to support or disprove it.

An important factor that is generally recognized is that surface cleanliness is essential for reliable, reproducible ohmic contacts [15, 16, 18, 20, 28]. The problem is obviously acute for AlAs which quickly forms an oxide layer upon exposure to air. Less well known is the fact that a significant oxide layer can also form on an exposed GaAs surface thus affecting ohmic contact formation, for example, a 20 Å gallium oxide layer can form on GaAs in one hour[30].

Device considerations

Device applications of group III–V materials include injection lasers, light emitting diodes, Schottky barrier FET's, bulk-effect oscillators, IMPATT oscillators, bistable resistors, and multilayer devices such as semiconductor superlattices. Compared to most devices, lasers and light emitting diodes have relatively less severe contacting problems because the active regions are of necessity highly doped. Ohmic contacts for the *N*-type GaAs Schottky barrier FET are achieved by diffusion of Au–Te through a Cr–Rh metal layer [23]. Bistable resistors have the unique difficulty that the material is often semi-insulating (e.g., GaN) and the associated contact problems are still far from eliminated.

The fabrication of bulk-effect oscillators placed severe

demands on the ohmic contact technology. The first Gunn diodes used contacts alloyed directly to the lightly to the lightly doped N-type active region[19]. It was subsequently determined that the alloying process introduces damage into the active region which degraded device performance. Another problem, particularly with Sn contacts, was electromigration under high electric fields which led to conducting channels through the material. These problems were relieved by making an alloy contact to an epitaxial $N^+/N/N^+$ device structure, and commercial Gunn devices now almost always use this structure[31]. Similarly, microwave avalanche diodes (IMPATT'S, TRAPATT'S, etc.) also commonly use a double epitaxial process or diffusion into an epitaxial layer to improve the ohmic contact [32].

The successes with double epitaxy have led to increasing interest in multilayered device structures. Of these the room temperature injection laser is the most notable achievement thus far. With some layered device structures, namely Gunn and IMPATT diodes and the exploratory semiconductor superlattice[33], alloying is sometimes followed by etching in an attempt to reduce the active region of the device. A problem that is often encountered is that the alloyed region under and around the contact tends to etch faster than the surrounding active region. This effect has at least two possible explanations: (1) the contact region is chemically more reactive due to localized stresses or surface damage, or (2) the metal layer establishes an electrolytic cell that locally enhances the etching rate.

Contacts to mixed crystals

The development of the GaAs–Ga_{1-x} Al_xAs heterojunction laser generated considerable interest in ohmic contacts to mixed III–V crystals [17,31] Table 2 lists III–V mixed crystals with their contact materials. For P-type materials, Au–Zn gives a satisfactory ohmic contact, but for P-type $GaAs_{1-x}P_x$, Al yields an even better contact[17]. For some unexplained reason, however, Al yields a rectifying contact on P-type $Ga_{1-x}Al_xAs$. For N-type materials, Au–Ge gives a satisfactory ohmic contact, while Au–Si has yet to be tested. With $Ga_{1-x}Al_xAs$ the contact behavior appears to be very sensitive to the Al concentration and difficulties increase as the Al mole fraction, x, increases. This problem has led to increasing reliance on epitaxial regrowth of N^+ or P^+ GaAs layers for ohmic contacts mixed crystal devices.

SUMMARY

Let us briefly summarize some of the essential features of a satisfactory ohmic contact. From a commercial point of view the process technology must be suitable for mass production and yield reliable and reproducible contacts. From a device point of view, and depending on the application, the contact should be noninjecting for minority carriers and the contact material should not undergo electromigration under high electric fields. Furthermore, surface damage associated with the fabrication process should not be so high that reliability is affected. The thermal impedance of the contact must be low enough that sufficient heat can be removed from the device through the contacts if required. Thermal impedance decreases as contact thickness increases which may cause increased surface strain and subsequent surface damage, hence, there may be an optimum metal thickness depending on the device application[28]. A working definition of a satisfactory ohmic contact is one that can supply the required current density with a sufficiently small voltage drop, even though the current–voltage characteristic of the contact may not be strictly linear.

The subject of ohmic contacts is at best a pragmatic art rather than a science, and consequently it tends to be a rather unglamorous area of research. Nevertheless, the

Table 2. Ohmic contact technology for mixed III–V compound semiconductors

III–V	Type	Contact material	Techniques	Alloy temp (°C)	Application
$GaAs_{1-x}P_x$	P	Au–Zn	Evap.	500	LED
	P	Al	Evap.	500	LED
	N	Au–Ge–Ni	Evap.	450	LED
	N	Au–Sn	Evap.	450	LED, superlattice
$Ga_{1-x}Al_xAs$	P	Au–In	Electroplate	400–450	LED
	P	Au–Zn	Evap.	500	LED
	P	Al	Evap.	500	
	N	Au–Ge–Ni	Evap.	450–485	LED, superlattice
	N	Au–Sn	Evap, electroless	450	LED, superlattice
	N	Au–Si	Evap.		LED, superlattice
$Ga_{1-x}In_xSb$	N	Sn–Te	Evap.		Gunn osc.
$Ga_{1-x}Al_xP$	N	Sn	Preform		LED
$Ga_{1-x}In_xAs$	N	Sn	Preform		LED
$InAs_xSb_{1-x}$	N	In–Te	Preform		Hall meas.

established practicality of group III–V compound semiconductors for device applications is causing increasing demands for reliable ohmic contacts to these materials. Contact difficulties are particularly acute for wide band gap *N*-type III–V materials such as GaAs, GaP, AlAs, and mixtures of these semiconductors which have intrinsically high barrier heights. For these materials, which are among the most promising III–V's for device use, a metal does not exist with a low enough work function to yield a low barrier. In such cases the general technique for fabricating an ohmic contact involves establishment of a highly doped surface layer by alloy regrowth, in-diffusion of a dopant contained in the contact material, double epitaxy, shallow diffusion, or ion implantation. Presently, double epitaxy (epitaxial regrowth) is the most reliable approach. Although ion implantation is not yet directly useful for ohmic contact fabrication, the technique should provide a useful tool for examining the important question of the effect of surface damage on ohmic contact formation.

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