

Solar Energy Materials and Solar Cells 46 (1997) 289-310

Solar Energy Materials and Solar Cells

Amorphous silicon/p-type crystalline silicon heterojunction solar cells

B. Jagannathan^a, W.A. Anderson^{a,*}, J. Coleman^b

^a Department of Electrical and Computer Engineering, Center for Electronic and Electro-optic Materials, State University of New York at Buffalo, Amherst, NY 14260, USA ^b Plasma Physics Corporation., P.O Box 548, Locust Valley, NY, USA

Received 20 January 1997

Abstract

We have investigated the photovoltaic (PV) characteristics of both glow discharge deposited hydrogenated amorphous silicon (a-Si:H) on crystalline silicon (c-Si) in a n^+ a-Si:H/undoped a-Si:H/p c-Si type structure, and DC magnetron sputtered a-Si:H in a n-type a-Si:H/p c-Si type solar cell structure. It was found that the PV properties of the solar cells were influenced very strongly by the a-Si/c-Si interface. Properties of strongly interface limited devices were found to be independent of a-Si thickness and c-Si resistivity. A hydrofluoric acid passivation prior to RF glow discharge deposition of a-Si:H increases the short circuit current density from 2.57 to 25.00 mA/cm² under 1 sun conditions.

DC magnetron sputtering of a-Si:H in a Ar/H_2 ambient was found to be a controlled way of depositing n type a-Si:H layers on c-Si for solar cells and also a tool to study the PV response with a-Si/c-Si interface variations. 300 Å a-Si sputtered onto 1–10 Ω cm p-type c-Si resulted in 10.6% efficient solar cells, without an A/R coating, with an open circuit voltage of 0.55 V and a short circuit current density of 30 mA/cm² over a 0.3 cm² area. High frequency capacitance-voltage measurements indicate good junction characteristics with zero bias depletion width in c-Si of 0.65 μ m. The properties of the devices have been investigated over a wide range of variables like substrate resistivity, a-Si thickness, and sputtering power. The processing has focused on identifying and studying the conditions that result in an improved a-Si/c-Si interface that leads to better PV properties.

Keywords: Amorphous silicon; Crystalline silicon; Solar cell; Sputtering; Glow discharge; High frequency capacitance; Spectral response; Interface

^{*} Corresponding author. Tel.: + 1 716 645 2422; fax: 1 716 645 5964.

1. Introduction

Glow discharge deposited amorphous silicon on tin oxide coated glass has perhaps been the most researched in the class of Si thin films for achieving low cost terrestrial solar cells. However, the Staebler-Wronski effect limits the usefulness of these devices over long exposures to illumination. Multijunction cells [1] fabricated by glow discharge deposited a-Si:H, a-Si:Ge, and a-Si:C type alloys have been projected as a solution for overcoming the losses associated with the light induced degradation. This technology requires many layers of bandgap tuned material and so is sophisticated in its processing requirements and this can only serve to increase the cost of the cell. An alternative to the a-Si alloy based solar cells would be the use of large grained thin film polycrystalline silicon (poly-Si) as the absorber layer for the solar cell. For the past few years, there has been much effort put in this direction and there has been some success by research groups in obtaining large grained poly-Si on inexpensive substrates. Baba et al. [2] have obtained the polysilicon by solid phase crystallization (SPC) of a-Si and have reported a grain size of $1-2.5 \,\mu\text{m}$, although only for n-type a-Si. In our laboratory [3], work has been done to develop poly-Si on sheet Mo by a solid phase growth technique and $20 \,\mu\text{m}$ + grain sizes have been achieved. The other important development has been the ability to deposit microcrystalline Si (µ c-Si) on glass by H₂ dilution of SiH₄ [4]. Larger as-deposited grain size ($\sim 0.2 \,\mu m$) by a microwave plasma enhanced chemical vapor deposition process [5] has also been reported. Perhaps, as this technology matures, larger grained poly-Si can be obtained by solid phase or metal induced crystallization of the as-deposited μ c-Si. Since the amount of bonded H_2 in these materials is low, they are expected to show little or no degradation after long exposures to illumination. For growth of the poly-Si or μ c-Si, the maximum processing temperature employed is much less than 600°C, and so the conventional junction forming techniques that require annealing/dopant activation cannot be applied. One possible method of fabricating solar cells on these base materials is depositing a thin layer of a-Si or microcrystalline silicon window layer to form a junction. a-Si:H deposition to form a junction has many beneficial properties. The a-Si deposition is usually done at around 300°C, which makes it compatible with all the polysilicon processes and is especially relevant in the case of μ c-Si obtained by H₂ dilution of SiH₄. Further, poly-Si possesses low blue response and high red-infrared response and hence a-Si with its higher photoresponse in the blue-violet region could augment the response of the solar cells. Finally, since the a-Si layer is thin, the photoinduced defect creation would also be low.

The a-Si/c-Si type structures have received some attention because of their application in not only solar cells but also in heterojunction transistors [6] and X-ray detectors [7]. Solar cells utilizing this structure have been reported by Tanaka et al. [8]. They showed 18% efficient devices for a p a-Si/i a-Si/n c-Si type structure. However, it would appear that a-Si does not play any role in photogeneration because it is only 70 Å thick. Baba et al. [2] also reported fabrication of an 8% efficient a-Si/SPC poly-Si type solar cell and recently Fisher et al. [9] have reported 13% efficient pin a-Si/ pin μ c-Si type thin film cells. This study focuses on the a-Si/c-Si type solar cells in an attempt to understand some of the complexities involved and the nature of the processing required in integrating an amorphous layer to a polycrystalline layer. Here, relatively thicker a-Si has been used in an attempt to involve this layer in active photogeneration along with its use for junction formation. The first cells studied are of a n⁺a-Si/i a-Si/p type c-Si form where the a-Si layer has been deposited by a rf glow discharge process. The PV properties were found to be dominated by the nature of the a-Si/c-Si interface. The effect of this interface has been elucidated in various properties of the cells. A simple hydrofluoric acid (HF) dip of the c-Si, prior to the a-Si deposition, results in much improved device performance. It was realized that the a-Si needed to be deposited by a process where the interface formation and a-Si thickness could be finely controlled. DC magnetron sputtering with n-type Si targets was examined because it is a controlled method to deposit thin a-Si layers. The properties of the devices using sputtered Si were optimized with respect to doping in c-Si, thickness of the a-Si:H layer, and deposition temperature. Effect of the a-Si/c-Si interface on the photovoltaic (PV) characteristics of the devices was examined by studying the effect of the sputter discharge power and deliberate oxide at the interface.

2. Experimental

In all instances, the p-type Si wafers were first RCA cleaned then cleaned in a acetone/methanol/deionized (DI) water sequence. The native oxide was etched away by a buffered hydrofluoric acid (BHF) dip for ~ 30 s, and then 1000 Å of Al was deposited. The contact was then sintered in a muffle furnace at 600°C to form the back ohmic contact. Following this, the front surface of the wafer was cleaned with BHF. In some instances, the wafers were retreated with HF or BHF (30 s) and rinsed with DI water just prior to loading for either glow discharge or sputter deposition of a-Si.

The n⁺a-Si/i a-Si/p c-Si type solar cells where fabricated by the successive deposition of the amorphous layers on the wafer substrates by RF glow discharge deposition of SiH₄ at Plasma Physics Corporation. The undoped layer was deposited by decomposition of 100% SiH₄, and the n⁺a-Si layer by using 1%PH₃ (balance of H₂) along with 10% SiH₄ (balance of He). 50 W RF power was used in the i layer deposition, and the substrate was maintained at 250°C. The front ohmic contact to the cells has been formed by using 2 mm Yb dots about 250 Å thick with 1 mm Al dots about 1000 Å thick.

The other type of solar cell discussed here has been fabricated by DC magnetron sputtering of a-Si using n-type Si targets onto p-type c-Si substrates to form an n-p type heterojunction. The chamber was evacuated to a base pressure of $\sim 3 \times 10^{-7}$ Torr. The magnetron sputtering was carried out in an Ar/H₂ ambient at a total chamber pressure of <10 mTorr. Sputtering was carried out using 2 in. diameter high purity silicon targets in a US gun and later US-II type gun. After pumping to the specified base pressure, the high vacuum gate valve was throttled and H₂ and Ar partial pressures were set. Sputtering was carried out for a minute with the shutter closed under the experimental conditions of pressure and substrate

temperature to allow for target cleaning. Unless otherwise specified, the substrate temperature during sputtering was kept at 275°C. Further, the substrate-target distance of 8 cm, and 64 W of power was normally used.

Photoconductivity and photoresponse tests were performed at 100 mW/cm^2 AM1.0 spectrum from a tungsten halogen lamp calibrated with a standard solar cell. Spectral studies in the visible range were performed using Oriel filters between 0.4 and 0.7 µm with a 50 Å bandwidth under constant intensity condition. The output power from the filter had been calibrated by a standard solar cell and a power meter.

Glass substrates were used to characterize the sputtered silicon by Raman spectroscopy, and dark or photoconductivity experiments. Dark and photoconductivity evaluation was performed by evaporating Mg contacts $(1 \text{ mm} \times 1 \text{ mm})$ spaced 40 µm apart, and defined by photolithography. Evolved gas analysis (EGA) was performed on Si deposited on an oxidized wafer to determine the total H₂ content of the film. The process and equipment used has been described in Ref. [10]. The small area cells had a 2 mm diameter Mg ohmic contact, about 250 Å thick, with a 1000 Å thick 1 mm Al dot in the center. The larger area cells had a thick Au/Mg grid defined by photolithography for ohmic contact. In some instances, 600–800 Å of SiO₂ was reactively evaporated to form the anti-reflection (A/R) coating.

3. Results and discussion

3.1. Glow discharge deposited amorphous silicon/crystalline silicon solar cells

A n⁺/i a-Si:H structure was chosen to provide a good ohmic contact to the amorphous layer and to ensure good carrier collection. The a-Si deposited by this method has been characterized extensively before [10, 11]. Undoped a-Si:H films deposited around 250°C shows a dark conductivity (σ_D) of 1×10^{-7} S/cm and a photoconductivity (σ_{PH}) of 1.5×10^{-6} S/cm. The total H₂ content in these films determined by EGA has been estimated to be around 19%, most of which exists in a bonded form as observed from Fourier transform infrared experiments. For the devices themselves, no heat treatment was permissible after the a-Si deposition, so the Al ohmic metal was deposited on the c-Si wafer and sintered first. For the same reason, Yb, a low work function metal, was used as the front ohmic contact. Within this context, devices are being compared broadly with respect to surface preparation conditions, viz., with and without a HF treatment just prior to glow discharge deposition.

3.1.1. Photoresponse of the solar cells

Table 1 shows the PV properties of some of the solar diodes. All cells in this table had an area of 0.03 cm^2 . In the diodes #1UN-4UN to be discussed now, the wafer has not been treated with HF just before loading for a-Si:H deposition. The untreated solar cells have low short circuit current density (J_{SC}) , open circuit voltage (V_{OC}) and fill factor (FF). In addition, the photocurrent kept increasing with applied reverse bias

Cell #	c-Si resistivity (Ω cm)	HF clean	i layer thickness (µm)	$V_{\rm OC}$ (V)	$J_{\rm SC}~({\rm mA/cm^2})$	FF
1UN	1.4	No	0.10	0.33	2.70	0.42
2UN	1.4	No	0.05	0.40	0.52	0.20
3UN	1-3	No	0.40	0.39	0.08	0.19
4UN	0.1	No	0.10	0.20	2.60	0.10
5CL	1-10	Yes	0.10	0.48	23.50	0.39
6CL	1-10	Yes	0.30	0.54	28.00	0.36
7CL	0.1-0.3	Yes	0.10	0.56	15.60	0.20

Table 1 Photovoltaic properties of some glow discharge deposited n⁺a-Si/i a-Si/p c-Si solar diodes

indicative of poor carrier collection in the devices. Amorphous layer thickness and c-Si resistivity were expected to have a large effect on the cell properties and hence were varied over a wide range to observe any changes that might occur. Reducing the amorphous layer thickness from 0.4 to 0.1 μ m and lower was expected to decrease the recombination in the layer and also reduce the series resistance, thereby leading to better FF, and perhaps better J_{SC} . A large increase in the doping of the substrate was expected to alter the built-in field in the junction and cause a lower depletion width in the c-Si, which in turn would affect the device response. However, as can be seen from the table, no specific trend in properties could be observed with these variations. The rapid increase in collected current with increasing reverse bias pointed to some shunt resistance mechanism to be prevalent in the cells.

To evaluate the nature of the problem, the current-voltage response of the cells was observed in blue ($\lambda = 0.4 \,\mu\text{m}$) and red ($\lambda = 0.6 \,\mu\text{m}$) light of equal intensity. Complete absorption of light at any wavelength would require at least $1/\alpha(\lambda)$ of a-Si:H thickness, where α is the absorption coefficient. For an absorption coefficient value of 3×10^5 cm⁻¹ this thickness is 330 Å. Since the a-Si thickness used in the experiments was at least 500 Å it was expected that light at $\lambda = 0.4 \,\mu\text{m}$ would be completely absorbed in the a-Si layer. Further, the light at $\lambda = 0.7 \,\mu\text{m}$ was expected to be predominantly absorbed in the crystalline silicon. In effect this could act as probe to sense generation/collection in a given layer at a certain depth from the surface. In such a case for example, photons with $\lambda = 0.4 \,\mu\text{m}$ would generate carriers in a-Si:H, and hence an I–V behavior would be indicative of generation/collection problems associated with this layer and collection through the other layer. Fig. 1a and Fig. 1b show the blue and red response of the cell #1UN. It can be observed that the photocurrent in blue light is low but the FF of the cell is much better than in red light, and photocurrent in the blue light did not vary significantly with reverse bias. Red response on the other hand has the same nature as the overall response of the cell in reverse bias and also exhibits similar magnitude of the photocurrent. This presented a curious problem that the minority carrier transport through a-Si to c-Si seemed far better than from c-Si to a-Si. This observation and the increase in collection with reverse bias pointed to a shunt resistance mechanism prevalent in the cells and was



Fig. 1. Blue and red response of cell #1UN.

thought of as a manifestation of states at the a-Si/c-Si interface. These states could be a result of dangling bonds, oxide growth in the time span between the HF clean of Al sintering step and plasma deposition of a-Si or plasma induced damage during growth of the a-Si layer.

There have been reports on the beneficial effects of HF dip of a silicon wafer [12, 13]. An HF dip causes etching of the native oxide and passivates the surface of c-Si by saturating the dangling bonds. Lai et al. [12] suggest that a HF/H_2O followed by a methanol/HF treatment without a DI water rinse results in a better interface than just a HF/H_2O dip. In the present study, since the Al back contact had to be protected from HF, only the front surface of c-Si was treated with HF and subsequently rinsed

with DI water. Thus, over the next depositions, the substrate surface was re-treated with HF (diluted 1:5 in DI water) just before the pump-down sequence began for the a-Si deposition. It was hoped that this would result in an oxide-free surface until the deposition could be started, and also that it would hydrogen passivate the dangling bonds on the c-Si surface. Cells subsequently fabricated in this way show an enormous improvement in properties especially the J_{SC} as seen from samples 5CL, 6CL, and 7CL in Table 1. The response on cell #7CL, fabricated on a 0.1–0.3 Ω cm wafer is much lower compared with the cells made on 1–10 Ω cm. Although the collection in the treated cells is much better, the cells still suffered from a non-saturating photoresponse and the FF is still not high. It was not clear if the problems seen now were still due to a poor interface, or was an effect of the series resistance of the amorphous layer. To investigate this, the a-Si layer in cell #6CL was successively etched by Sirtyl etchant from 15 to 40 s. Although the exact thickness of the a-Si layer was not known, fill-factor improved marginally to 0.42 for the cells subsequently fabricated on these and it was concluded that the interface was still a problem in these cells.

3.1.2. Dark current properties

Dark current properties of some of the devices have been investigated in some detail [14]. Fig. 2 compares the I-V characteristics of several samples, for both treated and untreated samples. The behavior of the untreated cell #1UN and treated 5CL ostensibly look the same in both the forward and the reverse bias at 300 K, in spite of the fact that they are very different in their photoresponse. Both of these samples in a bias range < 0.4 V show transport agreeing with the multi-tunnelling-capture-emission (MTCE) model. The reverse currents are proportional to $V^{1/2}$ indicative of generation in the depletion region of a-Si. However, the discrepancies become evident as the temperature is lowered to about 150 K. The current from the treated sample was too low to be measured at this temperature, but for the cell #1UN, an extra mechanism can be observed in the forward bias. Reverse characteristics of this cell also reflected a change, exhibiting an $I \propto V$ dependency, in the bias range of 0–0.2 V, a mechanism not expected in these types of cells. This behavior is more intense for cell #3UN (very poor PV properties) where $I \propto V$ dependencies are seen both in reverse bias as well as in the 0.15–0.3 V region in forward bias at room temperature. This $I \propto V$ behavior in the devices has been interpreted to be an effect of the interface states.

3.1.3. High frequency C–V characteristics

High frequency C-V response of the a-Si/c-Si cells using abrupt heterojunction theory, where the amorphous layer is taken to be a dielectric in series with the depletion layer capacitance in c-Si, has been reported [15] for 1 µm a-Si/p c-Si structure. A 1 MHz signal is too fast for the states in a-Si to follow, hence the capacitance offered by the a-Si layer is simply $\varepsilon_0 \varepsilon_s / L$, where L is the a-Si thickness. Using this and the abrupt heterojunction theory, the dependence of the depletion width in c-Si on the applied bias is expressed as

$$x_{\rm s}^2 = \left(\frac{\varepsilon_0 \varepsilon_{\rm s}}{C} - L\right)^2 = \frac{2\varepsilon_0 \varepsilon_{\rm s} N_{\rm I}}{q N_{\rm A} (N_{\rm I} + N_{\rm A})} (V_{\rm D} - V),\tag{1}$$



Fig. 2. Dark I-V behavior of some HF passivated and unpassivated n⁺a-S/i a-Si/p c-Si type solar cells.

where $N_{\rm I}$ is the effective defect density in a-Si, $N_{\rm A}$ is the doping concentration in c-Si, $V_{\rm D}$ the total diffusion voltage, and V the applied voltage. The diffusion voltage, $V_{\rm D}$, can be expressed as $V_{\rm D} = V_{\rm Da} + V_{\rm Ds}$, where $V_{\rm Da}$ is the diffusion potential on the amorphous side and $V_{\rm Ds}$ is the potential on the crystalline side. Solution to Poisson's equation results in expressions of built-in voltage for each side in terms of the depletion width as

$$V_{\rm DA} = \frac{q N_{\rm I} x_{\rm a}^2}{2\varepsilon_0 \varepsilon_{\rm s}},\tag{2}$$

$$V_{\rm Ds} = \frac{q N_{\rm A} x_{\rm s}^2}{2\varepsilon_0 \varepsilon_{\rm s}},\tag{3}$$

where x represents the depletion width on either side of the junction. Fig. 3 shows the 1 MHz C-V relationship for four devices representing one typical untreated sample and three treated ones varying in a-Si thickness and the substrate resistivity. The capacitance values for the untreated sample is rather low, when compared with a treated sample of similar a-Si thickness and substrate resistivity. For HF treated



Fig. 3. High frequency characteristics of some HF passivated and unpassivated n^+a -Si/i a-Si/p c-Si type solar cells.

samples, a decrease in the substrate resistivity for similar a-Si thickness yields large capacitance values indicative of low depletion widths in the substrate. This decrease in depletion width would be consistent with the reduction in J_{SC} observed for this cell (Table 1). Using Eq. (1) the effective defect density in the amorphous layer, zero-bias depletion width in c-Si and built-in voltage extracted from the C-V variation are shown in Table 2 (sample # 1UN-7CL). For the untreated sample, the capacitance does not show significant variation with bias which would imply that the depletion width is not varying with application of reverse bias, and any attempt to use the above formalism's results in erroneous values for $N_{\rm I}$, and unrealistically large values of take more reasonable values. Sample 5CL, fabricated on a 1–10 Ω cm substrate shows a depletion width of 0.57 μ m in c-Si compared with 0.07 μ m in the sample 7CL on a 0.1–0.3 Ω cm substrate. The computation of $N_{\rm I}$ leads to situations where $N_{\rm I}/N_{\rm A} + N_{\rm I} = 1$, and this could be interpreted as $N_{\rm I} > N_{\rm A}$ or a non-applicability of

Table	2
-------	---

5SP

2SPHD

 2×10^{16}

Sample #	Defect density (N_1) (cm ⁻³)	Zero-bias depl. width W _o (μm)	Built-in volt. $V_{\rm D}(V)$		
1UN	_	3.40	2.42		
5CL	$> 3.0 \times 10^{15}$	0.57	0.74		
6CL	1.8×10^{16}	0.36	0.94		
7CL	$> 1.5 \times 10^{17}$	0.07	1.07		
1SP	4×10^{16}	0.50	0.65		
2SP	$> 3 \times 10^{15}$	0.62	0.88		
3SP	$> 3 \times 10^{15}$	0.55	0.71		

0.59

0.27

0.68

1.01

Parameters from the high frequency C-V measurements for the RF glow discharge and DC magnetron sputtered a-Si/c-Si type solar cells

the abrupt heterojunction theory. For cell # 6CL, $N_{\rm I}$ computed from Eq. (1) is 1.8×10^{16} cm⁻³ which is higher than values reported in the literature for glow discharge deposited a-Si. The values of built-in voltages are higher than the values reported by Matsuura et al. [15]. The reduction in depletion width and increase of the built-in voltage for an increased a-Si thickness is also not clear. Since the photoresponse of the treated samples still indicates that the interface in these devices is still a problem, in spite of the HF treatment, it is quite likely that band-bending at the interface is affected, thereby affecting the depletion width in c-Si. Also, as has been pointed out by Sharma et al. [16], Eq. (1) does not account for the distribution of the density of states and band-bending in a-Si, which in reality might control the charge density in a-Si. This would result in the modification of the extracted values of diffusion voltage and $N_{\rm I}$.

It is fairly evident now that to obtain a good working solar cell, a good preparation of the substrate is needed and also the integrity of the interface must be preserved as the films are being deposited. Sputtering of silicon was considered a more attractive proposition due to a better control that one could exercise on growth power.

3.2. DC magnetron sputtered amorphous silicon/crystalline silicon solar cells

Although RF glow discharge deposited a-Si:H has become the "standard" a-Si for devices, a-Si:H with good electronic properties deposited by sputtering has been reported [17]. Pinarbasi et al. [17] have deposited films with σ_{ph} of 10^{-5} S/cm and σ_D of 10^{-8} S/cm with an activation energy for conduction of 0.8 eV in a UHV sputtering system. Compared with glow discharge deposition of a-Si, sputtering is completely different in that the H₂ is introduced externally and hence the surface conditions that result in a-Si:H would be different too. For our purposes, sputtering presented a technique by which properties of the a-Si/c-Si cells could be studied as a function of some parameters controlling the interface, without changing the properties of the amorphous layer. Interface damage could be increased or decreased by

simply increasing the sputter power or could be mitigated by placing a third electrode near the anode. Further, in magnetron sputtering, the target-substrate distance can be varied significantly, so the substrate can be moved from the plasma region to a region outside the plasma confinement thus modifying the interface formation.

3.2.1. Properties of sputtered a-Si

Before fabricating the cells, some of the properties of the sputtered Si were studied to find the conditions suitable and repeatable for fabricating devices. The two conditions that perhaps are the most important for obtaining an a-Si layer with good electronic properties are substrate temperature and H_2 partial pressure since the H_2 incorporation in the film and passivation of dangling bonds solely depends on these. As with RF glow discharge deposited a-Si:H, the properties of sputtered Si have also been reported to peak around deposition temperatures of 300°C. Thus, this investigation has centered around such substrate temperatures. An $Ar/(H_2 + Ar)$ ratio of 0.2 was chosen to allow for maximum amount of H_2 in the plasma, with a minimum amount of Ar required to start a discharge.

Si was sputtered using both 1–3 and 0.02 Ω cm n-type targets onto oxidized wafers and Corning glass. The microstructure has been evaluated for powers of 40, 64 and 90 W which correspond to the powers over which the effect of plasma power on the PV properties has been examined. Since the sputtering was conducted in a H₂ rich environment, it was necessary to confirm that the microstructure of the deposited silicon did not show any presence of micro-crystallites at the powers being studied. Raman spectroscopy performed for silicon deposited on glass at 48, 64, and 90 W power, only show a broad TO phonon peak at 480 cm⁻¹, indicative of amorphous silicon with no peak at 520 cm⁻¹ and hence no micro-crystalline silicon formation takes place at higher powers. EGA analysis done on films sputtered at 48 W indicate 11% total H₂ content in the films.

The electrical properties, namely, dark and photoconductivity and conduction activation energy of the a-Si film were evaluated with respect to variations in substrate temperature, Ar/H₂ ratio, sputtering powers, and target resistivity. Table 3 summarizes the film properties with respect to these variations. The condition referred to in this table and subsequent ones as "Standard" is a-Si deposited at 64 W of sputter power with an Ar/(Ar + H₂) ratio of 0.2, a temperature of 275°C, and a targetsubstrate spacing of 8 cm. All the other conditions have been stated as deviants from "standard". As can be observed, the films sputtered in the range of 225-300°C with a power of 40/64 W do not show any sharp variation in dark or photo-conductivity for both 1–3 and 0.02 Ω cm targets but an increase in power to 90 W power seems to result in higher conductivities. The dark conductivity was found to be thermally activated, agreeing with the relation $\sigma = \sigma_0 \exp[\Delta E_a/kT]$ where the activation energy $\Delta E_{\rm a}$ could be interpreted as $E_{\rm C} - E_{\rm F}$, the difference between the conduction band energy and the Fermi level. The high values of conductivity obtained could be due to a combination of defect states and also donor atom incorporation from the target. However, the rather high conductivity and low activation energy for the sputtering carried out at 90 W would seem to indicate that the conductivity is primarily due to high density of defect states in the Si.

Sample #	Conditions	Target type (Ω cm)	$\sigma_{\rm D}~({\rm S/cm})$	$\sigma_{\rm PH}~({\rm S/cm})$	$\Delta E_{\rm act}~({\rm eV})$
1SPGL	200°C, 40 W	0.02	1.77×10^{-5}	1.62×10^{-4}	0.28
2SPGL	250°C, 40 W	0.02	5.00×10^{-5}	5.60×10^{-4}	0.22
3SPGL	275°C, 40 W	0.02	1.96×10^{-5}	5.97×10^{-4}	0.30
4SPGL	300°C, 40 W	0.02	1.77×10^{-5}	1.40×10^{-4}	0.28
5SPGL	Standard ^a	0.02	9.00×10^{-5}	1.00×10^{-4}	0.28
6SPGL	275°C, 90 W	0.02	7.40×10^{-4}	2.00×10^{-3}	0.20
7SPGL	Standard ^a	1-3	1.00×10^{-4}	2.00×10^{-4}	0.32

Table 3 Properties of DC magnetron sputtered amorphous silicon

^a Standard refers to condition of 64 W power, 275°C temperature, and 8 cm source-subtrate distance.

The properties of the a-Si/c-Si devices have been investigated with respect to a-Si layer thickness, substrate resistivity, target resistivity, and input power. A substrate temperature of 275° C and a Ar/(Ar + H₂) ratio of 0.2 has been chosen for the solar cell fabrication. All the substrates, unless explicitly mentioned, have been re-treated with BHF for 30 s and DI water rinsed before loading for sputtering.

3.2.2. Dark I-V characteristics

(a) Effect of a-Si thickness: Fig. 4 shows the dark I-V nature of the a-Si/c-Si solar cells (sample #1SP-3SP) at 296 K for a-Si thicknesses of 300, 500 and 900 Å sputtered at 64 W with a 0.02 Ω cm target onto 1–10 Ω cm substrates. Conduction mechanism studies on this structure are underway. There seem to exist three transport mechanisms in the forward bias; one region between 0 and 0.4 V, a second region between 0.4 and 0.6 V where an increased slope can be seen in the I-V behavior, and finally a space charge limited region beyond 0.6 V. Upon increasing the a-Si thickness from 300 to 500 Å, the transport in the 0–0.4 V region seems to be affected, whereas transport in 0.4–0.6 V seems to be essentially the same. Increasing the a-Si thickness further to 900 Å causes one of the transport mechanisms to vanish and the magnitude of current to drop significantly in both forward and reverse bias. The reduced current level itself could be explained by the increased series resistance due to the increasing a-Si thickness. The origin of two regions of transport is perhaps an effect of the a-Si/c-Si interface as detailed in the next section.

(b) Effect of sputter power: Fig. 5 shows the dark I-V variation for devices (sample #8SP, 1SP, 9SP) fabricated at three powers, viz, at 48, 64 and 90 W of sputtering, keeping the a-Si thickness the same. Increasing the sputter power generally results in an increased ion bombardment of the substrate. This is expected to lead to an increased damage of the a-Si/c-Si interface, and hence creation of more defects at the interface. Since the thickness and the microstructure of the a-Si layer has been essentially kept the same within this range of powers, any differences arising in the carrier transport would exclusively be due to the a-Si/c-Si interface. When the I-V of the devices resulting from 48 and 64 W of sputtering are compared, it can be observed



Fig. 4. Dark I-V characteristics of sputtered a-Si/c-Si solar cells showing the variation with a-Si thickness.

that transport is essentially identical in the 0–0.35 V range, but the slopes start to vary in the 0.35–0.6 V range. Also, current levels drop significantly for the device made at 90 W and there is a sharp change in slope of the I-V curve at 0.35 V.

Comparing the observations from Figs. 6 and 7 it appears that the carrier transport in the region 0.35-0.6 V depends on the interface conditions, and transport for biases less than 0.35 V reflects some form of tunneling from c-Si into the a-Si region.

3.2.3. High frequency C–V response

Fig. 6 shows the high frequency C-V response for the devices for various targets, substrates and a-Si layer thicknesses configurations. Sample #1SP-3SP have a-Si layers sputtered from a 0.02 Ω cm target, and 1-3 Ω cm target for sample #5SP and 2SPHD. The linearity of the $1/C^2$ vs. voltage curves is apparent, and this is to be expected since the a-Si is relatively thin. Decreasing the substrate resistivity to 0.1-0.3 Ω cm (sample #2SPHD) leads to a lower depletion width in c-Si as evidenced



Fig. 5. Variation of dark I-V characteristics of sputtered a-Si/c-Si solar cells with sputter power.

by the higher capacitance values. Sputtering with 0.02 Ω cm or 1–3 Ω cm targets does not seem to affect the slopes of the curves or the absolute capacitance values very significantly. This is consistent with the conductivity data shown in Table 3, where a variation in target resistivity within this range does not seem to affect the dark/photoconductivity and activation energy of the a-Si film and hence no changes in depletion width or band bending would be expected. Table 2 also shows the diffusion voltage, defect density in a-Si and the zero bias depletion width in c-Si calculated by Eq. (1) for some of the cells (1SP-2SPHD). The computed N_1 values of $\sim 4 \times 10^{16}$ cm⁻³ are consistent with the data available in literature. As with the glow discharge devices, the depletion width reduces to 0.29 μ m for the 0.1–0.3 Ω cm substrate (sample #2SPHD) at zero bias as compared with 0.6 μ m for the 1-10 Ω cm substrate (sample # 5SP). Devices with thicker a-Si layers are again seen to exhibit larger values of band-bending. However, unlike the glow discharge deposited samples, the depletion width does not seem to vary too much with different a-Si thickness. From the computed values of $N_{\rm I}$ and c-Si depletion width, it appears that the a-Si would also be fully depleted under equilibrium conditions.



Fig. 6. High frequency C-V characteristics of some sputter deposited a-Si/c-Si solar cells.

3.2.4. Photoresponse

(a) Effect of a-Si layer thickness: Cells labelled # 1SP-7SP in Table 4 illustrate the variation of PV properties with thickness for sputtering with both the $1-3 \Omega$ cm, and 0.02Ω cm targets at a temperature of 275°C at 64 W power. Here again, no significant differences attributable to a difference in targets are seen. Cells having 100 Å of a-Si layer show a lower J_{SC} but a high FF. As the thickness of the a-Si layer increases to 300–370 Å the cells show an increased collection, with comparable J_{sc} and V_{oc} values to the glow discharge deposited a-Si/c-Si cells and much improved FF. A sharp degradation of cell properties, especially J_{SC} and FF, can be observed when the a-Si thickness is increased. Though it is likely that this is due to increased recombination in a-Si, spectral response tests were done to determine if the reduction was uniform for all wavelengths. Cells # 1SP, 2SP, and 3SP were exposed to light of constant intensity between wavelengths of 0.4 and 0.7 µm. The photocurrent is a function of the generation/collection at a particular depth for each wavelength and its variation with reverse bias is indicative of collection efficiency at each wavelength. Fig. 7d shows the variation of absolute photocurrent in the three cells. The current reduces severely at all wavelengths when the thickness of the a-Si layer is increased. The reduction is greater for longer wavelengths. The spectral dependence of the normalized photogenerated current for the three thicknesses is shown in Fig. 7a-Fig. 7c for zero bias, and reverse biases of 0.2 and 0.4 V. In these figures, the normalized photocurrent has



Fig. 7. (a)–(c) Normalized and (d) absolute photocurrent variation for sputtered a-Si/c-Si solar cells for 300, 500 and 900 Å thick a-Si.

Ceil #	Conditions	Target type (Ω cm)	a-Si thickness (Å)	$V_{\rm OC}$ (V)	$J_{\rm SC}~({\rm mA/cm^2})$	FF
1SP	Standard ^a	0.02	300	0.55	27.0	0.6
2SP	Standard ^a	0.02	500	0.52	12.5	0.36
3SP	Standard ^a	0.02	900	0.49	10.6	0.2
4SP	Standard ^a	1-3	100	0.50	14.90	0.61
5SP	Standard ^a	1–3	370	0.51	27.3	0.50
6SP	Standard ^a	1–3	500	0.51	17.60	0.36
7SP	Standard ^a	1-3	4000	0.52	0.14	0.15
8SP	48 W power	0.02	300	0.48	25.00	0.55
9SP	90 W power	0.02	250-300	0.43	13.85	0.27
10SP	20 Å SiO ₂	0.02	300	0.40	0.79	0.28
1SPHD	Standard ^a	1-3	100	0.51	7.95	0.65
2SPHD	Standard ^a	1–3	300	0.50	13.60	0.42

Table 4Photovoltaic properties of sputtered a-Si/c-Si solar cell

^a Standard refers to the condition of 64 W power, 275°C temperature, and 8 cm source-substrate distance.

been defined as the ratio I (λ ,rev bias)/I($\lambda = 0.4$,rev bias = 0); the photocurrent has been scaled with respect to zero bias photocurrent observed at a wavelength of 0.4 µm. For the cell with 300 Å of a-Si, the carrier generation/collection with red light is about 4 times that for the blue, implying that the majority of the response is from the c-Si and the collection itself is good as evidenced by the fact that a reverse bias of -0.4 V results in moderate increase in the current collected. The carrier collection is also uniformly improved throughout the wavelength regime by increasing the reverse bias which implies that the collection efficiency for this cell is similar for all the wavelengths. Increasing the a-Si thickness to 500 Å results in a maximum current generation at $\lambda = 0.6 \,\mu\text{m}$ and this drops for further increases in wavelength. The collection efficiency over all the wavelengths is reduced when the amorphous layer thickness is increased as seen by the rapid increase in current with the application of a reverse bias of 0.4 V. This effect is more pronounced for the cell with thicknesses of 900 Å. Since the depletion width in c-Si is actually higher (Table 4) for the 500 and 900 Å devices, the origin of the low generation for wavelengths above 0.60 µm is unclear. One possible explanation might be that as the a-Si thickness is increased, a greater portion of the longer wavelengths are absorbed in the a-Si layer and in regions closer to the junction. Such a condition would lead to a lowered generation in the devices, but a slightly improved collection for the longer wavelengths. The collection in the cells with thicker a-Si layer indeed improves for wavelengths greater than 0.6 µm.

(b) Effect of substrate resistivity: The cells 1SPHD and 2SPHD in Table 4 illustrate the variation of the PV properties with the substrate resistivity. As can be seen, the J_{SC} for the cells fabricated on the 0.1–0.3 Ω cm c-Si substrates is reduced by half compared to the 1–10 Ω cm substrates, over the two amorphous thicknesses studied. This observation can be explained by the high frequency C–V response of the solar

Cell #	A/R	$V_{\rm OC}$ (V)	$J_{\rm SC}~({\rm mA/cm^2})$	FF	η%	
1L	No	0.55	30.00	0.60	9.9	
2L	No	0.55	30.00	0.64	10.6	
1LAR	Yes	0.55	34.80	0.60	11.4	

Table 5 Photovoltaic properties of large area sputtered a-Si/c-Si solar cells

cells. The zero bias depletion width (Table 2) for the cell fabricated on the 1–10 Ω cm substrate is 0.65 μ m while that for the cells on the 0.1–0.3 Ω cm wafer is 0.3 μ m. Since the extent of the depletion width essentially determines the collected current, hence the reduction in current for the 0.1–0.3 Ω cm wafer.

(c) Effect of plasma power: Cells #1SP, 8SP and 9SP in Table 5 show the PV properties as a function of the sputter power. Cells fabricated at 48 and 64 W show similar characteristics, but for 90 W power the V_{OC} , J_{SC} and FF are severely reduced. Fig. 8d shows the absolute photocurrent as a function of wavelength for the three powers. As seen, the sputtering at 64 W yields the largest response and shows a rather large differential when compared with the sputtering performed at 48 W. The response at 90 W is low for all the wavelengths. Generation/collection studies were again performed by evaluating the response under various reverse biases. Fig. 8a-Fig. 8c show the normalized photocurrent for the three cells. Cells made at 64 W also show slightly better collection than those fabricated at 48 W over all the wavelengths. One other difference that arises is that the red response of cells made at 48 W is about 2 times the blue response, but for 64 W this ratio stands at about 4. The apparent discrepancy in the spectral response of cells sputtered at 48 and 64 W power, in that the generation and collection for the latter being better, can be explained as follows. It was observed that for sputtering performed at 64 W that after the power was set and the shutter opened for deposition, the power actually dropped to 45 W for a few seconds before it stabilized at its preset value of 64 W. This would result in the formation of an a-Si/c-Si interface with lower defects. Since, the a-Si sputtered at higher powers shows a higher conductivity, it is plausible that resulting cells fabricated at 64 W are better in comparison to the cell fabricated at 48 W. In fact, this technique is being used to fabricate large area solar cells. In Fig. 8c, for the cells fabricated at 90 W, the generation increases from 0.4 to 0.55 µm, but reduces for longer wavelengths. The collection efficiency, on the other hand, is low for all the wavelengths, especially in the $0.5-0.6 \mu m$ region. Thus, the interface damage results in lowered generation and collection for the wavelengths that would be predominantly absorbed in the interfacial region.

(d) Effect of SiO_2 at the interface: To study the effect of an oxide layer at the interface, a thermal oxide was grown onto the wafer during the sintering of the back Al contact. Ellipsometry indicated ~ 15 Å of SiO₂ on the wafer surface. Solar cells were fabricated in a method akin to that for cell #1SP. As can be observed in the Table 4, the PV properties of this cell (#10SP), especially J_{SC} and FF, reduce



Fig. 8. (a)-(c) Normalized and (d) absolute photocurrent variation for sputtered a-Si/c-Si solar cells for sputter powers of 48, 64, and 98 W.



Fig. 9. High frequency C-V of a-Si/SiO₂/c-Si type structure for various oxide thicknesses.

dramatically. Thin oxide layers at the interface are easily detectable by 1 MHz C-V measurements of the solar cell. Fig. 9 shows the C-V data for three cells. Cell #1SP had no oxide, cell #9SP has 20 Å of SiO₂, and another cell was prepared which had 100 Å of SiO₂. Only for the cell with 100 Å of SiO₂ does the C-V characteristics show the classic MOS type behavior. For the cell with 20 Å SiO₂, the capacitance follows that for the no oxide cell in high reverse bias, but large deviations occur for smaller reverse biases. It appears that the depletion width in c-Si reduces rapidly for the low reverse biases and has very low equilibrium values. In effect, the presence of thin oxide layers hampers the depletion width spread in c-Si and this in turn resulted in very low collection properties of the devices. These cells also show a lower V_{OC} , which could be a result of voltage loss across the oxide layer.

(e) Large area cells: In fabricating the large area solar cells, all the conditions leading to the formation of good cells have been utilized. The substrate was BHF/DI water passivated just prior to loading for sputtering. The amorphous layer was deposited by

starting the sputtering at powers of 48 W to form a good interface and then increased to 64 W to complete the required thickness of 300 Å. The ohmic contacts were formed with Au/Mg grid and 700 Å of SiO₂ was deposited as an A/R coating. Table 5 shows some of the properties of the solar cells fabricated on 1–10 Ω cm substrates using a 0.02 Ω cm target. The cells are ~ 0.3 cm² in area. The cell #2L has been fabricated with a new US-II type gun. As seen from the table, the fabrication conditions of low interface damage yield cells with high $J_{\rm SC}$ of 30 mA/cm² and FF of ~ 0.6. Efficiencies of 11.4% were obtained (Cell #1LAR) with 700 Å of SiO₂ deposited on the cells as an A/R coating by a reactive evaporation process.

4. Conclusions

Solar cells have been fabricated by depositing a-Si:H by both RF glow discharge and DC magnetron sputtering. The following conclusions have been drawn from the glow discharge n^+a -Si/i a-Si/p c-Si type solar cells.

(i) A good a-Si/c-Si interface is perhaps the most important requirement to obtain a good working cell. Severely interface-limited solar cells mask the effect of a-Si:H thickness and doping in the substrate; probably, a result of the band-bending at the interface. This manifests as very poor collection and hence low J_{SC} in the devices.

(ii) Thin SiO₂ layers seem to be the most common cause for interface limitations. A HF treatment of the wafer just prior to the loading of the sample for the amorphous layer causes J_{SC} to improve from 2.7 to 25 mA/cm², and V_{OC} to improve from 0.4 to 0.55 V. This improvement could be due to removal of native oxide from c-Si and subsequent passivation of the dangling bonds by the HF treatment.

(iii) The dark I-V characteristics of the devices HF treated or untreated look remarkably the same at room temperature and carrier transport seems to agree with the MTCE model. Only the very severely interface-limited devices can be differentiated from their I-V behavior at room temperature.

(iv) High frequency C-V response of the devices not treated with HF was found to deviate significantly from the abrupt heterojunction model. For the HF passivated devices, the capacitance values suggest a 0.55 µm depletion width in c-Si for a 0.1 µm a-Si layer deposited on a 1–10 Ω cm substrate. This value reduces to 0.07 µm for a 0.1–0.3 Ω cm substrate.

Sputtering of n type a-Si:H with n type targets also results in good heterodiodes. High frequency C-V measurements indicate that a 0.5–0.6 µm thick depletion region exists in c-Si at zero bias. 300 Å of sputtered silicon has thus far yielded the most consistent and repeatable results. The nature of the devices indicates that the major absorption of light takes place in the c-Si region.

Specific conclusions from sputtering of a-Si are as follows.

(i) Dark I-V data show an additional transport mechanism not observed in glow discharge deposited samples. It has been postulated that the one region seen for forward bias < 0.4 V reflects tunneling in the amorphous layers, and the region between 0.4 and 0.6 V reflects the extent of the states at the a-Si/c-Si interface.

(ii) High frequency C-V analysis shows that fairly abrupt heterojunctions are obtained by sputtering. For devices having good PV properties, depletion widths of 0.5–0.63 µm are observed. The defect density in a-Si obtained by ideal heterojunction theory is about 4×10^{16} /cm³.

(iii) Spectral analysis at constant photon intensity indicates that thicker a-Si layers result in greater recombination for photons of all wavelengths, but the effect is more so for the longer wavelengths. Degradation of the response starts with even 500 Å of a-Si and becomes very pronounced for 900 Å thick amorphous layers. Severe interface damage is observed for sputtering powers of 90 W. As a result, carrier collection is affected for wavelengths greater than 0.55 μ m. The best response is observed for an intermediate power of 64 W.

(iv) Presence of ~ 15 Å oxide at the interface reduces the J_{sc} from 25 to 0.5 mA/cm². Thin oxides severely reduce the zero-bias depletion width in c-Si.

(v) Solar cells with an area of 0.3 cm^2 having a J_{SC} of 34.80 mA/cm², V_{OC} of 0.55 V, and an FF of 0.60 were fabricated from the processing conditions developed from the analysis of the small area cells.

Acknowledgements

The authors acknowledge financial support for this project by National Renewable Energy Laboratory and New York State Energy Research and Development Authority.

References

- [1] S. Guha, Proc. 25th IEEE PVSC, 1996, p. 1017.
- [2] T. Baba, T. Matsuyama, T. Sawada, T. Takahama, K. Wakisaka, S. Tsuda, S. Nakano, Proc. 24th IEEE PVSC, Vol. 2, 1994, p. 1315.
- [3] R. Wallace, W.A. Anderson, K.M. Jones, R. Ahrenkiel, Proc. 25th IEEE PVSC, 1996, 697.
- [4] C.C. Tsai, R. Thompson, C. Doland, F.A. Ponce, G.B. Anderson, B. Wacker, Mater. Res. Soc. Symp Proc. 118 (1988) 49.
- [5] K.C. Wang, H.L. Hwang, P.T. Leong, T.R. Yew, J. Appl. Phys. 77 (1995) 6542.
- [6] M. Yabe, N. Sato, Y. Seki, in: S. Kataoka (Ed.), Proc. 4th Sensor Symp., 1984, p. 105.
- [7] J. Symons, J. Nijis, R.P. Mertens, IEEE Trans. Electron. Dev. ED 36 (1989) 2889.
- [8] M. Tanaka, M. Taguchi, T. Matuyama, T. Sawada, S. Tsuda, S. Nakano, H. Hanafusa, Y. Kuwano, Jpn. J. Appl. Phys. 31 (1992) 3518.
- [9] D. Fisher, S. Dubail, J.A.A. Selvan, N.P. Vaucher, R. Platz, C. Hof, U. Kroll, J. Meier, P. Torres, H. Keppner, N. Wyrsch, M. Goetz, A. Shah, K.D. Ufert, Proc. 25th IEEE PVSC, 1996, p. 1053.
- [10] N. Sridhar, D.D.L. Chung, W.A. Anderson, J. Coleman, J. Electron. Mater. 24 (1995) 1451.
- [11] J. Yi, Ph.D. Dissertation, State Univ. New York at Buffalo, 1994.
- [12] K. Lai, M.Y. Hao, W.M. Chen, J.C. Lee, IEEE Electron Dev. Lett. 15 (1994) 446.
- [13] N. Hirashita, M. Kinoshita, I. Aikawa, T. Ajioka, Appl. Phys. Lett. 56 (1990) 451.
- [14] B. Jagannathan, W.A. Anderson, Solar Cells and Materials, accepted for publication.
- [15] H. Matsuura, T. Okuno, H. Okushi, K. Tanaka, J. Appl. Phys. 55 (1994) 1012.
- [16] D.K. Sharma, K.L. Narasimhan, Phil. Mag. B 63 (1991) 543.
- [17] M. Pinarbasi, N. Maley, A. Myers, J.R. Abelson, Thin Solid Films 171 (1989) 217.