

**Ultrahigh-Density Nanowire Lattices and Circuits**Nicholas A. Melosh, *et al.**Science* **300**, 112 (2003);

DOI: 10.1126/science.1081940

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11. Monoclonal antibody [mouse immunoglobulin G (IgG)] against *S. typhimurium* CIC (StCIC) was obtained as described (23). Total messenger RNA was isolated from the mouse hybridoma cells using TRIzol reagents (Gibco BRL). The DNA encoding the variable region of the antibody was obtained by reverse transcription polymerase chain reaction (RT-PCR) by the 5' RACE system (Gibco BRL). The antibody was sequenced using the RT-PCR product as template. *E. coli* CIC was purified in the detergent decylmaltoside (DM) as described (10). Mouse IgG was purified from mouse hybridoma cell culture supernatant using ion exchange chromatography (Q-sepharose, Pharmacia). Fab fragments were obtained by papain proteolysis followed by Q-sepharose chromatography. *E. coli* CIC and Fab were mixed in an OD₂₈₀ ratio of 1:2.3. The complex was purified on a Superdex 200 column (Pharmacia) equilibrated in 150 mM NaCl, 10 mM tris-HCl (pH 7.5), and 10 mM DM. For crystallization, the NaCl concentration was lowered to 90 mM by dilution. For preparation of crystals in NaBr, the protein was dialyzed against a solution containing 90 mM NaBr. Crystals of the *E. coli* CIC Fab complex were grown in sitting drops at 20°C by equilibrating a 1:1 mixture of protein and reservoir solutions against the reservoir. The reservoir contained 28 to 31% polyethylene glycol (PEG 300), 50 mM glycine (pH 9.5), and 100 mM NaCl. For crystals grown in Br⁻, NaCl was replaced by NaBr. Crystals were frozen in a stream of boiled-off nitrogen. The PEG 300 concentration was raised to 35% by dialysis before freezing. All data sets were collected on frozen crystals.
12. Point mutations were introduced by the QuikChange method (Stratagene) and confirmed by sequencing of the entire DNA insert. Capped RNA was transcribed from wild-type and mutated CIC-0 and injected into *Xenopus* oocytes. After 1 day, currents were measured by a two-electrode voltage clamp (OC-725B, Warner Instrument Corp.). Electrodes had a resistance of ~0.5 megohms (3 M KCl). The bath solutions contained 5 mM Hepes (pH 7.5), 2 mM MgCl₂, and 100 mM NaCl. For experiments at pH 5.0, Hepes was replaced with 5 mM citrate.
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23 January 2003; accepted 11 March 2003

Published online 20 March 2003;

10.1126/science.1082708

Include this information when citing this paper.

REPORTS

Ultrahigh-Density Nanowire Lattices and Circuits

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We describe a general method for producing ultrahigh-density arrays of aligned metal and semiconductor nanowires and nanowire circuits. The technique is based on translating thin film growth thickness control into planar wire arrays. Nanowires were fabricated with diameters and pitches (center-to-center distances) as small as 8 nanometers and 16 nanometers, respectively. The nanowires have high aspect ratios (up to 10⁶), and the process can be carried out multiple times to produce simple circuits of crossed nanowires with a nanowire junction density in excess of 10¹¹ per square centimeter. The nanowires can also be used in nanomechanical devices; a high-frequency nanomechanical resonator is demonstrated.

One of the great challenges in developing nanofabrication patterning techniques involves the reduction of feature size, and the corresponding

increase in pattern density, of various metal and semiconductor structures. Such device scaling has often been demonstrated as the most productive route toward developing more efficient and faster electronics circuitry. In addition, there is also the hope of eventually developing patterning techniques that begin to approach the feature sizes and densities that are characteristic of macromolecules. Such approaches would open up new opportunities for constructing devices and circuits that can interface with, for example,

biological systems. To this end, a tremendous amount of effort has been put into reducing the feature sizes of the traditional, parallel patterning techniques of photolithography, as well as more specialized, serial patterning approaches such as electron beam lithography (EBL). All of these approaches face fundamental challenges, but for one-of-a-kind devices, EBL is the highest resolution technique available (1).

Standard metrics for the resolution of a patterning process are the line width and center-to-center distance (pitch) of an array of aligned nanowires. EBL has yielded patterns with nanowire diameters as small as 20 nm (1). However, the pitch is limited to ~60 nm because of "noise" in the processing steps required to translate a pattern that has been written into resist material into an actual array of aligned, conducting wires. For example, a thin layer of metal is typically evaporated onto the resist layer, adhering directly to the substrate in the windows patterned through the resist layer. The resist is then dissolved in the appropriate solvent, causing the newly unsupported metal film to tear free, or "lift off," leaving only the metal that was in direct contact with the substrate. However, for very small features, the metal-substrate adhesion area is quite small, and those features may also lift off. This problem is reversed at very small pitches, because the cohesion of the metal film may prevent or disrupt the lift-off process.

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To avoid some of the inherent difficulties in photolithographic procedures, or to overcome the limitations of the serial nature of EBL, researchers have devised nonphotolithographic patterning techniques to achieve wires less than 50 nm in diameter, including nanoimprinting, microcontact printing, and other “soft lithography” methods (2, 3). These procedures are based on direct transfer of a physical pattern—essentially a stamp—to a substrate, either by imprinting into a compliant film or by deposition of molecules. In practice, however, these procedures still rely on photolithography or EBL to fabricate the master stamp, and development of the pattern still involves various lift-off procedures. Thus, such methods may translate the serial method of EBL into a parallel patterning process, but most of the other intrinsic limitations are present.

We demonstrate a technique for fabricating aligned metal nanowires through a one-step deposition process without subsequent etching or lift-off. Further processing steps can translate these metal nanowire patterns into semiconductor nanowires. Our method uses molecular beam epitaxy (MBE) to create a physical template for nanowire patterning, enabling simple physical transfer of fully formed metallic wires from a selectively etched GaAs/Al_{0.8}Ga_{0.2}As superlattice onto a silicon wafer. The wires are defined by evaporating metal directly onto the GaAs layers of the superlattice after selective removal of the AlGaAs to create voids between the GaAs layers. By depositing the metal solely on the GaAs, the wire widths are defined by the thickness of the GaAs layers, and the separation between the wires is defined by the thickness of the AlGaAs layers. Atomic-level control over the thickness and composition of each layer is achieved by synthesizing the GaAs/AlGaAs superlattice via MBE. In this manner, atomically defined templates for metal wires can be fabricated down to 1 nm or less, although wires of

this dimension have not been successfully transferred thus far.

This deposition technique, which we refer to as superlattice nanowire pattern transfer (SNAP), is related to other physical lithographic techniques, with two important advances. First, this method does not rely on photolithography or EBL to define features, hence it can produce thinner wires with much smaller pitches than can be fabricated even with EBL. Second, a metal lift-off step is not needed because fully separated metal lines are directly deposited. Avoiding this step greatly enhances our ability to fabricate wires at very small separations, where previously metal adhesion limited the possible wire pitch. In addition, the metal wires themselves can be used as etch masks to transfer the nanowire pattern to an underlying semiconductor substrate, such as silicon-on-SiO₂ (SOI) wafers, thereby generalizing this technique for both metal and semiconductor wires. Finally, the selectively etched GaAs/AlGaAs superlattice may also find uses as a master stamp for other physical lithographic techniques such as nanoimprinting.

The SNAP synthetic procedure is illustrated in Fig. 1. A GaAs/Al_{0.8}Ga_{0.2}As superlattice was grown on the [100] surface of a GaAs substrate with the use of MBE techniques. A dilute mixture of buffered hydrofluoric acid (15 ml of 6:1 buffered oxide etchant, 50 ml of H₂O) was used to selectively etch the AlGaAs layers roughly 20 to 30 nm deep (4). Metal wires were then evaporated onto the top of the GaAs layers by orienting the superlattice at 36° with respect to the evaporative flux within the vacuum chamber of an electron beam metal evaporation system. This tilt caused the metal to be deposited only on the GaAs layers because of their elevation relative to the etched AlGaAs layers. Gold, chromium, aluminum, titanium, niobium, platinum, and nickel wires were all used in this study; however, a variety of other metals are also expected to work.

Transfer of the metal wires to a silicon wafer was performed by contacting the metal-coated GaAs/AlGaAs superlattice to a

heat-curable epoxy film 10 nm thick, supported on an oxidized silicon wafer; the epoxy served as an adhesion layer. The epoxy was cured at 150°C for 30 min, after which the sample was suspended upside down in a solution of KI (4 g)/I₂ (1 g)/H₂O (100 ml) to remove the GaAs oxide layer at the nanowire-GaAs interface (5). The silicon wafer was removed, rinsed, and dried. A brief O₂ plasma etch effectively removed the residual epoxy layer, if necessary.

Wires deposited with this technique were uniform and continuous over the 2- to 3-mm length of the GaAs superlattices, with remarkably few defects. Figure 2, A and B, shows scanning electron microscopy (SEM) images of two sets of Pt wires: 40 wires 10 nm in diameter at a pitch of 60 nm, and 20 wires 10 nm in diameter at a pitch of 30 nm (6). Figure 2C is an image of the highest density nanowire patterns we have fabricated: 20 Pt wires 8 nm in diameter at a pitch of 16 nm. All wires shown in Fig. 2 are straight; they do not cross or touch, and they show no visible defects over stretches greater than 100 μm. The color variegations observed in the SEM images are attributed to slight height variations due to nonuniform curing of the epoxy. Upon higher magnification (Fig. 2C), it is apparent that the wires are fully intact. The wires have distinct sidewalls, sharp edges, and uniform widths and separations. We attribute these characteristics to the well-defined shape of the superlattice used to create these wires. Aside from gold wires, which show some structural evolution over time, the metal is quite smooth and continuous. The defects observed most often are small voids, presumably from contaminants in the fabrication process. The smallest wires, when fabricated at a pitch of 20 nm or less, do show some slight variations in alignment, but even those generally do not touch over 10-μm distances.

Several methods exist to create nanowires of similar dimensions, but organizing these wires into highly ordered arrays with predetermined spacing and registry has been ex-

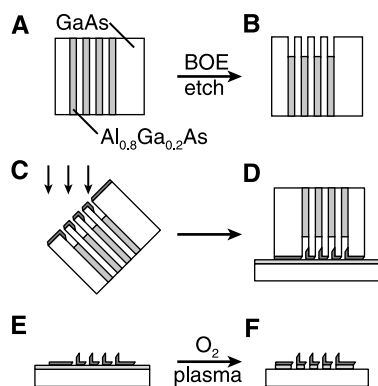


Fig. 1. Process diagram to create small pitch wires. (A) The GaAs/AlGaAs superlattice, (B) after selectively etching the AlGaAs, (C) metal deposition while tilted at 36°, (D) contact of superlattice onto adhesive layer on silicon, (E) release of metal wires by etching GaAs oxide, and (F) after optional O₂ plasma to remove adhesive layer.

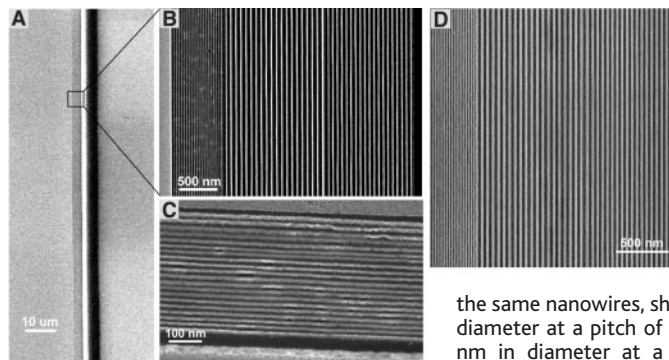


Fig. 2. Aligned Pt nanowire arrays produced using the SNAP process. (A) An electron micrograph of a ~100-μm section of an array of 60 nanowires. The bright line next to the nanowires is due to residual epoxy. (B) A higher resolution micrograph of the same nanowires, showing 40 Pt wires 10 nm in diameter at a pitch of 60 nm, and 20 Pt wires 10 nm in diameter at a pitch of 30 nm. (C) The highest density nanowire array fabricated with the same nanowires, showing 20 Pt wires 8 nm in diameter at a pitch of 16 nm. (D) SEM image of SOI silicon nanowires.

The 19 wires at the left are 18 nm wide at 30 nm pitch; the 40 wires at the right are 20 nm wide at 60 nm pitch. These wires were straight and continuous for >100-μm stretches.

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tremely challenging (7, 8). For technological applications, it is necessary not only to have nanoscale wire widths but also to know the location and registry between wires precisely. Otherwise, every time electrical contact to the nanowires is to be made, the beginning and end locations of every single nanowire must be determined and the contacts patterned specifically for each wire. The SNAP wires have precise beginning and ending locations based on the superlattice template, allowing contact to the wires in a predetermined manner.

The SNAP nanowire arrays are robust to further fabrication steps. For example, electrical contacts to the nanowires can be established for current-voltage measurements, which are crucial for electronic applications. The metal nanowires can be used as etch masks to transfer the wire pattern to an underlying thin film, such as SOI, to form semiconductor nanowires. Nanowire arrays can be suspended over a trench to fabricate high-frequency nanomechanical resonators. The SNAP process can also be repeated multiple times to make high-density nanowire crossbar circuits.

Many additional scientific and technological studies could be performed if the SNAP process could be modified to fabricate semiconducting nanowires. For certain ion-based etching processes, metal structures serve as excellent etch masks, and so we explored the possibility of extending SNAP nanowire patterns to create silicon and poly-Si nanowires. In this case, metal SNAP nanowires are deposited onto a substrate coated with a thin film of the desired wire material on top—for instance, silicon-on-insulator. Reactive ion etching (RIE) was used to remove the thin film material located between, but not under, the metallic wires deposited on top (9). This method extends SNAP to produce wires from almost any thin film material that can be directionally etched. Silicon wires fabricated in this manner, 18 nm or 20 nm wide with pitches of 30 and 60 nm, respectively, are shown in Fig. 2D. Just like the metallic template, these wires are straight and continuous for tens to hundreds of micrometers, showing good separation and well-defined edges. Because all the wires are exactly the same height (determined by the initial film thickness) and are free of epoxy, no

color variations along the wires are observed.

Electrical conductivity was measured by sectioning the metal or Si nanowires into 10- to 20- μm lengths by RIE, and electrical contacts were fabricated by EBL (10). The semiconductor wires were chemically bonded to the underlying substrate but the metal wires were not; hence, this exercise was not only a check against their transport characteristics but also a check against how processing steps such as resist spinning might disrupt the alignment of an array. In fact, all wire types were stable to all of the processing steps. Pt wires exhibited metallic conductance down to temperatures of 4 K, indicating that clean electrical contacts unperturbed by organic residue from the epoxy were established. Typical room-temperature resistance values were 8 to 10 kilohms for a single Pt wire 6 μm long and 15 nm in diameter (Fig. 3A), slightly more than the theoretical bulk value of 5 kilohms. For the silicon and poly-Si wires, several wires were measured in parallel and exhibited linear current-voltage scans (Fig. 3B). Resistance for a wire 20 nm wide was ~ 2 megohms at phosphorus doping densities of 10^{19} cm^{-3} , about a factor of 4 higher than the theoretical bulk value of 780 kilohms (11). We attribute the increased resistance to damage caused by RIE. Electrical isolation between sets of wires was extremely good, greater than 10,000 gigohms for silicon wires separated by five wires from one another (Fig. 3B, gray trace).

These nanowires can be used as high-frequency nanomechanical resonators. A rectangular wire suspended across a gap is expected to have a resonance frequency ω_{res} that scales with the dimensions of the wire and with the size of the gap according to $\omega_{\text{res}} = (c_1 t/L^2)(E/\rho)^{1/2}$, where c_1 is a constant of order unity, t is the wire thickness, L is the length suspended, E is Young's modulus, and ρ is density (12). Because of the low mass and variable gap dimension, the resonance frequency of the wires is expected to range from tens of MHz to GHz.

Pt nanowire resonators were fabricated by selectively undercutting the supporting substrate, thus suspending them over a trench (Fig. 4A). We used the SNAP technique to deposit 20-nm Pt wires at 150-nm pitch onto a bare Si wafer; the epoxy was removed with an O_2 RIE plasma.

Trenches of various widths were patterned over the wires with EBL in polymethyl methacrylate resist. The exposed Si substrate beneath the wires was etched away with XeF_2 gas. The nanowire resonators were electrically contacted, then mounted on the cold finger of a liquid helium cryostat equipped with a superconducting magnet. The sample was then cooled to 4 K and the resonance frequency was measured using a magnetomotive technique (13, 14). Multiple wires were electrically connected together into a single device to increase the signal strength. This undoubtedly increased the measured width of the resonance peak. At zero magnetic field, no induced current (measured as a voltage) was observed, as expected (Fig. 4B). However, increasing the magnetic field strength increases the force on the wires as well as the magnitude of the induced current, corresponding to increased signal intensity. For the 20-nm Pt wires suspended over a 0.75- μm trench shown here, ω_{res} was ~ 162.5 MHz. The calculated ω_{res} is 99 MHz, with the difference likely arising

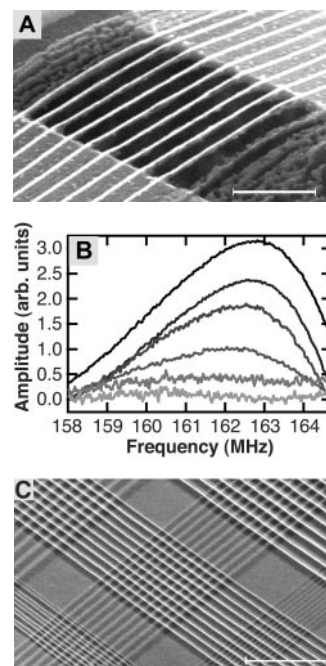
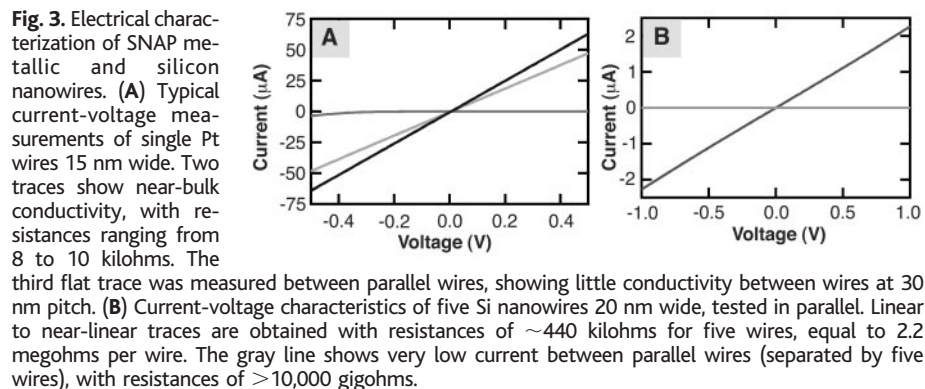


Fig. 4. A high-frequency nanomechanical resonator fabricated by the SNAP process. (A) The resonator contains nine Pt nanowires 20 nm in diameter suspended over a 0.75- μm gap. (B) A resonance frequency (ω_{res}) of ~ 162.5 MHz is monitored as a function of increasing field strength, from 0 to 5 T. The 0-field measurement is subtracted from each of the readings. The response increases with field strength, with the 5-T recording presented as the darkest trace. (C) Electron micrograph of a few hundred Pt nanowire crossbar circuits fabricated by repeating the SNAP process. The crossbars are fabricated from Pt nanowires with pitches ranging from 20 to 80 nm. The central crossbar has a junction density of $\sim 5 \times 10^{10} \text{ cm}^{-2}$, and the two crossbars to the lower left and right of this central one are at a junction density of $\sim 10^{11} \text{ cm}^{-2}$. Scale bars in (A) and (C), 500 nm.

from additional tension in the wires. With a reasonable reduction of resonator lengths to 0.25 μm , it should be possible to fabricate resonators with $\omega_{\text{res}} \sim 2.5$ GHz.

As a final demonstration of the flexibility of the SNAP process, the process was repeated to fabricate ultradense crossbar circuit elements. As discussed above, one intrinsic advantage of the SNAP process is that it is a direct transfer of prefabricated nanowires, enabling many patterns to be deposited on top of one another. A second advantage of the SNAP process is related to the extremely high aspect ratio of the nanowire arrays. Because the arrays are so long (mm lengths), the only critical alignment between a top and bottom pattern is the angle between the two patterns. In other words, no particular spatial alignment is needed even to fabricate crossbar structures at densities in excess of 10^{11} junctions cm^{-2} . Figure 4C is an electron micrograph of several crossbar circuits fabricated by repeating the SNAP process at 90° to each other. An obvious limitation of the SNAP process is that it can only produce crossbar circuits (or other relatively simple structures). However, the crossbar has emerged as the circuit of choice for a number of nanoelectronic applications (15), such as molecular switch-based random access memory (16) or nanowire-based logic circuits (17, 18).

Many applications are possible with the combination of nanowire materials, diameters, pitches, and aspect ratios that the SNAP approach yields. Possibilities include one-dimensional superconductors, high-density semiconductor nanowire sensor arrays, gigahertz nanomechanical resonators, and high-density molecular electronics circuits. However, one critical issue that must be faced if this approach is to be fully exploited is the task of individually addressing each nanowire within a small pitch array. The SNAP technique can generate wiring networks that are well beyond the resolution of even EBL. Thus, this approach brings into focus the problem of interfacing the micrometer or sub-micrometer world of lithography and the macromolecular-type densities achievable with this technique. This is one of the outstanding problems in nanotechnology, but potential solutions, such as binary tree demultiplexers, have been proposed (19). Building such demultiplexers, with less stringent (>50 nm) requirements in terms of the pitch and alignment of the electrical connections (an essential requirement), will be a major challenge.

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4. We have reproduced this technique on more than a dozen commercially purchased and grown-in-house superlattices, and we have found that there is appreciable chemical variability from wafer to wafer, with a corresponding variability in etch chemistry.
5. Currently the superlattice is not being reused because of the small amount necessary for each imprint.

However, polishing of GaAs/AlGaAs superlattices is well established for laser devices and may be useful here.

6. The brightness/contrast of the SEM images was adjusted, but no other image processing was used.
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9. Typical Si and poly-Si thin films were 30 to 50 nm thick and were etched using Cl_2 RIE at low power (80 W) and pressure (5 mT) to carefully control the etch rate.
10. Contacts were made by using EBL to define ~ 100 -nm wires placed on either side of the etched portion of the wire array. Accurate placement of the contact wires was achieved with the use of predeposited alignment markers. Wires with narrow pitch (<80 nm) could generally not be individually addressed this way because of the resolution limits of EBL. Contact of a single wire was achieved by depositing electrodes onto all the wires in parallel, then using a focused ion beam to cut all but one wire between the electrodes.
11. The metal nanowires (>15 nm wide) exhibited consistent bulk metallic conductivity to 4 K; smaller wires could not be measured individually. The conductivity of the SOI nanowires fluctuated much more widely, depending on the processing conditions and nanowire crystallographic orientation.

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20. Supported by the Office of Naval Research and the Defense Advanced Research Projects Agency. We thank M. Roukes and his group for teaching us how to perform high-frequency nanomechanical resonator measurements.

27 December 2002; accepted 4 March 2003

Published online 13 March 2003;

10.1126/science.1081940

Include this information when citing this paper.

Recognition of Paleoearthquakes on the Puente Hills Blind Thrust Fault, California

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Borehole data from young sediments folded above the Puente Hills blind thrust fault beneath Los Angeles reveal that the folding extends to the surface as a discrete zone (≤ 145 meters wide). Buried fold scarps within an upward-narrowing zone of deformation, which extends from the upward termination of the thrust ramp at 3 kilometers depth to the surface, document the occurrence of at least four large (moment-magnitude 7.2 to 7.5) earthquakes on this fault during the past 11,000 years. Future events of this type pose a seismic hazard to metropolitan Los Angeles. Moreover, the methods developed in this study can be used to refine seismic hazard assessments of blind thrusts in other metropolitan regions.

During the past 30 years, paleoseismology (the study of ancient earthquakes) has provided a wealth of information on the locations, magnitudes, and dates of earthquakes (1, 2). These data are critical for probabilistic seismic hazard assessments, which dictate modern hazard zoning, emergency response, and risk mitigation strategies. Previous paleoseismological studies, however, have largely neglected an entire class of faults—the so-called blind thrust faults. These faults do not extend all the way to the surface,

and shortening in the near-surface is accommodated by folding rather than by fault slip (3–6). The absence of paleoearthquake age and displacement data from blind thrust faults creates a major gap both in our understanding of the collective behavior of regional fault systems and in our ability to construct accurate seismic hazard models. Here we document the ages and displacements of individual paleoearthquakes on a major, active blind thrust fault.

Our study focused on the Puente Hills thrust (PHT), a major blind fault beneath metropolitan Los Angeles, California (7). Extensive petroleum-industry seismic reflection and well data, relocated earthquakes, and geomorphologic observations demonstrate that the PHT, which dips gently northeastward and terminates upward at a depth of ~ 3 km, extends for 40 to 50 km from northern Orange County, beneath downtown Los

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