Journal of
Nanoscience and Nanotechnology
Vol. 10, 6363–6368, 2010

Light Extraction Efficiency Enhancement of GaN-Based Light Emitting Diodes on *n*-GaN Layer Using a SiO_2 Photonic Quasi-Crystal Overgrowth

H. W. Huang[1, 2, *], K. Y. Lee[2], J. K. Huang[1], C. H. Lin[2], C. F. Lin[3], C. C. Yu[2], and H. C. Kuo[1]

[1] *Institute of Electro-Optical Engineering, National Chiao-Tung University, Hsinchu 30050, Taiwan, R.O.C*
[2] *Luxtaltek Corporation, Chunan, Miaoli 350, Taiwan, R.O.C*
[3] *Department of Material Engineering, National Chung Hsing University, Taichung, 400, Taiwan, R.O.C*

In this paper, GaN-based LEDs with a SiO_2 photonic quasi-crystal (PQC) pattern on an *n*-GaN layer by nano-imprint lithography (NIL) are fabricated and investigated. At a driving current of 20 mA on Transistor Outline (TO)-can package, the better light output power of LED III ($d = 1.2$ μm) was enhanced by a factor of 1.20. After 1000 h life test (55 °C/50 mA) condition, Normalized output power of LED with a SiO_2 PQC pattern (LED III ($d = 1.2$ μm)) on an *n*-GaN layer only decreased by 5%. This results offer promising potential to enhance the light output power of commercial light-emitting devices using the technique of nano-imprint lithography.

Keywords: GaN, Light Emitting Diodes (LEDs), Photonic Quasi-Crystal (PQC), Nano-Imprint Lithography (NIL).

RESEARCH ARTICLE

1. INTRODUCTION

Impressive recent developments of high brightness light extraction of GaN-based nitride light-emitting diodes LEDs is dominated on both material techniques such as metal organic chemical vapor deposition (MOCVD) epitaxial growth and device fabrication processes. Thus, high brightness LEDs have been used in various applications, including large and small size flat-panel displays backlight, traffic signal light and illumination lighting by white light LEDs.[1–3] In order to get higher brightness of LEDs, extensive research has been conducted. In epitaxial growth method, a number of attempts have been made to reduce the dislocation effect using such strategies as the insertion of a micro-scale epitaxial lateral overgrowth (ELOG) layer of SiO_2 or a Si_xN_y pattern on the GaN thin film[4–6] as well as the use of micro-scale patterned sapphire substrate (PSS).[7–10] Moreover, high quality GaN-based LEDs have been demonstrated on a micro-scale PSS by wet or dry etching,[7–10] where the micro-scale patterns served as a template for the ELOG of GaN and the scattering centers for the guided light. Both the epitaxial crystal quality and the light extraction efficiency were improved by utilizing a micro-scale PSS. Recently, the MOCVD growth of GaN-based LEDs on the PSSs with micro-scale and nano-scale pyramidal patterns has been reported and compared.[11–12] The LEDs grown on the nano-scale PSS showed more enhancements in the external quantum efficiency (EQE) than those grown on the micro-scale PSS. Furthermore, photonic crystal (PhC) is the promising technique due to the great improvement of light extraction efficiency.[13–16] PhC structures were usually fabricated by e-beam lithography,[17] holographic lithography,[18] and nanoimprint lithography.[15, 19] However, the drawbacks of the e-beam and holographic lithography techniques are low throughput. Therefore, a high throughput and economic technique, nanoimprint lithography, was recommended to manufacture the light-emitting devices with PhC or PQC structures.[19]

In this paper, we report the NIL and epitaxial overgrowth techniques to fabricate the GaN-based LEDs using a SiO_2 PQC nano-patterned overgrowth on an *n*-GaN layer for 2-inch mass production. As a result, the intensity-current (L–I) measurements demonstrate that the light output power of LED with a SiO_2 PQC overgrowth on an *n*-GaN layer was higher than that of a conventional LED at 20 mA with standard device processing.

2. EXPERIMENTAL DETAILS

In this experiment, GaN-based LED samples are grown by MOCVD with a rotating-disk reactor (Veeco) on a

*Author to whom correspondence should be addressed.

 1533-4880/2010/10/6363/006 doi:10.1166/jnn.2010.2639

c-axis sapphire (0001) substrate at the growth pressure of 200 mbar. In Figure 1 shows the process flowcharts of a SiO_2 PQC pattern on an *n*-GaN layer by NIL. The LED structure with a 100 nm-thick SiO_2 PQC patterned on an *n*-GaN layer structure to fabricate from sapphire substrate consists of a 50 nm-thick GaN nucleation layer grown at 500 °C, a 2 μm un-doped GaN buffer, a 1.0 μm-thick Si-doped GaN buffer layer grown at 1050 °C. Afterward the sample process sequence starts with Step 1 generating an intermediate polymer stamp (IPS) from a Ni master stamp by a nano-imprint process. The pressure of 30 bar and a temperature of 160 °C were applied to the nano-imprint lithography system for about 5 min. Step 2, we spin coated a 200 nm polymer layer on a 100 nm-thick SiO_2/GaN LED sample surface. Step 3, in a second imprint the IPS is used as a single use template in a simultaneous thermal and UV-process (STU). We placed a PQC patterned mold onto the dried polymer film. By applying high pressure of 40 bar, and UV radiation time of 10 sec, we heated the LED wafer to constant working temperature of 65 °C to transition PQC pattern to the polymer layer. Step 4, the LED samples and the IPS were then cooled down to room temperature to release the IPS. Finally, we use a RIE with CF_4 plasma to remove the residual polymer layer and transfer the pattern onto SiO_2. Then, the LED structures with a SiO_2 PQC overgrowth on an *n*-GaN layer were designed and re-grown on a 2 inch wafer. The re-grown LED structures consisted

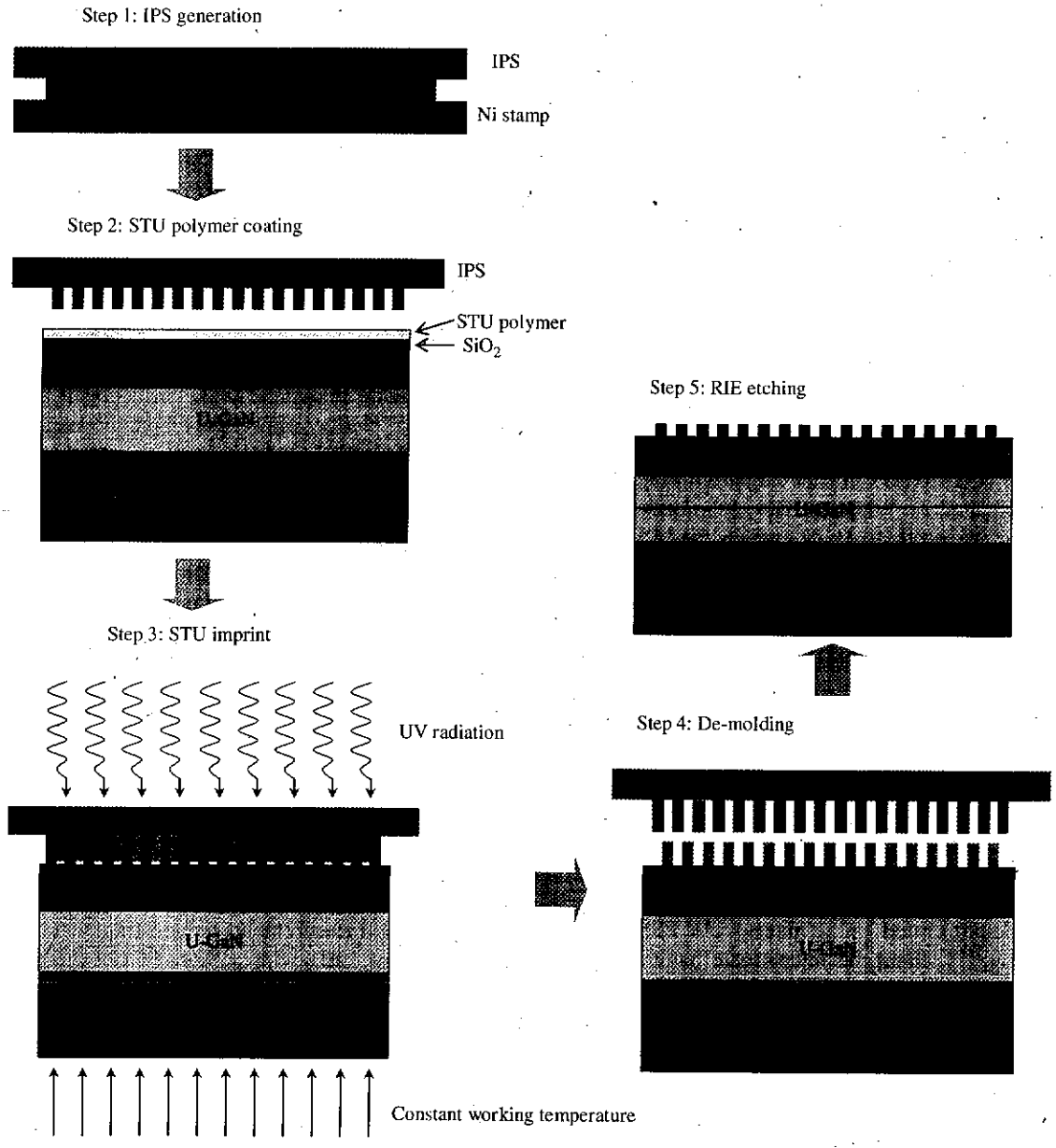

Fig. 1. Process flowcharts of a SiO_2 PQC pattern on an *n*-GaN layer by nano-imprint lithography.

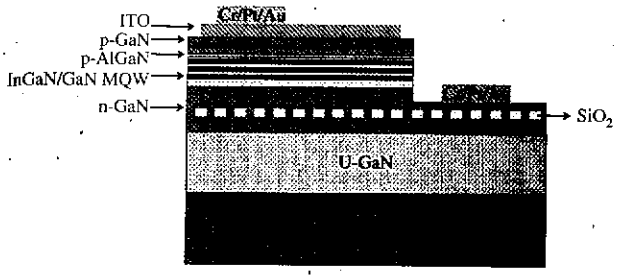

Fig. 2. Schematic diagrams of GaN-based LEDs with a SiO_2 PQC pattern on an *n*-GaN layer.

of a thickness d from 0.3 μm to 1.2 μm thick *n*-type Si-doped GaN layer at 1050 °C, anunintentionally doped InGaN/GaN multiple quantum well (MQW) active region grown at 770 °C, the MQW active region consists of five periods of 3 nm/7 nm-thick $In_{0.18}Ga_{0.82}N$/GaN quantum well layers and barrier layers, a 50 nm-thick Mg-doped *p*-AlGaN electron blocking layer grown at 1050 °C, and a 220 nm-thick Mg-doped *p*-GaN contact layer grown at 1050 °C, which were defined as the SiO_2 photonic quasi-crystal overgrowth on an *n*-GaN layer shown in Figure 2. The conventional LED structure consist of a 50 nm-thick GaN nucleation layer grown at 500 °C, a 2 μm un-doped GaN buffer, a 1.5 μm-thick Si-doped GaN buffer layer grown at 1050 °C, afterward the same epitaxial structure as LEDs with a SiO_2 PQC overgrowth on an *n*-GaN layer.

All the LED samples are fabricated using the following standard processes with a mesa area of 265 μm × 265 μm. A photo-resist layer with thickness of 2 μm is coated onto the LED samples surface by spin coater. Photo-lithography is used to define the mesa pattern. The mesa etching is then performed with Cl_2/BCl_3/Ar etching gas in an inductively coupled plasma reactive ion etching (ICP-RIE) system which transferred the mesa pattern onto *n*-GaN layer and remove photo-resist (PR) using PR stripper solution. After the mesa etching, a 270 nm thick indium-tin-oxide (ITO) layer is subsequently evaporated

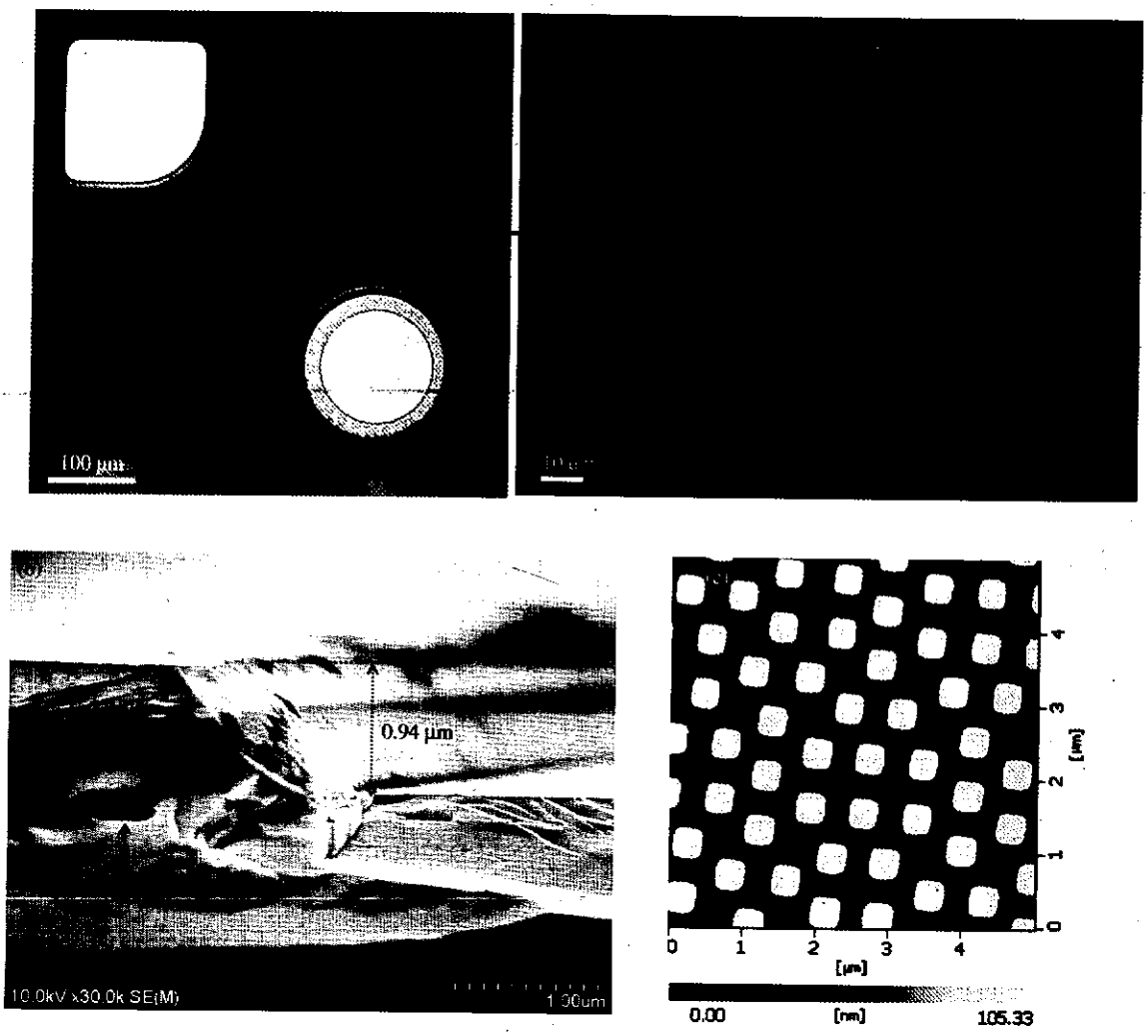

Fig. 3. (a) An OM image of an LED die with a SiO_2 PQC pattern on an *n*-GaN layer, and the tilted plane view OM image between TCL and *n*-side roughing region; (b) Cross-section SEM image of LED with a SiO_2 PQC pattern on an *n*-GaN. (c) Top-view AFM image of a SiO_2 PQC pattern on an *n*-GaN.

onto the LED sample surface. The ITO layer has a high electrical conductivity and a high transparency (>95% at 460 nm). Finally, the Cr/Pt/Au (30/50/1400 nm) contact metal is subsequently deposited onto the exposed n- and p-type GaN layers to serve as the n- and p-type electrodes.

The left-side image of Figure 3(a) is an optical micrograph (OM) image of LED die with a SiO_2 PQC pattern on an n-GaN layer (LED chip area of 300 μm × 300 μm). The right-side image of Figure 3(a) is the top-view OM image between the ITO transparent contact layer (TCL) and n-side surface regions. In right-side image of Figure 3(a), the chip surface of GaN-based LED with a SiO_2 PQC pattern was distinct between the ITO and n-GaN region. The cross-section scanning electron microscopy (SEM) picture of the LED with a SiO_2 PQC pattern on an n-GaN layer is shown in Figure 3(b). The SEM image in Figure 3(b) shows the thickness of the SiO_2 layer was approximately 100 nm, and the height of the etching depth of mesa was approximately 0.94 μm. The Figure 3(c) shows the top-view atomic force microscopy (AFM) image of 12-fold PQC based on square–triangular lattice. We choose the 12-fold PQC pattern due to the better enhancement of surface emission was obtained from the PhCs with a dodecagonal symmetric quasi-crystal lattice than regular PhCs with triangular lattice and 8-fold PQC.[20] The recursive tiling of offspring dodecagons packed with random ensembles of squares and triangles in dilated parent cells forms the lattice. Additionally, in this case we using the PQC rod dimension and pattern pitch (a) were approximately 435 nm and 750 nm, and the hole diameter (D) fixed to ratio $D/a = 0.58$.

3. RESULTS AND DISCUSSION

Figure 4(a) shows the typical current–voltage (I–V) characteristics. It is found that the measured forward voltages under injection current 20 mA at room temperature for conventional LED, LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm) were 3.11, 3.14, 3.10, and 3.09 V, respectively. In addition, the dynamic resistance of conventional LED, LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm) are about 16.0, 16.8, 16.7, and 16.7 Ω, respectively. Therefore, in terms of dynamic resistance, there is no influence on this type of devices by incorporating PQC structure. Besides, the inset graph of Figure 4(a) is the electroluminescence (EL) intensity–current characteristics of conventional LED, LED I (d thickness from 0.3 μm to 1.2 μm). The top luminance intensities of the LEDs on wafer were detected using the top-side photo-detectors. It was found that the top-side luminance intensities of the conventional LED, LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm) presented data of 70, 86, 98, and 104 mcd at 20 mA, respectively. Therefore, the top-side luminance intensity of the LED I ($d = 0.3$ μm), LED II

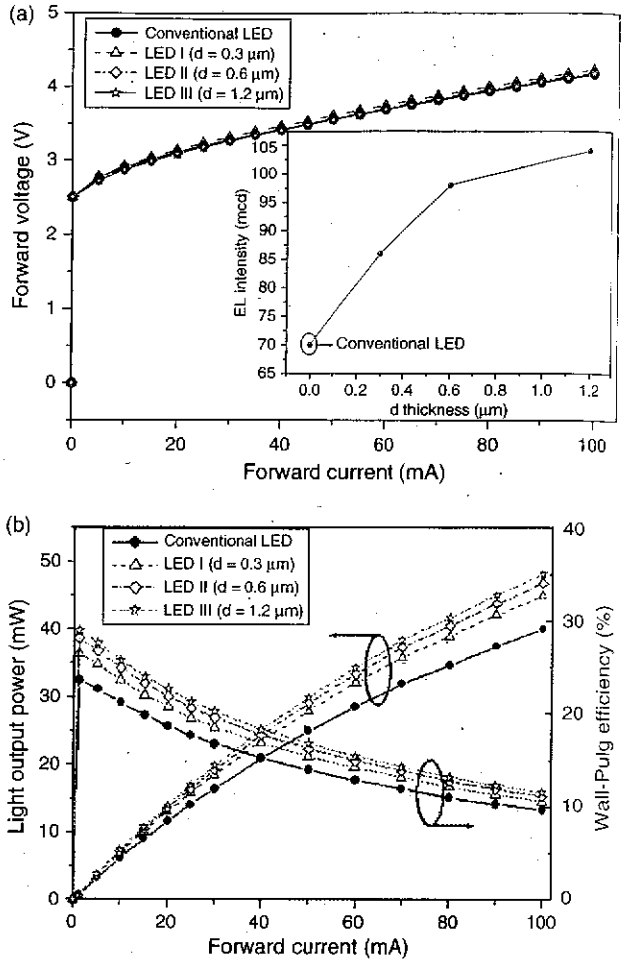

Fig. 4. (a) Shows the current–voltage (I–V) characteristics of conventional LED, LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm), respectively. (the inset data was measurement EL intensity–current); (b) Light output power–current (L–I) and wall-plug efficiency (WPE) characteristics of LED with/without a SiO_2 PQC structure on an n-GaN layer, respectively.

($d = 0.6$ μm), and LED III ($d = 1.2$ μm) increased 23%, 40%, and 48% in magnitude as compared with that of the conventional LEDs. The higher EL intensity on LED III ($d = 1.2$ μm) which maybe allows the reflect light from a SiO_2 PQC layer onto the top direction and higher epitaxial crystal quality.[20–21]

The light output is detected by calibrating an integrating sphere with Si photodiode on the package device, so that light emitted in all directions from the LED can be collected. The intensity–current (L–I) characteristics of the LEDs with and without PQC structure are shown in Figure 4(b). At an injection current of 20 mA and peak wavelength of 460 nm for TO-can package, the light output powers of conventional LED, LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm) on TO-can are given by 11.6, 13.0, 13.5, and 13.9 mW, respectively. Hence, the enhancement percentages of LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm) were 12%, 16%, 20%, respectively, compared to that of

conventional LED. The higher enhancement on LED III ($d = 1.2$ μm) were the reflect light from oxide PQC layer onto the top direction and higher epitaxial crystal quality[20–21] to increase more light output power. In addition, the corresponding wall-plug efficiencies (WPE) of conventional LED, LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm) were 19%, 21%, 22%, and 23%, respectively, which addresses a substantially improvement by a SiO_2 PQC pattern on an n-GaN layer as well at a driving current of 20 mA.

Figure 5 shows the integrated photoluminescence (PL) intensity of InGaN/GaN MQW emission peak with and without a SiO_2 PQC pattern on an n-GaN layer versus inverse temperature. The temperature dependent PL was used to determine the internal quantum efficiency (IQE) of the InGaN/GaN MQW structures. At low temperatures the non-radiative recombination is close to minimum and radiative recombination processes are dominant. With increasing temperature, non-radiative recombination processes get activated and play a key role at room temperature.[23] The IQE of LED samples with and without a SiO_2 PQC pattern on an n-GaN layer calculated from IQE = $PL_{300\ K}/PL_{90\ K}$; where $PL_{300\ K}$ is the PL intensity at room temperature and $PL_{90\ K}$ is the PL intensity at the lowest temperature in our system. Assuming that the internal quantum efficiency equals unity at 90 K, we obtained the internal quantum efficiency of LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm) were 35%, 40%, and 41% higher as compared with that of the conventional LED 34% at room temperature. Therefore, the LED III ($d = 1.2$ μm) has higher epitaxial crystal quality due to the improved IQE performance on LED structure.

During life test, 20 ea chips of LED III ($d = 1.2$ μm) was encapsulated and driven by 50 mA injection current

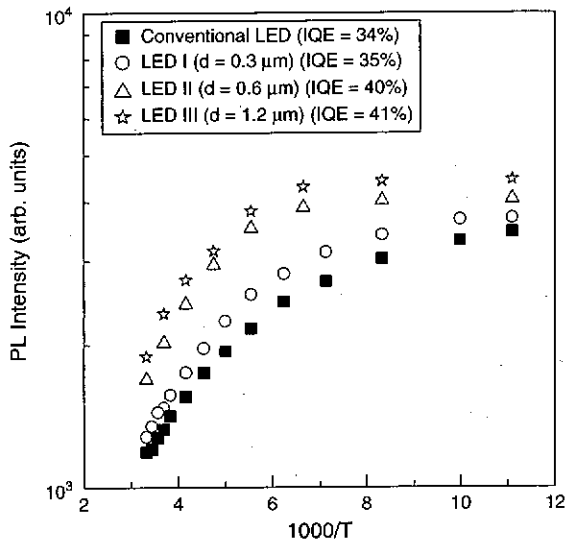

Fig. 5. Arrhenius plots of integrated PL intensities for GaN-based LED with/without a SiO_2 PQC structure on an n-GaN layer.

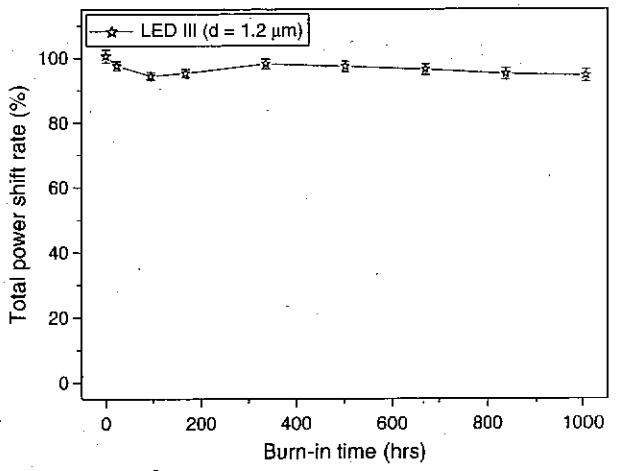

Fig. 6. The life test results of the LED with a SiO_2 PQC structure on an n-GaN layer under the condition of 50 mA/55 °C.

at 55 °C of ambient temperature. As shown in Figure 6, after 1000 h it was found that normalized output power of LED with a SiO_2 PQC structure on an n-GaN layer only decreased by 5%; indicates that the a SiO_2 PQC structure on an n-GaN is a reliable and promising method for device production.

4. CONCLUSION

In conclusion, GaN-based LEDs with a SiO_2 PQC pattern on an n-GaN layer by NIL are fabricated and investigated. At a driving current of 20 mA on TO-can package, the light output power of LED I ($d = 0.3$ μm), LED II ($d = 0.6$ μm), and LED III ($d = 1.2$ μm) were enhanced by a factor of 1.12, 1.16, and 1.20. The wall-plug efficiency of the InGaN/GaN LED were increased by 10~21% by a SiO_2 PQC pattern on an n-GaN layer. After 1000 h life test (55 °C/50 mA) condition, Normalized output power of LED with a SiO_2 PQC pattern on an n-GaN layer only decreased by 5%.

References and Notes

1. T. Mukai, M. Yamada, and S. Nakamura, *Jpn. J. Appl. Phys. I* 38, 3976 (**1999**).
2. M. Koike, N. Shibata, H. Kato, and Y. Takahashi, *IEEE J. Select. Topics Quantum Electron.* 8, 271 (**2002**).
3. E. F. Schubert, Light-Emitting Diodes, Cambridge University Press, Cambridge, UK (**2003**).
4. D. S. Wuu, W. K. Wang, K. S. Wen, S. C. Huang, S. H. Lin, R. H. Horng, Y. S. Yu, and M. H. Pan, *J. Electrochem. Soc.* 153, G765 (**2006**).
5. K. Iida, T. Kawashima, M. Iwaya, S. Kamiyama, H. Amano, I. Akasaki, and A. Bandoh, *J. Cryst. Growth* 298, 265 (**2007**).
6. K. Hoshino, T. Murata, M. Araki, and K. Tadatomo, *Physica Status Solidi (c)* 5, 3060 (**2008**).
7. D. S. Wuu, W. K. Wang, K. S. Wen, S. C. Huang, S. H. Lin, R. H. Horng, Y. S. Yu, and M. H. Pan, *J. Electrochem. Soc.* 153, G765 (**2006**).

8. Y. J. Lee, J. M. Hwang, T. C. Hsu, M. H. Hsieh, M. J. Jou, B. J. Lee, T. C. Lu, H. C. Kuo, and S. C. Wang, *IEEE Photon. Technol. Lett.* 18, 1152 **(2006)**.
9. D. H. Kang, J. C. Song, B. Y. Shim, E. A. Ko, D. W. Kim, S. Kannappan, and C. R. Lee, *Jpn. J. Appl. Phys.* 46, 2563 **(2007)**.
10. T. S. Oh, S. H. Kim, T. K. Kim, Y. S. Lee, H. Jeong, G. M. Yang, and E. K. Suh, *Jpn. J. Appl. Phys.* 47, 5333 **(2008)**.
11. Y. K. Su, J. J. Chen, C. L. Lin, S. M. Chen, W. L. Li, and C. C. Kao, *Jpn. J. Appl. Phys.* 47, 6706 **(2008)**.
12. H. Gao, F. Yan, Y. Zhang, J. Li, Y. Zeng, and G. Wang, *J. Appl. Phys.* 103, 014314 **(2008)**.
13. J. J. Wierer, M. R. Krames, J. E. Epler, N. F. Gardner, M. G. Craford, J. R. Wendt, J. A. Simmons, and M. M. Sigalas, *Appl. Phys. Lett.* 84, 3885 **(2004)**.
14. A. David, T. Fujii, R. Sharma, K. McGroddy, S. Nakamura, S. P. DenBaars, E. L. Hu, and C. Weisbuch, *Appl. Phys. Lett.* 88, 061124 **(2006)**.
15. S. H. Kim, K. D. Lee, J. Y. Kim, M. K. Kwon, and S. J. Park, *Nanotechnology* 18, 055306 **(2007)**.
16. K. J. Byeon, S. Y. Hwang, and H. Lee, *Appl. Phys. Lett.* 91, 091106 **(2007)**.
17. C. H. Lin, H. H. Yen, C. F. Lai, H. W. Huang, C. H. Chao, H. C. Kuo, T. C. Lu, S. C. Wang, and K. M. Leung, *IEEE Photon. Technol. Lett.* 20, 836 **(2008)**.
18. D. H. Kim, C. O. Cho, Y. G. Roh, H. Jeon, Y. S. Park, J. Cho, J. S. Im, C. Sone, Y. Park, W. J. Choi, and Q. H. Park, *Appl. Phys. Lett.* 87, 203508 **(2005)**.
19. H. W. Huang, C. H. Lin, K. Y. Lee, C. C. Yu, J. K. Huang, B. D. Lee, H. C. Kuo, K. M. Leung, and S. C. Wang, *Semicond. Sci. Technol.* 24, 085008 **(2009)**.
20. Z. S. Zhang, B. Zhang, J. Xu, K. Xu, Z. J. Yang, Z. X. Qin, T. J. Yu, and D. P. Yu, *Appl. Phys. Lett.* 88, 171103 **(2006)**.
21. C. H. Chiu, H. H. Yen, C. L. Chao, Z. Y. Li, P. Yu, H. C. Kuo, T. C. Lu, S. C. Wang, K. M. Lau, and S. J. Cheng, *Appl. Phys. Lett.* 93, 081108 **(2008)**.
22. H. Matsubara, S. Yoshimoto, H. Saito, Y. Jianglin, Y. Tanaka, and S. Noda, *Science* 319, 445 **(2008)**.
23. D. Fuhrmann, U. Rossow, C. Netzel, H. Bremers, G. Ade, P. Hinze, and A. Hangleiter, *Phys. Stat. Sol. (c)* 3, 1966 **(2006)**.

Received: 14 August 2009. Accepted: 26 November 2009.