

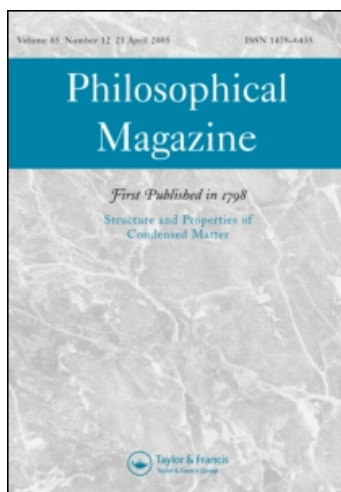
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Nanostructured silicon and its application to solar cells, position sensors and thin film transistors

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Nanostructured silicon and its application to solar cells, position sensors and thin film transistors

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This paper reports the performance of small area solar cells, 128 linear integrated position sensitive detector arrays and thin film transistors based on nanostructured silicon thin films produced by plasma-enhanced chemical vapour deposition technique, close to the onset of dusty plasma conditions, within the transition region from amorphous to microcrystalline. The small area solar cells, produced in a modified single chamber reactor, exhibited very good electrical characteristics with a conversion efficiency exceeding 9%. The 128 integrated position sensitive detector arrays, based on a similar pin structure, allow real-time 3D object imaging with a resolution higher than 901 p/mm. The thin film transistors produced exhibited field effect mobility of 2.47 cm²/V/s, threshold voltage of 2 V, on/off ratio larger than 10⁷ and sub-threshold slopes of 0.32 V/decade, which are amongst the best results reported for this type of device.

Keywords: nanostructured silicon; thin film devices; position sensitive detectors; TFTs; solar cells

1. Introduction

Amorphous silicon (a-Si:H) has been studied for many years [1–3], with a particular emphasis on optoelectronic devices, since the doping effect was demonstrated by Spear [4]. This material has been intensively studied and the work of Spear [5,6] and LeComber [7–9], among others, have been fundamental references. To these studies, we have to add the earlier work of Madan et al. [10] in determining the density of localized states that not only supported the development of high-grade electronic quality, undoped amorphous silicon for device applications, but was also the precursor in the use of amorphous silicon in field effect transistors [11]. Since then, the main bottleneck has been inherent light degradation of a-Si:H [12] and low carrier mobility, which prevents even larger application potential of the material.

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To overcome the carrier mobility limitation, several authors have proposed the production of new silicon alloys [13] or structured ordered thin silicon, such as microcrystalline [14–16], polymorphous [17] or protocrystalline [18] silicon. As far as devices are concerned, the main driving force has been its use in solar cells [19], field effect transistors/thin film transistors [20] and sensors [21–25]. Other possible applications have also been tried, such as switching memories [26], tunnelling-based devices [27], large area position sensitive detectors (psd) [28,29] or in biosensors [30,31].

It appears that degradation is due to the metastability in a-Si:H and closely related to the amorphous network nature and vast number of hydrogen atoms within the film. Therefore, to improve stability and electronic performance, the microstructure must be improved. To attain this goal, we produced hydrogenated diphasic nanostructured silicon thin films close to the onset of dusty plasma conditions, within the amorphous to microcrystalline transition region, using high hydrogen dilution conditions [32–36].

In honour of Professor Walter Spear and his major contribution to the field of amorphous silicon, related alloys and their integration into devices, we present the results of the process conditions used to produce nanostructured hydrogenated silicon (ns-Si:H) and its application in solar cells, psd integrated arrays [37,38] and TFTs. The psd 128 integrated array is presented for the first time and fully integrated into a linear camera that allows for real-time 3D inspection imaging. Concerning TFTs, the aim is to show that a high performance device can be produced with the material developed, as well as to prove that other materials, other than silicon dioxide or silicon nitride, [39] can be successfully used as the dielectrics.

2. Experimental details

2.1. Material deposition

The nanostructured thin films were deposited by plasma-enhanced chemical vapour deposition (PECVD) at 27.12 MHz using a single chamber, as described elsewhere [34,40]. The main features of these types of films, when compared to amorphous silicon, are the improvement in short-range order and a particular signature given by the hydrogen exodiffusion data (there is a characteristic peak, absent in the amorphous silicon, shifted to high temperatures, when compared to the microcrystalline silicon). Also noticeable is the absence of the usual high hydrogen content measured by infrared spectroscopy, which is considered one of the polymorphous fingerprints [14], and the absence of a distinct phase with a low hydrogen concentration occurring during the crystal growth, which evolves into a microcrystalline form (the so-called protocrystalline [15]) [41].

The deposition pressure (p) and the substrate temperature (T_s) were fixed at 187 Pa and 473 K, respectively. The influence of silane concentration [$d_r = \text{SiH}_4/(\text{SiH}_4 + \text{H}_2)$] and the role of power density (P_d) on film properties were studied on the range 1–9% and 63–383 mW/cm², respectively. The d_r was varied by increasing the silane flow in the mixture, from 1 to 9 sccm, keeping the hydrogen flow constant (100 sccm).

The films deposited were studied by micro-Raman spectroscopy and exodiffusion measurements. The exodiffusion data allow the determination of the exodiffusion hydrogen activation energy for the set of films produced, which was deduced from the relation between the heating rate (ϕ) and the peak temperature (T_m), given by Equation (1) [42]:

$$\frac{E_a \phi}{RT^2} = A e^{(-E_a/RT)}, \quad (1)$$

where A is the reaction constant, R is the gas constant (8.31 J/mol.K), T is the absolute temperature and E_a is the activation energy for the evolution process.

Taking logarithms on both sides of Equation (1) and differentiating it with respect to $1/T_m$ yields [43]

$$\frac{\ln(\phi/T_m^2)}{(1/T_m)} = \frac{E_a}{R}. \quad (2)$$

From the slope of a $\ln(\phi/T_m^2)$ versus $(1/T_m)$ plot, the E_a was calculated using the Kissinger method [44], which has been used to determine the activation energy of solid-state reactions through the method of differential thermal analysis. In this method, the dominant factor controlling the shape and position of the differential thermal analysis peak is the nature of the reaction itself. The heating rate was varied between 3 and 10 K/min.

2.2. Solar cells deposition

The solar cell with a p-doped layer/buffer1/buffer2/i-ns-Si:H layer/n-doped/Ag/Al structure was deposited on gallium zinc oxide (GZO)-coated glass substrate, as described elsewhere [45], using the material deposition conditions defined in Section 2.1. The two buffer layers are used to adjust the mismatch in the optical band gap between the p- (1.94 eV) and i- (1.82 eV) layers. The band gap of buffer1 is 1.88 eV and that of buffer2 is 1.84 eV. Additionally, the buffer layers are efficient in controlling the diffusion between the dopants of the p- and i- layers [46–48]. The back contact consists of a thin Ag layer (≈ 30 nm) used to improve the light reflectance, followed by an Al layer (≈ 170 nm) with an electrode area of 0.07 cm^2 [49]. Table 1 summarizes the characteristics of the different layers as well as the gas mixtures used. The silicon structure was removed by a dry-etching technique to avoid interference of the current collected in the vicinity surrounding the contact [50]. The study of these devices also served to establish the optimized process conditions for producing the integrated psd arrays. The solar cell performance was measured using a sun simulator under AM1.5 illumination conditions.

2.3. Linear integrated psd arrays fabrication and characterization

The linear integrated array and consisted of 128 psds, configured as a nip structure, processed using similar conditions to those described for solar cells, with the exception that the intrinsic layer has a thickness above $0.8 \mu\text{m}$. Details concerning the fabrication steps of the psd arrays are given previously [51]. The device linearity

Table 1. Summary of the characteristics of the different layers and gas mixtures used.

Layers	Thickness	Conductivity ($\Omega\text{ cm}$)	Optical gap (eV)
p-doped	$\approx 7.8 \pm 2\text{ nm}$	3.2×10^{-6}	1.94 ± 0.01
Buffer ₁	$\approx 0.5\text{ nm}$	—	1.88 ± 0.01
Buffer ₂	$\approx 0.8\text{ nm}$	—	1.84 ± 0.01
Intrinsic	$\approx 270 \pm 10\text{ nm}$	6.12×10^{-10}	1.82 ± 0.01
n-doped	$\approx 25 \pm 5\text{ nm}$	2.46×10^{-3}	1.80
Back contact	$\approx 30\text{ nm}$ of Ag + $\approx 170\text{ nm}$ of Al	—	—
Gas mixture used:			
p-layer = 1% $(\text{CH}_4)_3\text{B}_2$ + 40% CH_4 + 39% SiH_4 + 20% H_2 ;		i-layer = 5% SiH_4 + 95% H_2	
Buffer ₁ = 7% SiH_4 + 8% CH_4 + 85% H_2		n-layer = 1% PH_3 + 30% SiH_4 + 28% H_2 + 41% He	
Buffer ₂ = 7% SiH_4 + 4% CH_4 + 89% H_2			

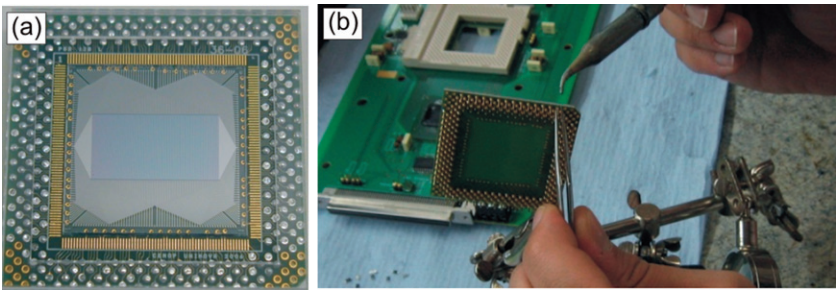


Figure 1. (a) Image of the 128 psd integrated array and (b) the pcb where it will be mounted.

versus incident light frequency measurements were taken in the photoconductive mode [37,51,52], where the back metal contact was grounded or reverse-biased at -1 V and the photocurrents detected at the pad electrodes located on the device edges (see Figure 1). The devices are mounted over a collecting printed circuit board (PCB) unit that contains the controller unit, the analogical/digital (A/D) converter and the MX4 microprocessors, schematically depicted in Figure 2. The functional characteristics of this 128 psd integrated array are depicted in Table 2. The PCB board is connected to the PC via an acquisition data board from National Instruments (NI 6031E). The detection system used to obtain a 3D image directly from the integrated psd array is depicted in Figure 2, and the camera performance is shown in Table 3. The light source is a diode laser (670 nm, 5 mW), which generates a line focused by a lens towards the surface to be inspected. The linear movement of the device was achieved using an automated control table (Parker-Hannifin M106061S 5M) with a spatial resolution better than $5\text{ }\mu\text{m/turn}$. All the experimental data were gathered using custom-developed software for data acquisition and control.

The main properties of the layers that constitute the devices such as thickness, conductivity and optical gap are the same used to process the solar cells described in Section 2.2 and referred to in Table 1.

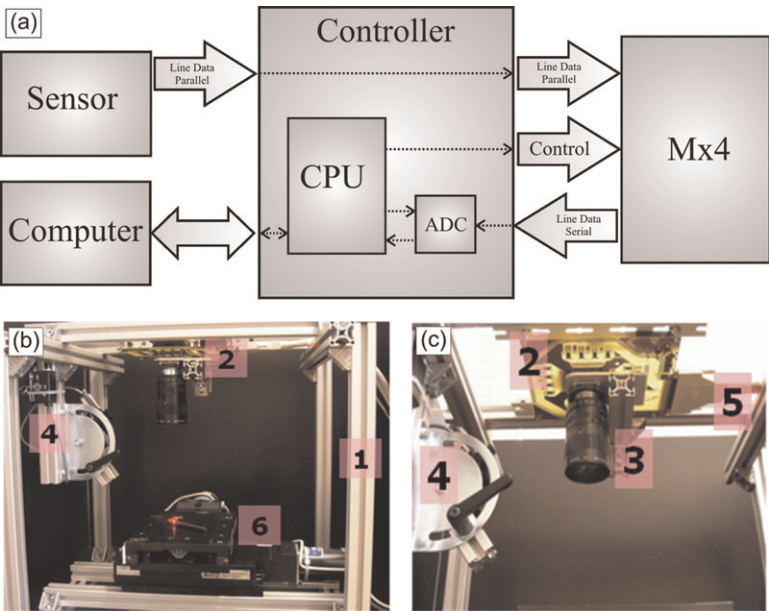


Figure 2. (a) Schematic of the electrical interconnections between the sensor, the controller unit, the MX4 and computer where the acquisition data board is located. (b) Global vision of the line inspection camera demonstrator used. (c) Detailed information on the optical system. The numbers refer to: (1) chassis; (2) pcb board containing the sensor; (3) lens (35–70 mm, f:1.4); (4) laser line generator (635 nm) + angular adjustment; (5) connecting cable from the pcb board to the PC; (6) x–y controlled table.

Table 2. Functional characteristics of the 128 psd integrated array.

Array type	Dimension [mm]	Active area [mm]	Non-linearity [%]	Line resolution [μm]	Working light wavenumber range [nm]	Frequency response [kHz]	NEP [W/Hz ^{1/2}]
128	Chip carrier 47 × 47 Sensor 30 × 30	20 × 12	<2%	<0.75	500–680	> 500	10 ^{−11}

2.4. Thin film transistor fabrication and characterization

For thin film transistors processing, the substrate is located in the dark region of the plasma, underneath a grounded metal grid. By not exposing the growth surface directly to the plasma, we avoided high ion bombardment at the silicon growth surface, leading to a less defective surface and highly compact films.

The TFTs were produced using different dielectric layers in a bottom gate configuration, as shown in Figure 3. The materials used as dielectric were a multilayer of aluminium oxide and titanium oxide, known as ATO,

Table 3. Camera performance.

Open space distance (h)	40–6 cm
Working range	10–0.5 cm
Sensor deep resolution (z)	2.5–0.75 μm
Sensor horizontal resolution (x)	50–10 μm
Scanning speed (v_y)	< 50 cm/s
Frequency response	> 500 kHz
Linearity	> 99.9%
Lens aperture	2.8

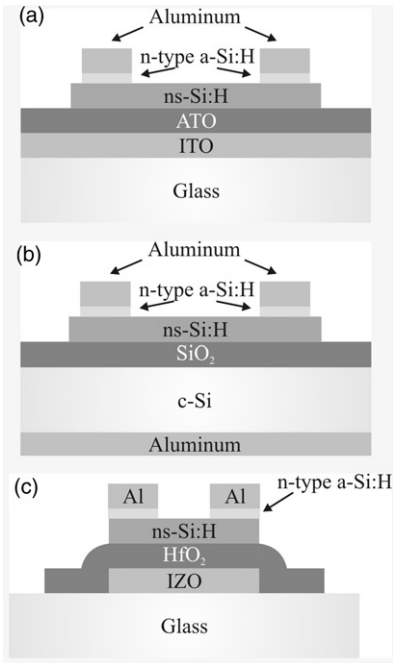


Figure 3. Schematic structure of bottom gate ns-Si:H TFTs integrating as dielectric. (a) Aluminum oxide/titanium oxide multilayer (ATO) deposited by ALD. (b) Thermal silicon oxide (SiO₂). (c) Sputtered hafnium oxide (HfO₂).

silicon oxide (SiO₂) and hafnium oxide (HfO₂) [53]. In the first case, the dielectric was deposited by atomic layer deposition (ALD) over indium tin oxide (ITO) that acts as a gate electrode. The substrate (glass)/ITO/ATO stack was supplied by Plannar Systems Inc. The SiO₂ was obtained by thermal oxidation of highly doped p-type silicon that was metalized on the back surface to form the gate electrode. The HfO₂ was deposited by r.f. sputtering over the gate electrode (sputtered indium zinc oxide, IZO). Both layers (dielectric and gate electrode) were patterned by lift-off lithography.

The deposition of the 120-nm thick ns-Si:H channel layer was done by PECVD at 200 °C with a power density of 128 mW/cm² at 27.12 MHz, following similar

procedures as those described in Section 2.1, to obtain nanostructured silicon films (ns-Si:H). The deposition pressure selected was 186 Pa and the total gas flow 105 sccm with $d_r \cong 5\%$. The source and drain n-type a-Si:H was deposited right after ns-Si:H, without breaking vacuum, also at 200°C. In this case, the power density was 35 mW/cm², using the same 27.12 MHz generator, while the pressure and gas flow (PH₃/SiH₄/H₂/He mixture) were 86 Pa (0.65 Torr) and 10 sccm, respectively. The growth rate changes from 10–12 to 6–8 nm/min for films grown with or without the grid, respectively. An Al layer of 200 nm in thickness was evaporated on top of the n-type silicon. The source and drain electrodes were then patterned by photolithography and wet etching using a H₂PO₄:HNO₃:H₂O solution. This metal layer serves as a mask for the n-type silicon etching by reactive ion etching (RIE). The etching time was accurately monitored to allow for the removal of just the doped layer deposited over the channel layer. The devices were terminated by also patterning the channel layer with photolithography and RIE. To enhance device performance, annealing at 200 °C in a forming gas (95% N₂–5% H₂) atmosphere was performed. The electrical characterization of the TFT was performed using an Agilent 4155C semiconductor analyzer connected to a Microprober Cascade M150, installed inside a dark box.

3. Results

3.1. Processed materials

Figure 4 shows typical micro-Raman results of the nanostructured films produced (dotted line) and reference data spectra of amorphous (dashed line) and microcrystalline (solid line) silicon thin films. The peak shift observed (from ~ 480 to ~ 485 cm⁻¹) is also seen in polymorphous films and is attributed to the improvement in the structural order at the nanoscale level [32,54].

The hydrogen exodiffusion spectra as a function of temperature are shown in Figure 5. Figure 6 summarizes all the plasma conditions that lead to the production

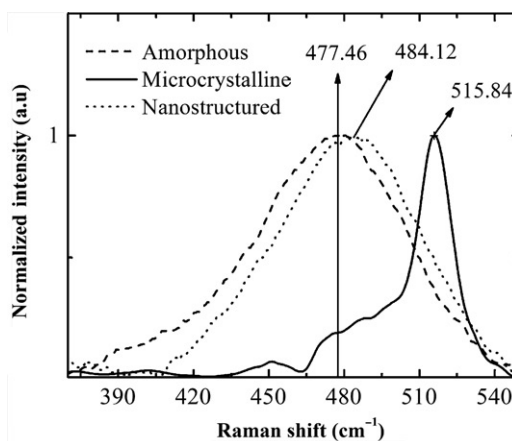


Figure 4. Micro-Raman spectra for the different sets of silicon thin films produced.

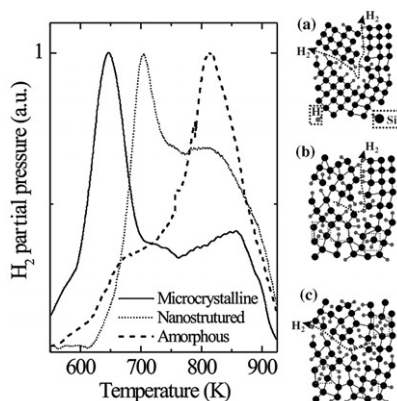


Figure 5. Hydrogen evolution spectra for the set of silicon thin films processed. The illustrations shown aim to represent the atomic rearrangements within the different type of structures studied: (a) microcrystalline films; (b) nanostructured films; (c) amorphous films.

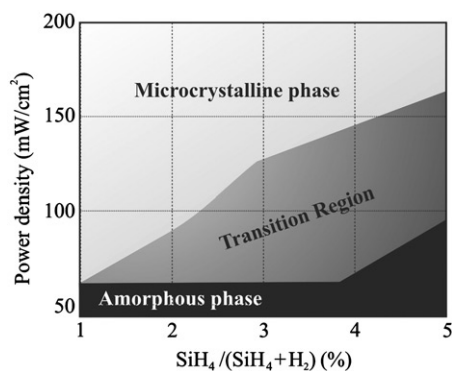


Figure 6. Power density as a function of the hydrogen dilution ratio used showing the different conditions leading to the production of materials where the amorphous or microcrystalline phases dominated. In between, we can see the transition region.

of materials with different types of structures (from amorphous to microcrystalline) as a function of P_d and d_r used. The different process conditions, which lead to the production of silicon thin films where the amorphous or microcrystalline phases clearly dominate, can be clearly seen. Inbetween we can see the transition region, where both phases may exist: close to the microcrystalline phase the predominant structure is dominated by the existence of nanocrystals, while close to the amorphous region we may still have a dominant amorphous phase but with a highly improved short-range order.

Figure 7 shows the change in the low temperature (LT) and high temperature (HT) peak positions as a function of P_d for films produced at high deposition rate, using $d_r=5\%$. The films deposited at the lowest P_d are amorphous, while the LT exodiffusion peak is related to the weak hydrogen silicon bonds. Thus, for

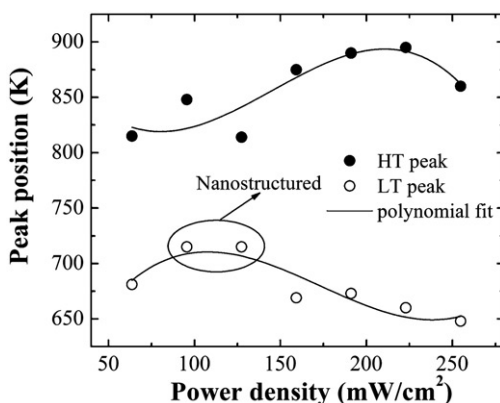


Figure 7. Evolution of LT and HT hydrogen exodiffusion peak positions as a function of power density, for $d_r = 5\%$.

$94 \text{ mW/cm}^2 < P_d < 128 \text{ mW/cm}^2$, the films are produced in the so-called transition region and the LT peak increases compared to amorphous films. For films with $P_d > 160 \text{ mW/cm}^2$, the crystalline fraction of the films increases and the hydrogen situated around the grains can diffuse easier through the network and the LT peak shifts towards 643 K.

3.2. Device results

3.2.1. Solar cells

Figure 8a shows the cross-section of the solar cell. The image reveals a highly compact structure, where we note the typical dense columnar structure of the polycrystalline GZO, exhibiting a bulk resistivity of $2.5 \times 10^{-4} \Omega \text{ cm}$, a mobility close to $20 \text{ cm}^2/\text{V/s}$ and a transmittance in the visible range above 82% for a film thickness of about $1.35 \mu\text{m}$ [55–57]. In addition, the GZO films clearly sustain the plasma process, as observed when analyzing different types of TCOs after sustaining an intense hydrogen plasma by 600 s [58], and do not suffer any chemical or physical degradation. Near the glass/GZO interface, small grains are observed. On the other hand, a highly compact structure near the surface makes it impossible to distinguish between grain boundaries, defects or voids.

The image also reveals a well compacted and dense pin structure, where no large crystallites or grains can be seen. In other words, we are in the presence of an almost amorphous film where the short-range order has been improved, in spite of the hydrogen content of these films [35].

Figure 8b and c show the J – V characteristics and quantum efficiency curves for the produced small area solar cells.

3.2.2. Integrated psd arrays

In Table 3, we present the characteristics of the 128 integrated arrays produced. Figure 9 shows the results of the spatial resolution determined in 1D

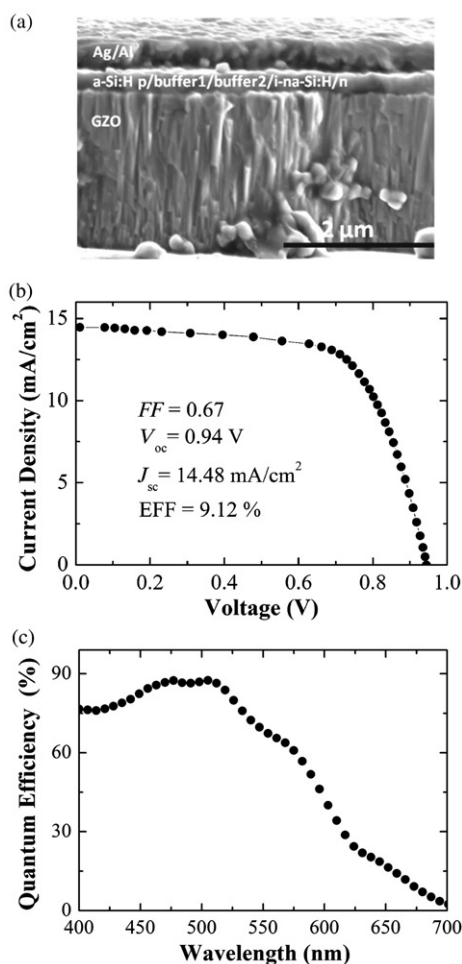


Figure 8. (a) Cross-section of the solar cell structure. (b) J - V characteristic of the solar cell. (c) Quantum efficiency curve for the produced solar cell.

psd element of the array, using spatial steps down to a minimum of $0.25 \mu\text{m}$ allowed by the measuring system and a focus light of $50 \text{ mW}/\text{cm}^2$. As observed, both measurements are linear but the proximity of the points in the $0.25 \mu\text{m}$ measurement causes the current to oscillate in such a way that one current value can correspond to two or three positions, which leads to inaccuracy in its position. In other words, the random distribution of currents measured to determine a clear position is inadmissible. Despite this, linear behavior can still be seen. This means that the minimum resolution of the sensor is higher than $0.25 \mu\text{m}$. With the $1 \mu\text{m}$ step measurements, the case of a current value corresponding to two or more positions does not occur, so it is possible to determine a position with an accuracy of $\pm 0.5 \mu\text{m}$.

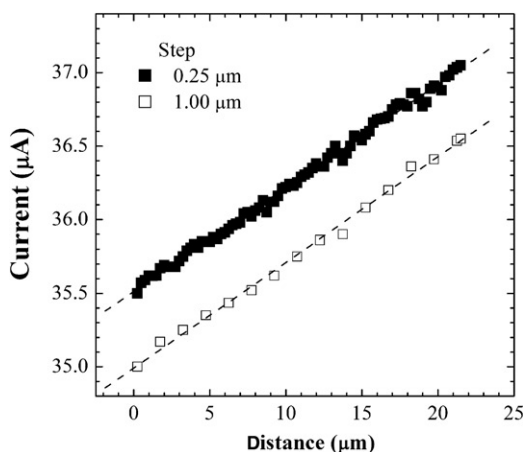


Figure 9. Spatial resolution measurements performed on a sensor at 0.25 and 1.00 μm steps.

3.2.3. Thin film transistor

Figure 10a shows the variation in transfer characteristics and transconductance (g_m) with gate voltage (V_{GS}) for the set of TFTs analyzed using different dielectrics. The typical electrical parameters extracted from the transfer characteristics, such as the field effect mobility (μ_{FE}), threshold voltage (V_T), on/off ratio (I_{on}/I_{off}) and sub-threshold slope (S) are shown in Table 4. In Figure 10b, the transfer characteristics of the TFT, produced using different channel dimensions, on linear ($V_{DS} = 1\text{ V}$) and saturation regimes ($V_{DS} = 10\text{ V}$) for ns-Si:H TFT with different channel dimensions integrating SiO_2 as dielectric, are shown. In Figure 10c, the transfer characteristics of a TFT, produced using the protection grid with optimized hole dimensions (1.5 times greater in diameter), is presented. The electrical parameters extracted from these data are shown in Table 5.

4. Discussion

4.1. Materials properties

The spectra in Figure 4 show the three main types of materials produced: (1) amorphous films, represented by a single Gaussian peak centered around 480 cm^{-1} [59]; (2) microcrystalline films, with a band close to the sharp peak around 516 cm^{-1} ; (3) nanostructured films, represented by an improved short-range order, where some nanocrystals exist ($<2\%$). This is conjectured by a slight shift in the amorphous peak towards higher wavenumbers combined with a slight narrowing of the full width at half maximum (FWHM). This shift towards higher wavenumbers can be attributed to the presence of nanocrystals randomly distributed in the film or to improvement in the short-range order. The presence of such nanocrystals (of small size, $<10\text{ nm}$) and of short-range order clusters can lead to an internal film stress, which is responsible for the observed shift [59].

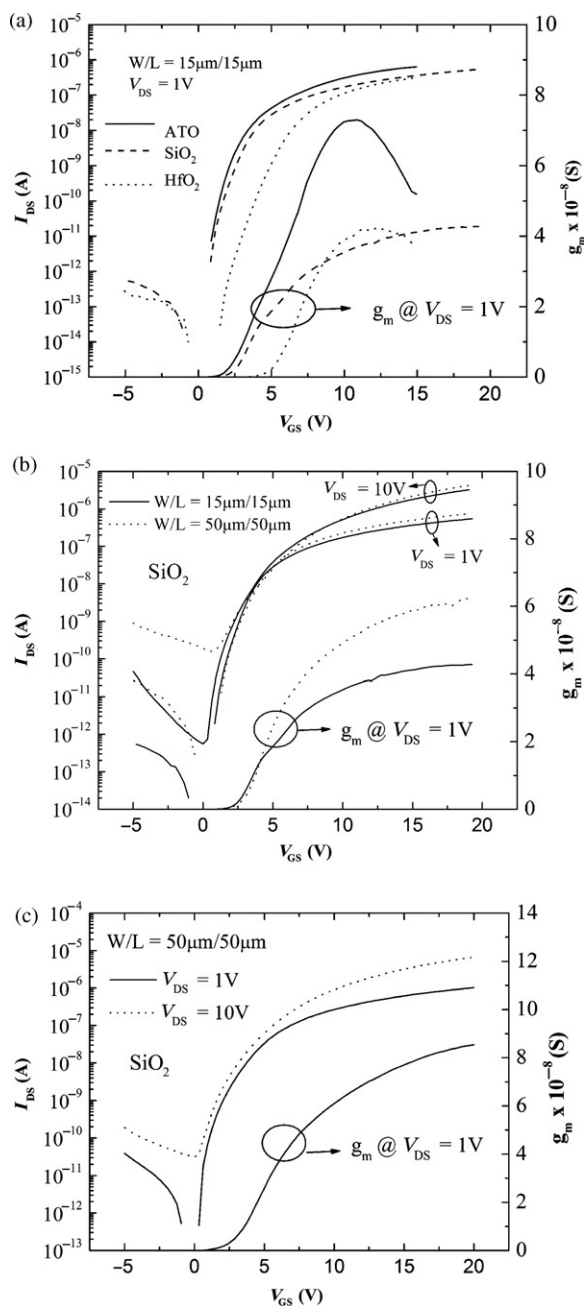


Figure 10. (a) Transfer characteristics on the linear regime for a ns-Si:H TFT produced with the protection grid integrating different dielectrics; the corresponding transconductance is also plotted. (b) Transfer characteristics on the linear ($V_{DS}=1\text{V}$) and saturation regimes ($V_{DS}=10\text{V}$) for a ns-Si:H TFT with different channel dimensions integrating SiO_2 as dielectric. The plot of the transconductance for both channel lengths analyzed is also shown.

Table 4. Typical electrical parameters extracted from the transfer characteristics.

Dielectric	μ_{FE} (cm ² /V/s)	V_{T} (V)	S (V/dec)	$I_{\text{on}}/I_{\text{off}}$
ATO	1.14	2.04	0.52	$> 10^6$
SiO ₂	1.24	2.35	0.45	$> 10^7$
HfO ₂	0.85	5.19	0.63	$> 10^7$

Table 5. Electrical parameters extracted from the data.

W/L (μm)	μ_{FE} (cm ² /V/s)	V_{T} (V)	S (V/dec)	$I_{\text{on}}/I_{\text{off}}$
15/15	1.24	2.35	0.45	$> 10^7$
50/50	1.84	2.82	0.56	$> 10^6$
50/50 OG*	2.47	2.78	0.32	$> 10^7$

*Device produced using a grid with a larger aperture than the others.

The exodiffusion data are shown in Figure 5 and, together with the illustrations, help to understand the characteristics of the structure of the developed materials. The films with different structures have different ways of releasing the bonded hydrogen, as a function of sample temperature. The first highest peak (at low temperature, LT) corresponds to hydrogen exodiffusion from microcrystalline silicon, due to loosely bonded hydrogen at the grain boundaries, while the HT peak of the same spectrum corresponds to hydrogen tightly bonded to silicon in the remaining amorphous phase.

With respect to the amorphous silicon film, in the exodiffusion spectrum (dash line), the LT peak represents the weak SiH₂/SiH₃ bonds and the clusters adsorbed by physisorption originating from van der Waal's interactions. Figure 5b shows a nanostructured film that shares some similarity with the microcrystalline structure since it also has the presence of some grain boundaries, but with a large fraction of amorphous tissue. This explanation is in agreement with the collected exodiffusion spectrum where a third spectrum corresponding to films produced in the so-called transition region, where the present films have been deposited, is shown. In this spectrum, the LT peak is shifted towards 703 K (about 60 K above the previous LT peak). Its position peak can be explained by the presence of a mixed phase material (disorder/short range order or disorder/nanoorder), where tightly bonded hydrogen is prevalent in the amorphous tissue with a combination of hydrogen in possible cavities or in the boundaries of nanograins. These data, together with the role of hydrogen dilution and P_{d} used, leads to the schematic shown in Figure 6, where a small “window” corresponding to films deposited on the transition region is defined. The transition region where nanostructured films can be processed depends on the reactor configuration and temperature uniformity on the deposition chamber [32,60,61].

Indeed, the interaction between atomic hydrogen and the surface during the deposition process markedly influences the type of structured film obtained [62].

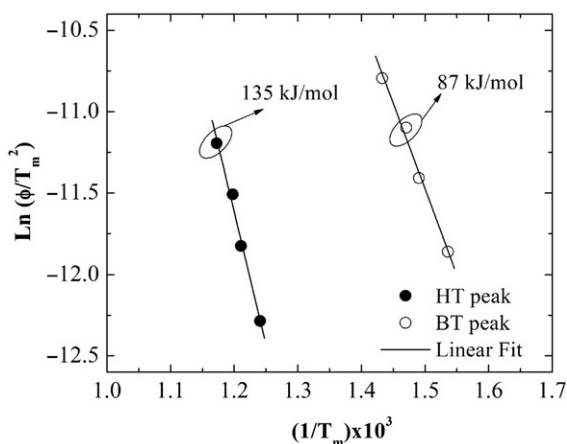


Figure 11. Activation energy for nanostructured films processed in the transition region. Data from Figure 8 were fitted by Equation (2).

As observed in Figure 7, the hydrogen evolution in films produced in the transition region reveals that they have a compositional structure that differs from that of conventional amorphous silicon. To compare film properties, the exodiffusion hydrogen activation energy was calculated using the Kissinger method [44]. The values recorded for the nanostructured films at LT and HT peaks are shown in Figure 11, and the data fitted by Equation (2). The E_a data reported in the literature for amorphous silicon for the LT and HT peaks are 79 and 112 kJ/mol, respectively [42]. On the other hand, the E_a data obtained for the nanostructured films for the LT and HT peaks are, respectively, 87 and 135 kJ/mol. The increase in E_a regarding the HT peak is related to hydrogen being more tightly bonded in the amorphous phase, while the higher values for the LT peak can be attributed to the formation of hydrogen bonds in nanocavities or in the boundaries of nanograins. This material, fabricated in the transition region, was used to fabricate devices such as solar cells, position sensitive detectors and thin film transistors, whose electronic performances are discussed below.

4.2. Solar cells

Analysis of the plots shown in Figure 8 for single junction solar cells based on ns-Si:H films leads to a fill factor (FF) of 0.67, an open circuit voltage (V_{oc}) of 0.94 V and a short circuit current density (J_{sc}) of 14.48 mA/cm², leading to a conversion efficiency (EFF) of 9.12%.

The high current density and good value obtained for the quantum efficiency are mainly attributed to the quality of the i-layer and to the p/i interface, which does not annihilate the photocarriers generated, and to the contribution of GZO as the front contact since it is not degraded by the hydrogen plasma during the deposition of the p-layer [45–47]. This is probably due to the stability of the GZO, leading to improved transmittance at the blue region of the spectrum. The high value of open circuit voltage is related to the wide band gap and high work function of GZO (respectively,

above 3.4 eV and 4.95 V), which leads to an enhancement of the band offsets between the p-type silicon front layer and the transparent conductive oxide layer used [63]. This analysis is supported by data achieved on similar solar cells where the only change in fabrication was the use of the conventional amorphous i-layer, keeping all other constituent layers the same. The data achieved under these conditions lead to short circuit current, fill factor and open circuit voltage of 13 mA/cm², 0.62 and 0.92 V, respectively, leading to an overall device efficiency of 7.4%. After continuous AM1.5 illumination for 250 h, we notice that the overall efficiency of the solar cells stabilizes to a value ~8.50%, showing that these devices are more stable than a-Si:H-based solar cells, where significant device degradation, sometimes exceeding 20%, has been reported [46]. These data cannot be compared with industry data where the devices are differently processed, as are the recent reported data from MVSsystems and United Solar, for instance [64–69]. The aim is to prove the consistency of laboratory results [63] and the integration of these nanostructured silicon thin films into device structure, such as solar cells, thin film position sensitive detectors and thin film transistors.

4.3. Integrated psd arrays

4.3.1. Working principles

The operation principle of the psd array is that an image line projected in the array induces photocurrents (I_{ph1} and I_{ph2}) or lateral photo voltages ($\Delta V = V_1 - V_2$) in the illuminated elements (see Figure 12). Then all elements are scanned to determine the position of the image line. In this case, the angle of incidence that the laser line makes with the surface to be inspected should allow its detection along the length of the detector. In other words, the maximum active length d_d of each element of the array has to be such that

$$d_0(\max) \geq \frac{d_d(\max)}{\cos \phi}, \quad (3)$$

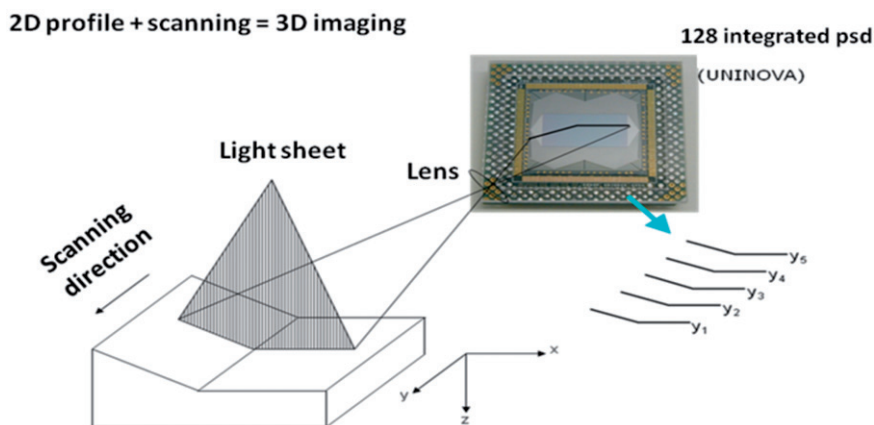


Figure 12. Schematic of the light line projected onto the integrated 128 psd arrays containing the information of the object to be displayed.

where d_0 is the distance between the sensor and the surface to be scanned [70,71]. Each element ΔI_{ph} has an uncertainty related to noise (n) and so, the measure position is given by

$$\begin{aligned} P(y_n) &= \frac{(I_{ph1} \pm n_1) - (I_{ph2} \pm n_2)}{(I_{ph1} \pm n_1) + (I_{ph2} \pm n_2)} \cdot \frac{L}{2} \Rightarrow P_{\max}(y_n) \\ &= \frac{I_{ph1} - I_{ph2}}{I_{ph1} + I_{ph2} - 2n} \cdot \frac{L}{2}, \quad \text{for } n_1 = n_2 = n, \end{aligned} \quad (4)$$

where n_1 and n_2 are the absolute noise detected at each element terminal and L is the length of each line. Thus, the position of an image line projected in the plane $z-y$ is determined by $P(y_n)$ obtained by the 128 stripes and related to the currents detected by the MX8 connected to the terminals of integrated arrays.

The detection threshold limit will depend on the signal-to-noise ratio (S/N), which is given by $S/N = (I_{ph1} + I_{ph2})/2n$. Thus, the positional resolution (dP) depends on the active length of each sensing element and on (S/N): $dP \approx (L/(2S/N))$.

Once the proper S/N ratio has been established, the performance of the 128 psd arrays is mainly dependent on the maximum distance at which a light spot from each of the collecting electrodes can be detected with a linear correlation between the spatial position and the lateral photocurrent measured [70].

As we aim to use these devices to supply planar information about 3-D objects (images), we should also define the modulation transfer function (MTF) as the appropriate image quality criteria in the frequency spatial domain (specifying resolution and perceived image sharpness) [72], i.e. the contrast at a given spatial frequency relative to low frequencies. In this case, the spatial frequency (ν) is typically measured in cycles or line pairs per millimeter (lp/mm). Therefore, high spatial frequencies correspond to fine image details.

In our case, MTF will correspond to how well the input signal is preserved after being imaged. To do so, we determine the fast Fourier transform of the signal and convert it into the frequency domain to define the pattern conditions that lead to proper spatial signal discrimination, i.e.

$$\text{MTF}(\nu) \approx \frac{I_{\max}(\nu) - I_{\min}(\nu)}{I_{\max}(\nu) + I_{\min}(\nu)}, \quad (5)$$

where I_{\max} and I_{\min} correspond to maximum and minimum currents discriminated between two consecutive spatial points. Thus, proper image plane resolution will correspond to the inverse of ν for which MTF has some meaning concerning image preservation and metric details. Finally, we have to consider the device non-linearity of each strip (position detection error) (δ):

$$\delta = \frac{2\sigma}{F}, \quad (6)$$

where σ is the rms (root mean square) deviation from the regression line data and F is the full scale measured.

4.3.2. Integrated 128 psd arrays performances

The process conditions selected for fabricating the integrated psd arrays were the same used to fabricate the solar cells. Thus, once the proper sensor geometry is

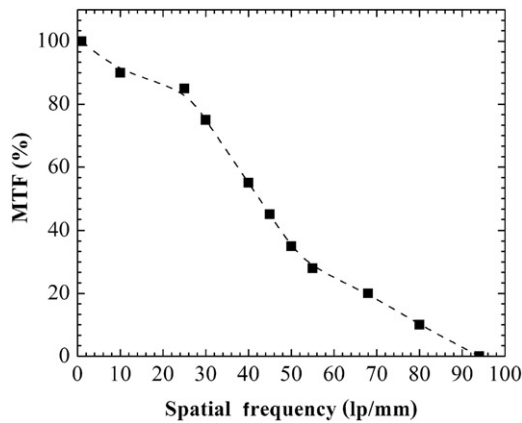


Figure 13. MTF (%) as a function of the spatial frequency.

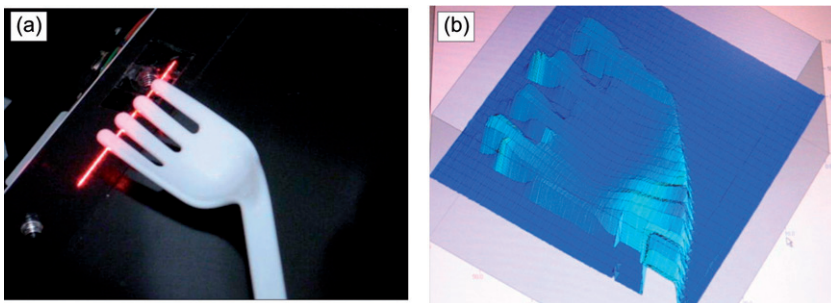


Figure 14. (a) Image to be 3D scanned, showing the laser line projected on it. (b) Image collected by the sensor, in real-time, without any type of data treatment.

established and before performing any measurement, the conditions for light illumination of the array were defined. Detailed information concerning the detection platform and the integrated array is given in Tables 2 and 3.

The minimum light power allowable P_i , which permits a good linear correlation with a spatial detection error below $\pm 4\%$, was approximately 50 nW/line for the integrated devices under analysis.

To determine the image plane resolution, the modulation transfer function (MTF) required to preserve proper image detail and information must be known. Following Equation (5), this means that $MTF = 0$ when $\nu = 2000$ lp/mm. Taking into account that the array has 128 elements, we reach the set of data depicted in Figure 13. For a good image plane resolution, $MTF \leq 10\%$, we obtain the maximum ν at about 90 lp/mm, from which we estimate that $I_{\max}/I_{\min} \geq 1.2$ to get a sharp image. Also taking into account the visible laser line used (red), the best performance is obtained for highly reflected surfaces for such color, as is the case for white surfaces.

Figure 14 shows the object scanned and the image collected using the laser triangulation principle and the detection system that integrates the sensor described

above, in real time, without any type of data treatment. It should be noted that a very good image is directly collected, which allows a fast 3D scan inspection or the reconstruction of surfaces, such as moulding features used to rebuild bones or teeth in the field of life sciences.

4.4. Thin film transistors

The performance of the ns-Si:H TFTs analyzed using different dielectrics and channel lengths is summarized in Tables 4 and 5, and Figure 10. Overall, we notice significant progress since the first device reported by LeComber et al. [11] and the present values are among the highest recorded in the literature for a-Si:H [73–79] or nanostructured silicon TFTs [80–82]. The improvement observed for the TFTs performance is mainly related to two factors: lower growth rate used and reduced hydrogen bombardment at the growing surface, which reduce defects.

For devices produced using ATO as the dielectric, the maximum on/off ratio was estimated since the transfer curve in the linear regime is not totally defined for source and drain current (I_{DS}) below 10^{-12} A. This effect is now under investigation and seems to be induced by ATO and does not correspond to measuring limitations. Thus, we can only say that the on/off ratio is higher than 10^7 . Also, the sub-threshold slope calculation is affected by the incomplete definition of the I_{DS} current below 10^{-12} A.

The data for ns-Si:H TFTs using thermally oxidized silicon and hafnium oxide as dielectric are also depicted in Figure 10a. The electrical characteristics of the devices produced on SiO₂ (see Table 4) are even better than those using ATO. The field effect mobility is now $1.24\text{ cm}^2/\text{V/s}$, while the I_{DS} is well defined down to 10^{-14} A, closer to the semiconductor analyzer measuring limit. Thus, we can clearly state that the on/off ratio is well above 10^7 , which confirms that the dark conductivity of the ns-Si:H layer is low, allowing off currents on TFTs below 10 fA. The threshold voltage is slightly higher than for ATO devices. This can be explained by the lower capacitance of SiO₂, which is 34 nF/cm^2 , on a 100 nm thick layer, when compared to the 64 nF/cm^2 for ATO. We must also take into account the difference in the gate electrode, which contributes to changes in the V_T value.

TFTs integrating a high k dielectric, such as HfO₂ were also produced (see Figure 10a). For a thickness of 300 nm, we found a capacitance of 50 nF/cm^2 , corresponding to a dielectric constant of ~ 17 . The electrical performance exhibited by these devices is not so impressive, which is attributed to the greater roughness of the dielectric surface. Despite being deposited at room temperature, sputtered HfO₂ normally presents a microcrystalline structure [53], which leads to a rough surface morphology as opposed to the smooth surfaces of amorphous ATO and SiO₂. This contributes to the creation of defects on the dielectric/semiconductor interface side of the bottom gate of the TFTs, affecting g_m and, thus, μ_{FE} and V_T . Also, the density of fixed charge in a 300 nm HfO₂ layer, which is normally positive and $\sim 10^{12}\text{ cm}^{-2}$ for sputtered films deposited at room temperature, is pushing the V_T towards high values (5.19 V).

Since the use of SiO₂ leads to better electrical performance on ns-Si:H-based TFTs, this dielectric was employed to monitor the effect of the channel length.

A device with a W/L of $50 \times 50 \mu\text{m}$ is compared with that already presented in Figure 10a, where the channel dimensions, W/L are $15 \times 15 \mu\text{m}$. Transfer characteristics on linear and saturation regimes, as well as the extracted electrical parameters exhibited by these devices, are, respectively, depicted in Figure 10b and summarized in Table 4. The data obtained show that g_m increases by $\sim 50\%$, which corresponds to $\mu_{FE} = 1.84 \text{ cm}^2/\text{V/s}$. However, V_T and S for long channel TFTs are, respectively, 20 and 10% higher than the values obtained in short channel TFTs. This behavior is attributed to the effect of the contact resistance (R_C) at source and drain regions, which is known to negatively affect device mobility, since the effective source to drain voltage is given by $V_{DS} - R_C I_{DS}$ [83]. In addition to affecting mobility, the contact resistance induces an error in extracting the device power parameter and V_T by the amount of $R_C I_{DS}/2$. This limitation is more pronounced on short channel devices, since I_{DS} is proportional to V_{DS}/L . The highest field effect mobility value ($2.47 \text{ cm}^2/\text{V/s}$) was obtained for devices where the active layer was produced using an optimized grid with larger holes (named 50/50 OG; Figure 10c). In this case, their diameter is 1.5 times larger than those used for fabricating the other devices, allowing a better balance of the hydrogen bombardment effect on the films properties. This is also reflected in the other electrical parameters determined from the transfer curve (Table 5).

5. Conclusions

In this work, we have focused on the deposition of nanostructured silicon (ns-Si:H) by PECVD in the so-called transition region and have shown improved properties, in comparison with amorphous silicon, when included in diverse applications. The hydrogen exodiffusion evolution observed on samples produced in this transition region shows two peaks, one at low temperature (698 K) and other at high temperature (840 K), associated with an E_a of 87 and 135 kJ/mol, which completely differ from those observed in either amorphous or conventional microcrystalline thin films. The micro-Raman spectroscopy data show that, in the transition region, the curves shift slightly towards a higher wavenumber and become narrow, which could be explained by the incorporation of nanocrystallites or the existence of nanostructured aggregates in the film. The solar cells produced in a single chamber system show good quantum efficiency, current density = $14.48 \text{ mA}/\text{cm}^2$, short circuit voltage = 0.94 V and fill factor = 0.67, which corresponds to an efficiency of 9.12% under AM1.5 conditions.

We have also fabricated a 128 psd integrated array, which is capable of satisfying the requirements for 3-D image processing, with a 7-bit lateral digital resolution, speed rates up to 10,000 frames per second, with a detection error below 5%, an image deep resolution of 2.5–0.2 μm , a horizontal resolution in the range 50–10 μm , a linearity better than 99.9%, and a frequency response better than 500 kHz. In other words, the integrated array can process frame image in real-time and fast enough to allow image inspection in a continuous manner.

The ns-Si:H TFT produced using a grid to control ion bombardment during the growth process lead to devices with improved μ_{FE} . Among the different types of dielectric used, it can be seen that TFTs based on SiO_2 exhibit the best μ_{FE}

($1.2\text{ cm}^2/\text{V/s}$), with on/off ratio higher than 10^7 and V_T close to 2 V. It was also verified that these TFTs suffer from non-negligible influence of source and drain contact resistance. This was verified on devices with longer channel, where μ_{FE} is $\sim 1.84\text{ cm}^2/\text{V/s}$. The optimization of the grid hole dimensions allowed the improvement of this value to $2.47\text{ cm}^2/\text{V/s}$. Another remarkable result concerns the use of dielectric materials other than conventional silicon oxide-, silicon nitride- or silicon oxynitride-based materials. These are the so-called high k dielectric films, ATO and hafnia, where the results achieved indicate a clear window for further improvement in TFTs' performance.

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