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1. Title: Hybrid Optical/Digital Processor for Radar Imaging

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c. Automated Tools for Embedded System Development

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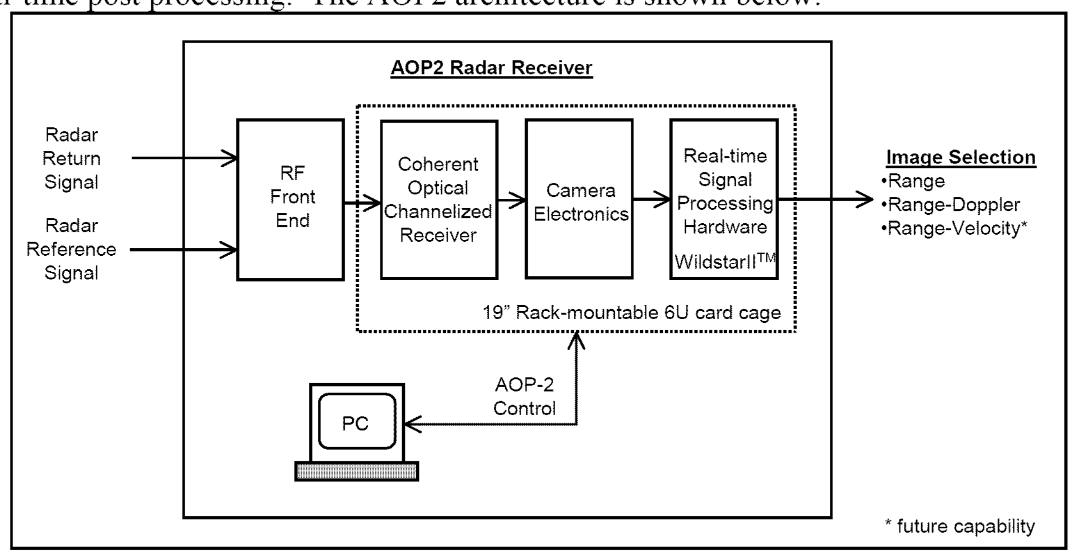
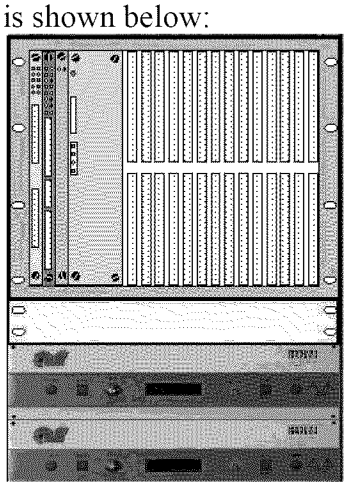
7. Abstract

Essex is developing a prototype hybrid optical/digital processor for radar image formation using wideband arbitrary waveforms. The processor is called the Advanced Optical Processor (AOP) and is a hybrid acousto-optic/digital processor that generates high dynamic range, range-Doppler images from wideband radar returns. This work is being funded by the Missile Defense Agency's office of Manufacturability and Producibility (MDA/MP) and will be tested at the MIT/LL Lexington Development Facility. The processor supports high resolution processing necessary for target discrimination and kill assessment by enabling the use of true arbitrary, wideband waveforms. The selected architecture combines the advantages of both embedded optical signal processing for the front-end receiver and embedded high-speed digital signal processing for the real-time post processing. This combination provides the capacity to process signals with 1 GHz of instantaneous bandwidth in a real-time environment without the need for wideband analog-to-digital converters (ADCs). This is achieved in a compact lightweight package that combines both an optical coherent channelizer and a WILDSTARII™ FPGA VME board from Annapolis Micro Systems that performs the real-time post processing. The AOP2 architecture is shown below:



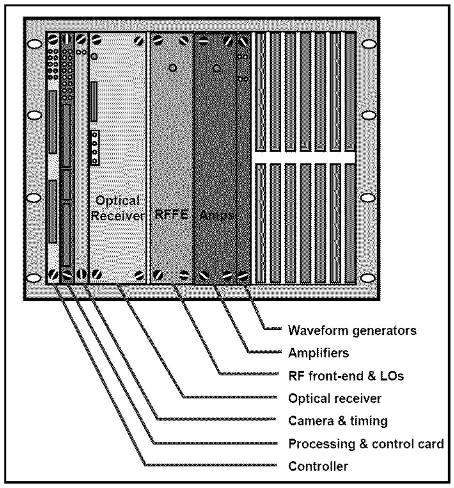
AOP2 Architecture

The AOP2 prototype hardware is shown below:



AOP2 Prototype Hardware

The production hardware can easily fit into a single 6U card cage, as shown below, without significant development costs.



AOP Production Configuration

By removing complex software and custom digital hardware, the cost for this processor is significantly less than an "all-digital" solution, even in modest quantities. The cost effectiveness of this processor allows use at the sub-array level for desired operational flexibility and performance enhancements, such as beamforming and STAP.

The development of this processor has been accelerated with the use of the AMS CoreFire™ FPGA Application Builder. This tool has allowed the mapping of the post processing algorithms to the COTS AMS FPGA hardware with minimal effort. Selected AOP2 algorithms were running as a demonstration in the WildstarII™ for the AOP2 critical design review with just a few weeks of effort. CoreFire™ also provided a hardware-in-the-loop debugger that allowed us to insert test data into the designs in the FPGAs and then review the test vectors from the host as they ran through each part of the algorithm. The AMS hardware configuration is a 6U form factor with 3 Xilinx Virtex II™ 6000 series FPGAs. This WILDSTARII board also has two I/O daughter card positions providing in excess of 4 GB/s I/O bandwidth. The DSP algorithms running in this hardware include:

1. data formatting algorithms
2. calibration algorithms
3. range-compression algorithm
4. Doppler compression algorithm
5. data storage formatting
6. display formatting
7. system timing and control functions

The chosen hardware can perform these algorithms in real-time and is flexible such that changes in the algorithms are easily accommodated. There is no operating system required so integration issues with a single board VME control computer are minimal.

Presented in this paper will be the architecture description and integration of the optical and FPGA technologies, along with updated test results.

ESSEX

Annapolis Micro Systems, Inc.

Hybrid Optical/Digital Processor for Radar Imaging

23 September 2003

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Problem Statement and Solution

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- **Problem:**
  - Projected BMD threat environment will have clutter and EMI
  - LFM waveforms have limitations with these threats
  - Desired advanced waveforms (chaotic, PRN*, …) are very processing intensive

- **Solution:**
  - The advanced optical processor (AOP) generates range-Doppler images from advanced arbitrary waveforms
  - AOP architecture incorporates:
    - Embedded optical signal processing
    - Embedded digital signal processing in FPGAs

Program Objectives

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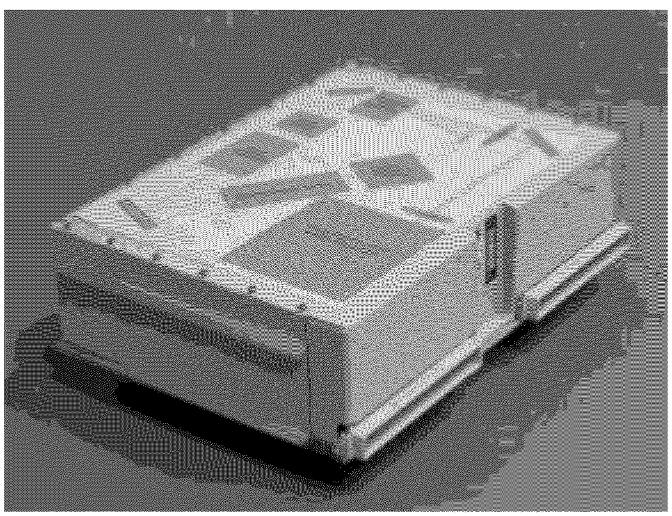
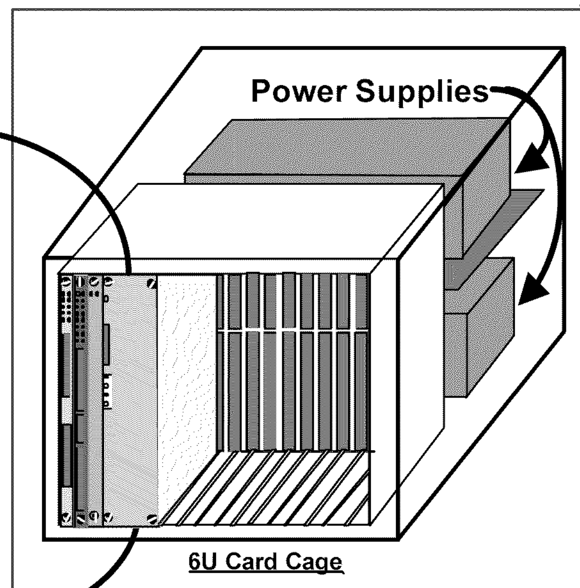
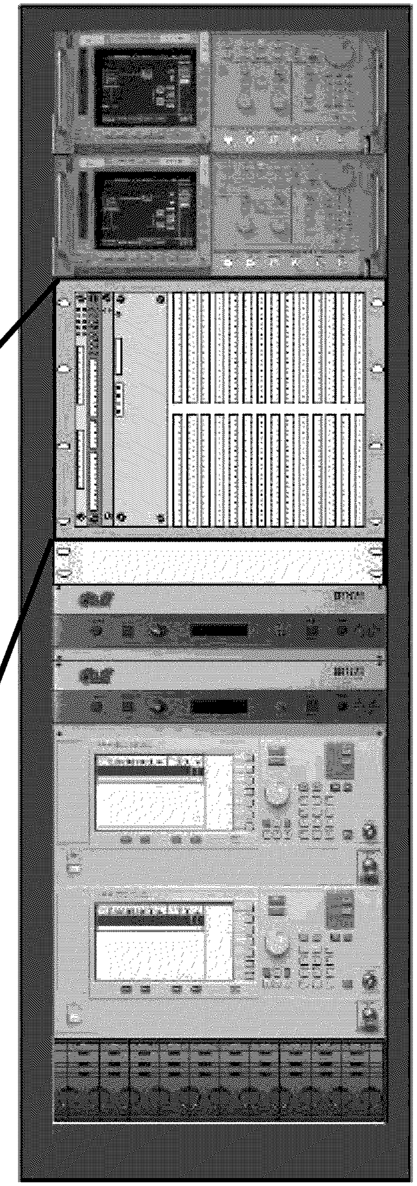
- Modernize the architecture, scaling to:
  - 1 GHz
  - Real-time operation
  - Full complex, single pass
  - Store images in real-time to disk
- Compact rack stackable configuration







AOP 2 Performance Characteristics

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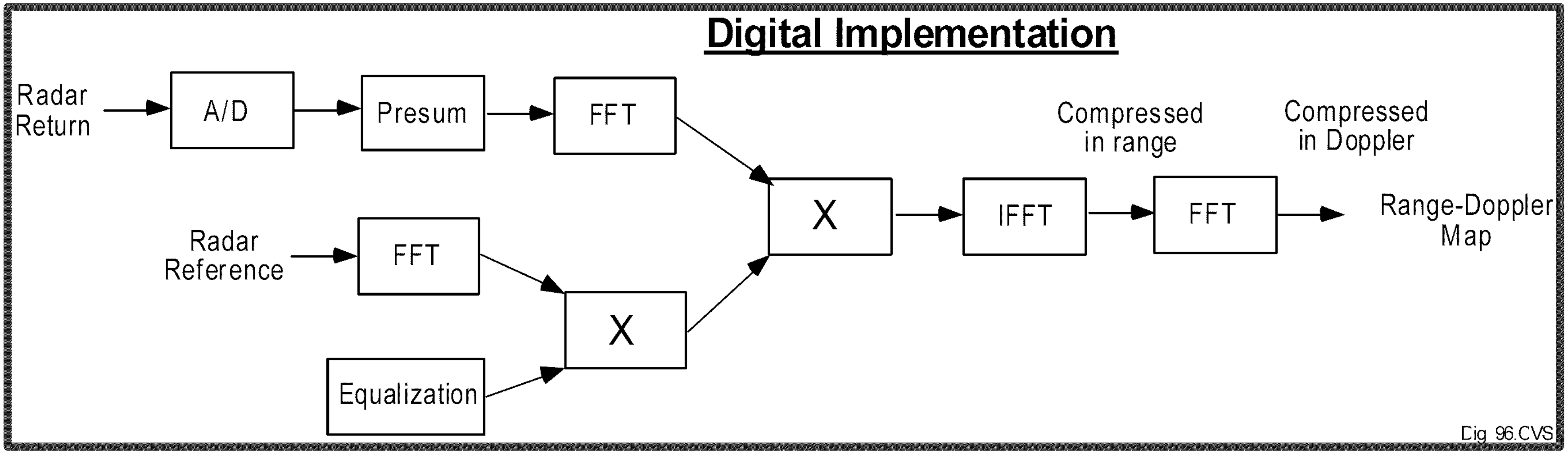
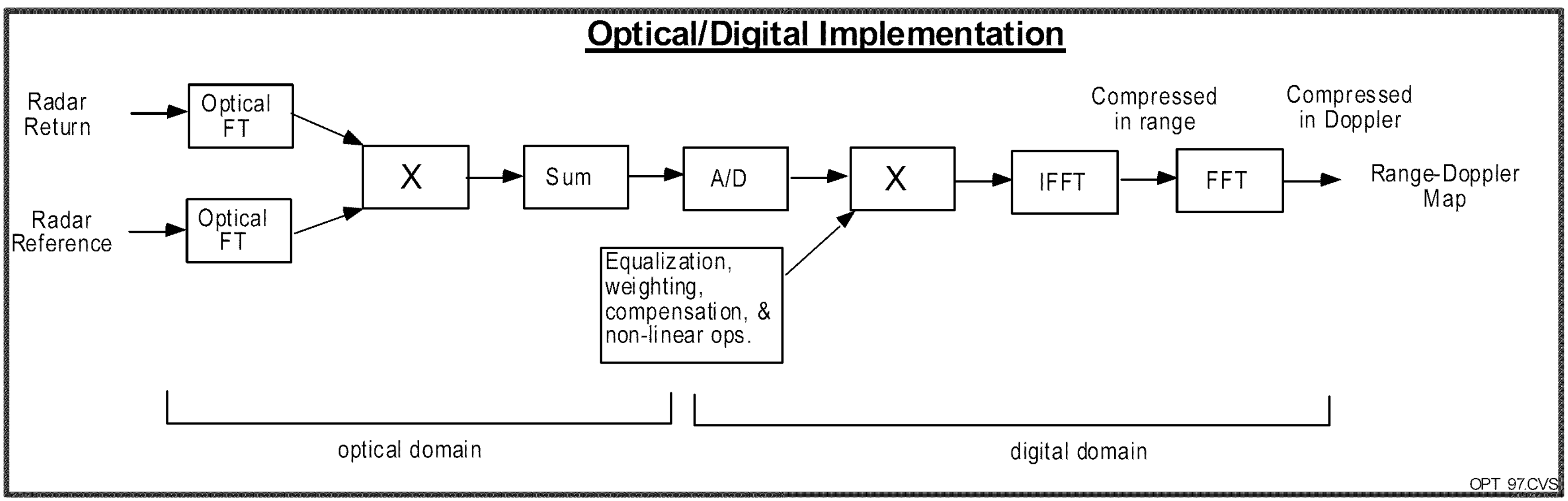
Pulse Width	10 ? sec to 50 msec
Pulse Repetition Interval (PRI) Pulse Repetition Frequency (PRF)	100 usec minimum 10 kHz maximum
Center Frequency	Tunable 5 GHz to 7 GHz (TBR)
Bandwidth (-3dB)	1 GHz
Stable Reference Frequency	10 MHz
Post-Compression Dynamic Range (peak to RMS noise)	66 dB
Spur Free Dynamic Range	85 dB for 128 coherently integrated pulses
Range Resolution	0.15 meters
SNR Loss vs. Range center	6 dB maximum @ +/- 76.7 meters relative to image center
Range Bins	1024 bins (+/- 512 about image center)
Range Extent	153 meters (+/-76.7 m about image center)
Range Sidelobes (Hamming weighting)	-34 dB
Frequency Response	3 dB uncorrected; 1 dB corrected
RCS Repeatability	+/- 0.1 dB
Phase Deviation from Linear in CPS	+/- 5 degrees

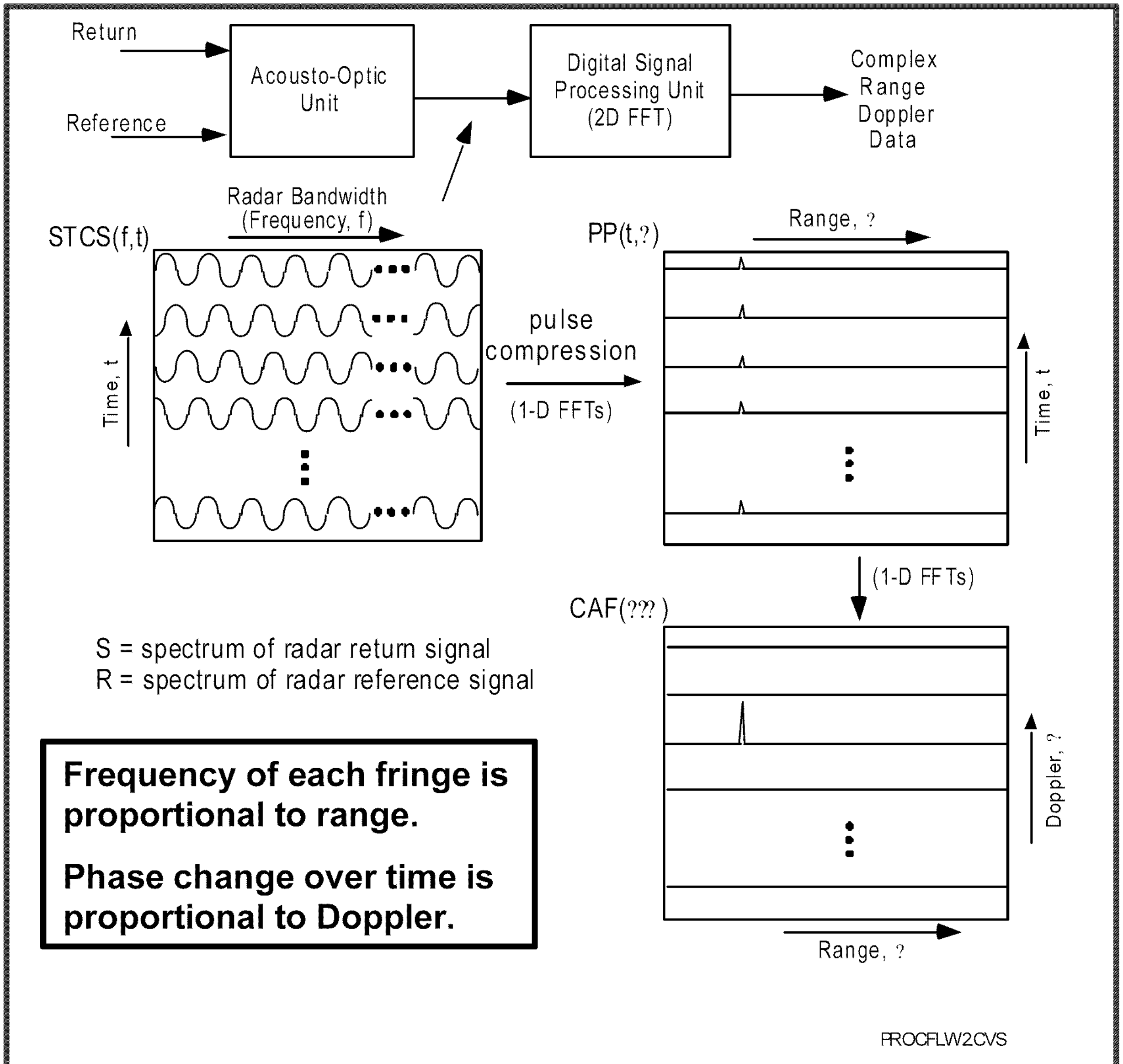
Algorithm Functionality is Similar





Process Flow

Cross power spectra vs. time



Correlator compresses pulse in range

FFT compresses pulses in Doppler

AOP2 Functional Configuration

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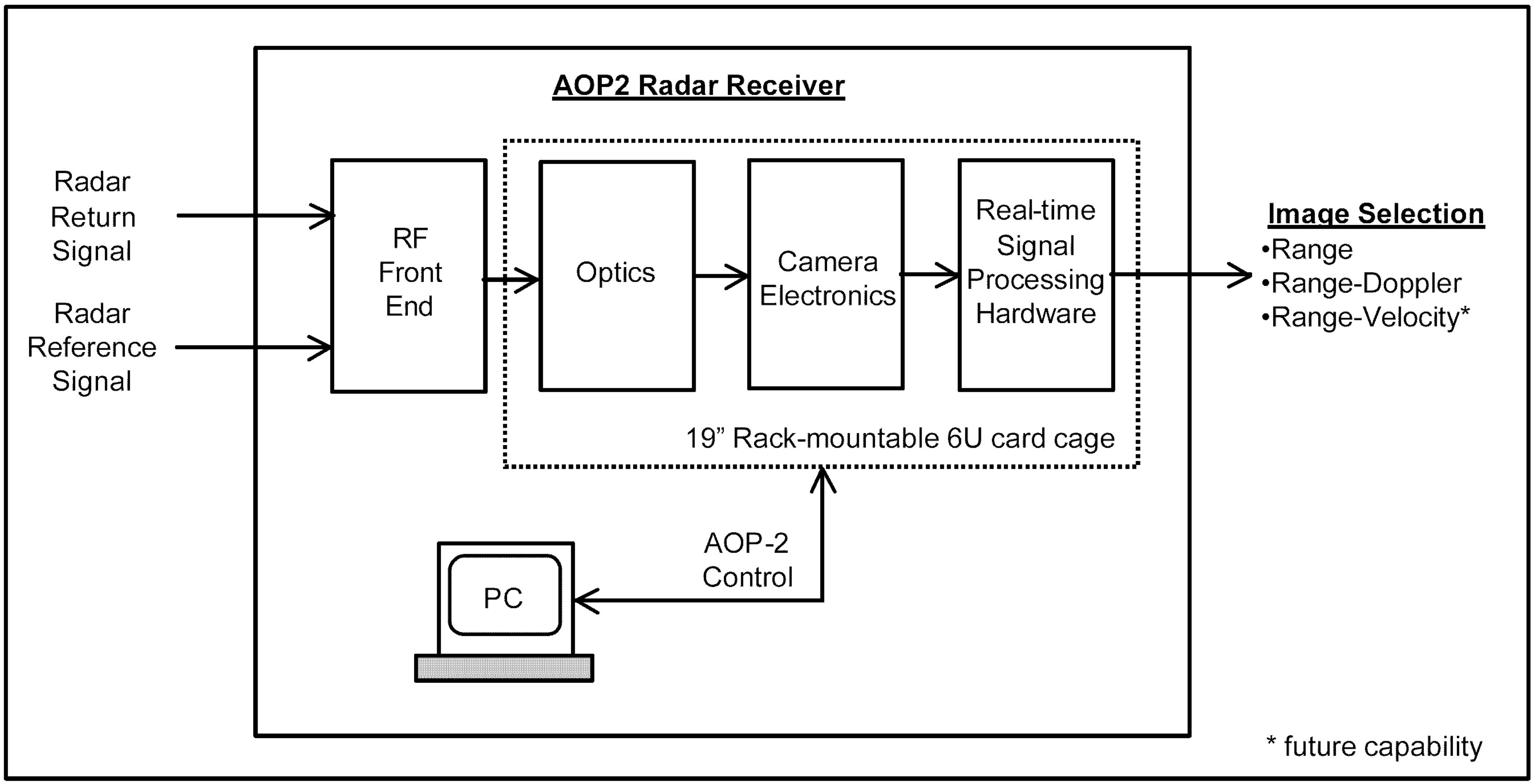

AOP 2 Top Level System Diagram

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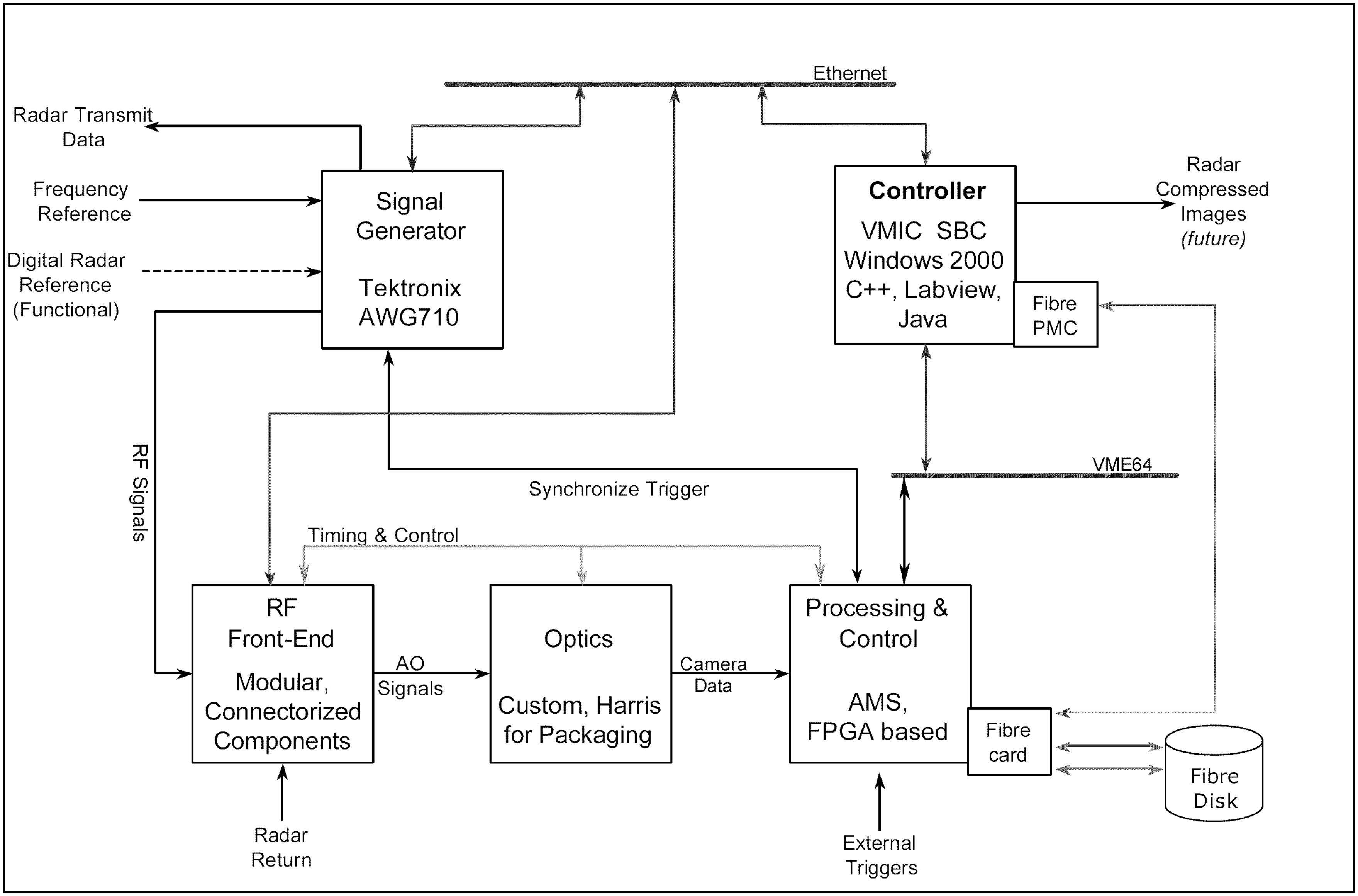
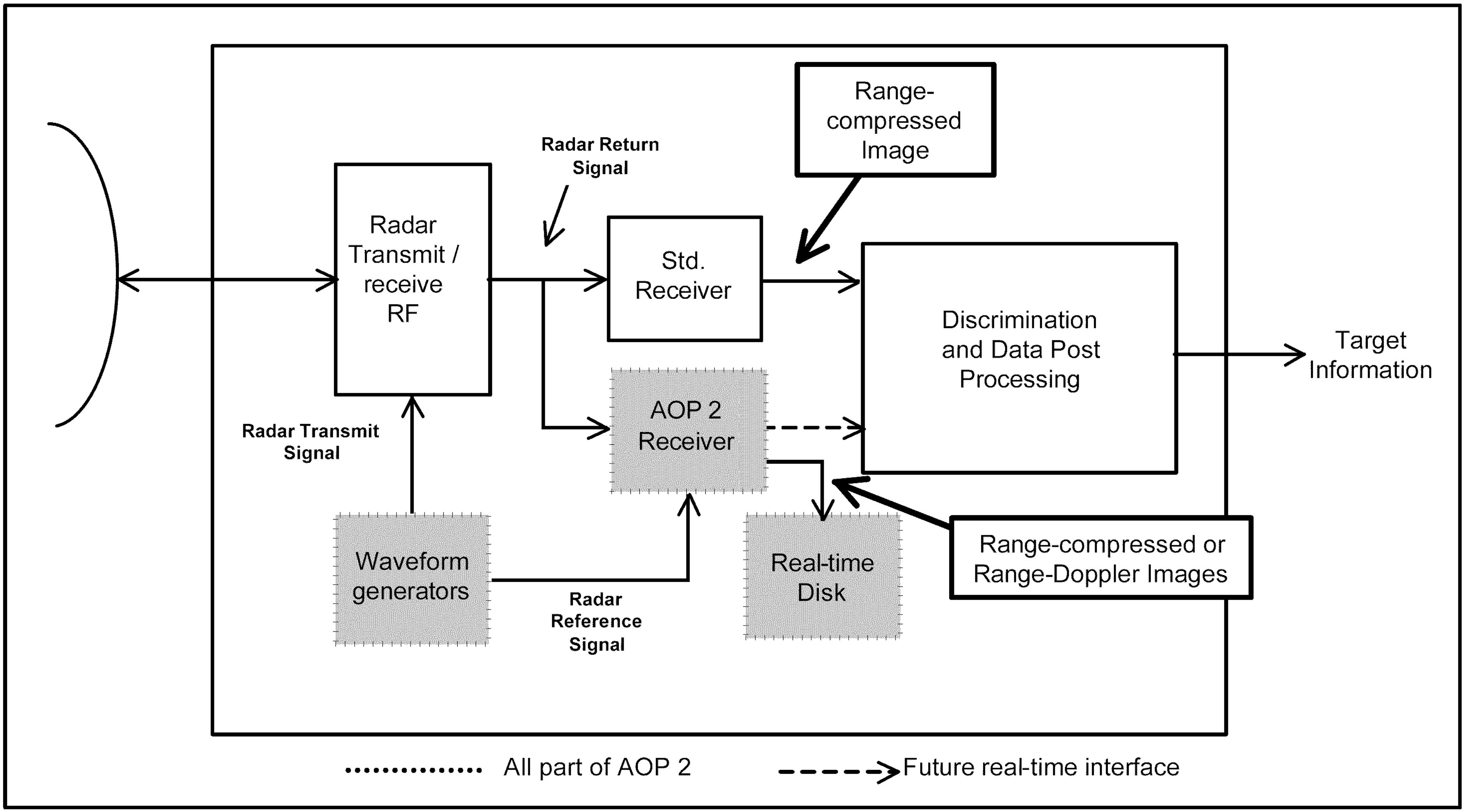


Radar Configuration with AOP2



Full Complex, Wideband Architecture

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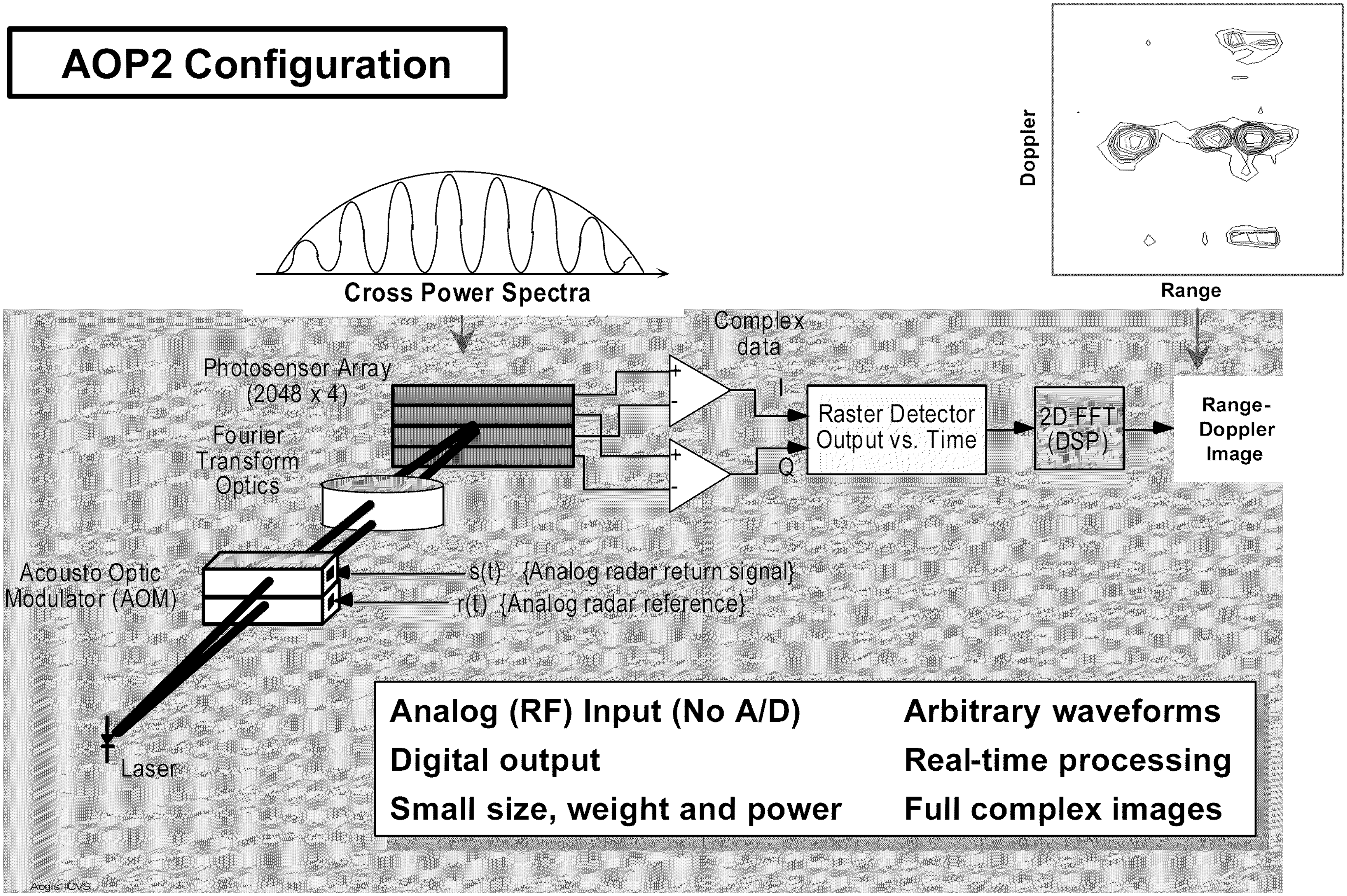
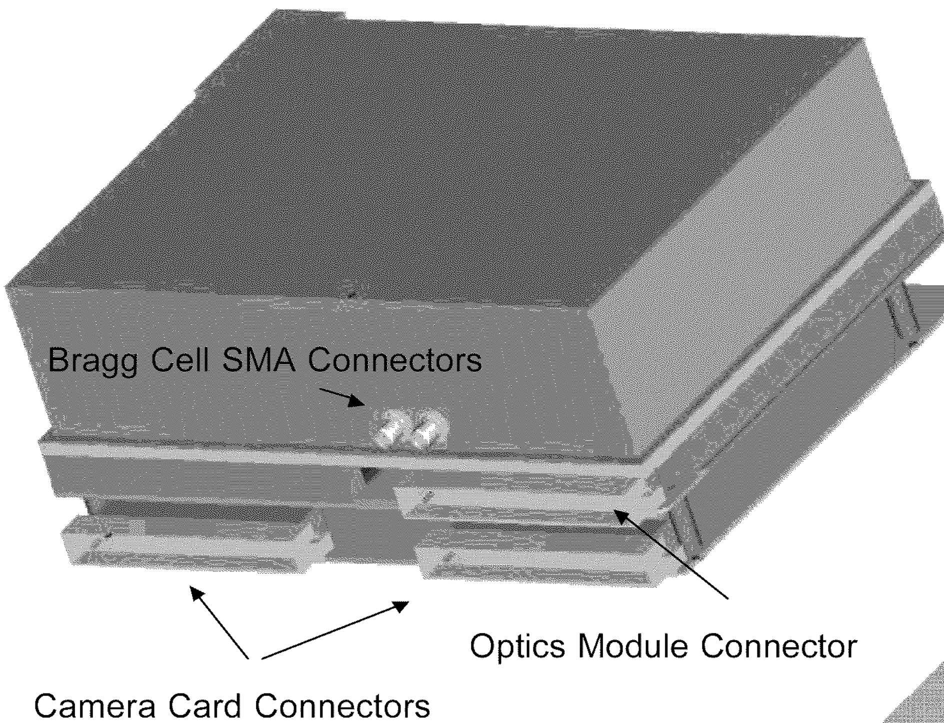
AOP2 Configuration

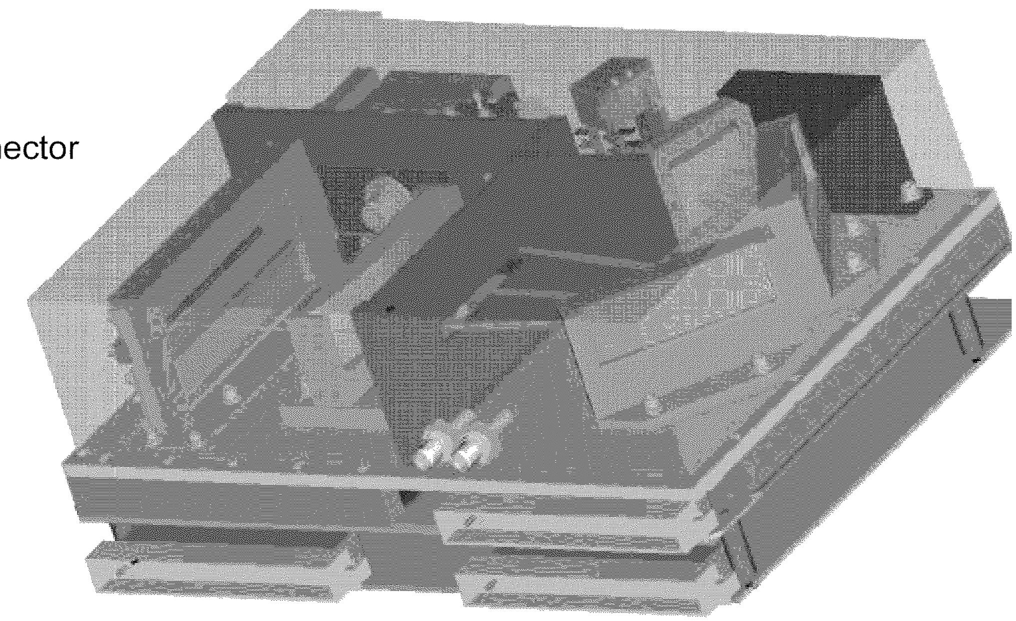


Analog (RF) Input (No A/D)	**Arbitrary waveforms**
Digital output	**Real-time processing**
Small size, weight and power	**Full complex images**

Optics Module Mated With Camera Module

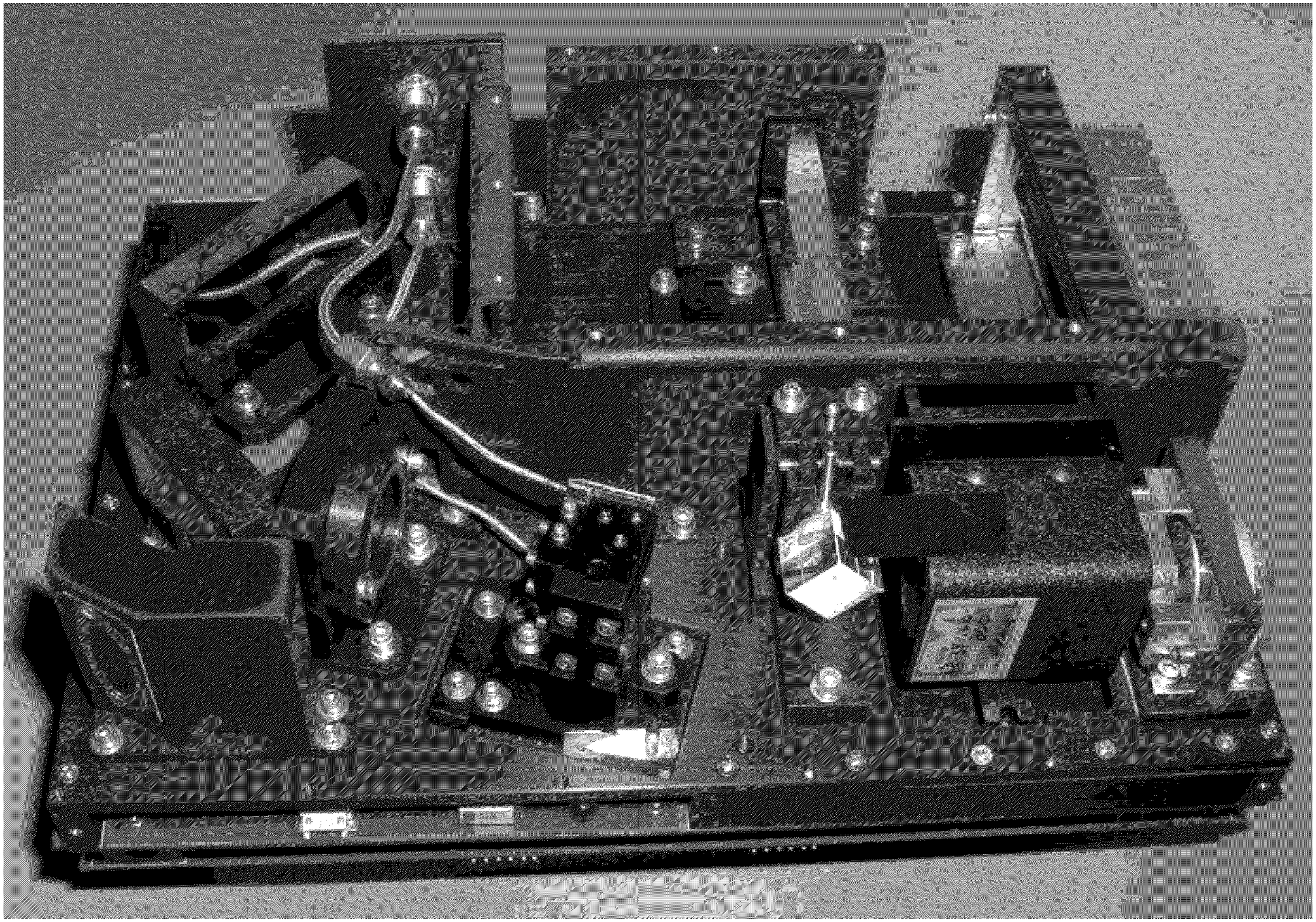


Optics Module
Camera Card
Optics Processing Module



6U VME form factor

AOP2 Optics Module



System Calibrations and Corrections

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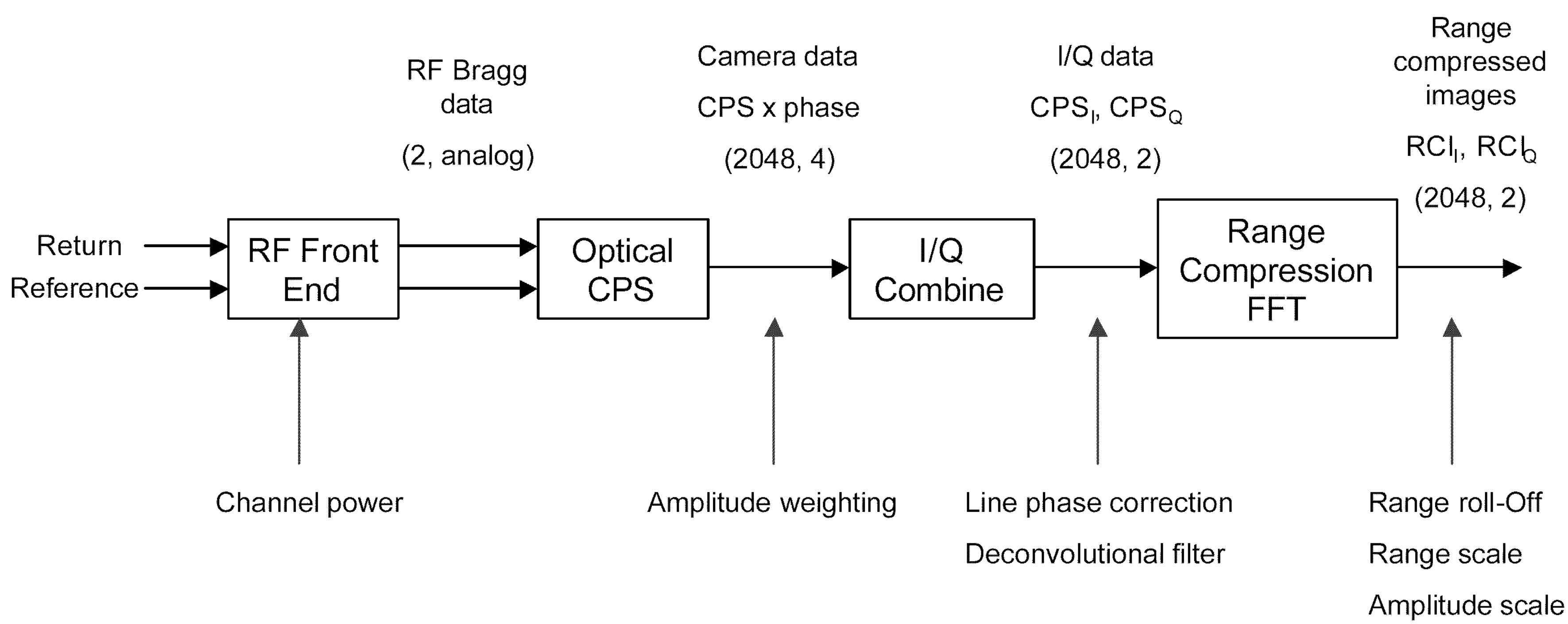
- **Calibrations and corrections are required at various points in the processing chain**
  - **Correct radar and processor response**
  - **Obtain optimum performance**



AOP2 Hardware Configuration*

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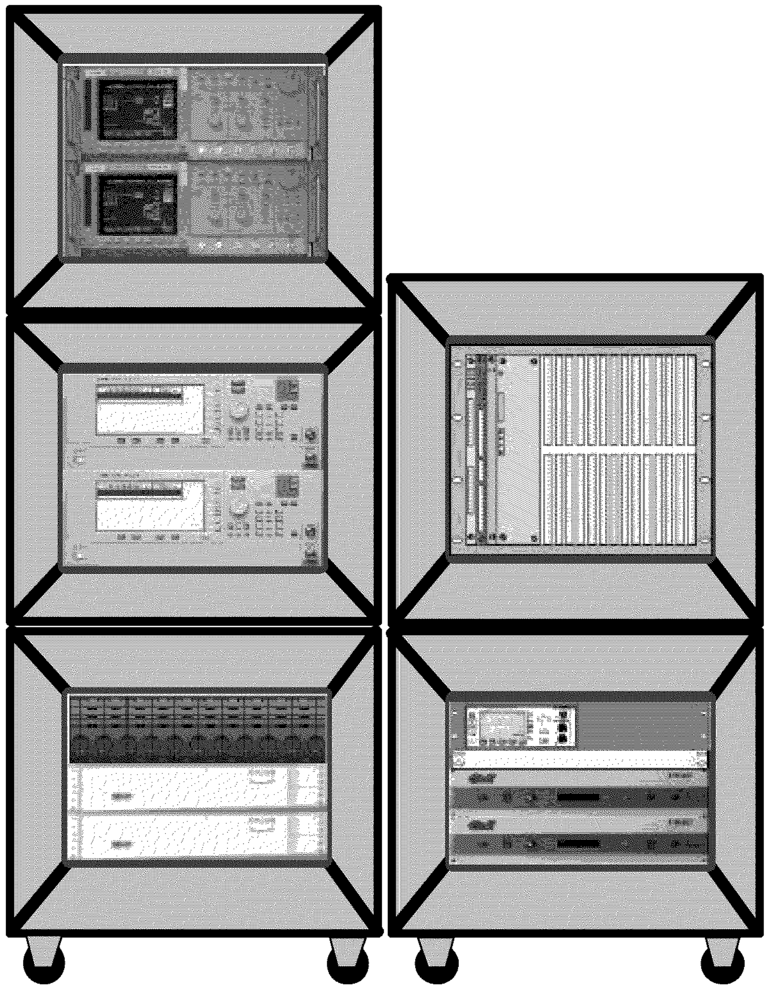
Waveform generators
- Reference
- Return

Programmable LOs for tunable RF front-end

Real-time file system

UPS



6U card cage
- Controller card
- Optical module
- Post processing & Timing card

Power Meter

RF module

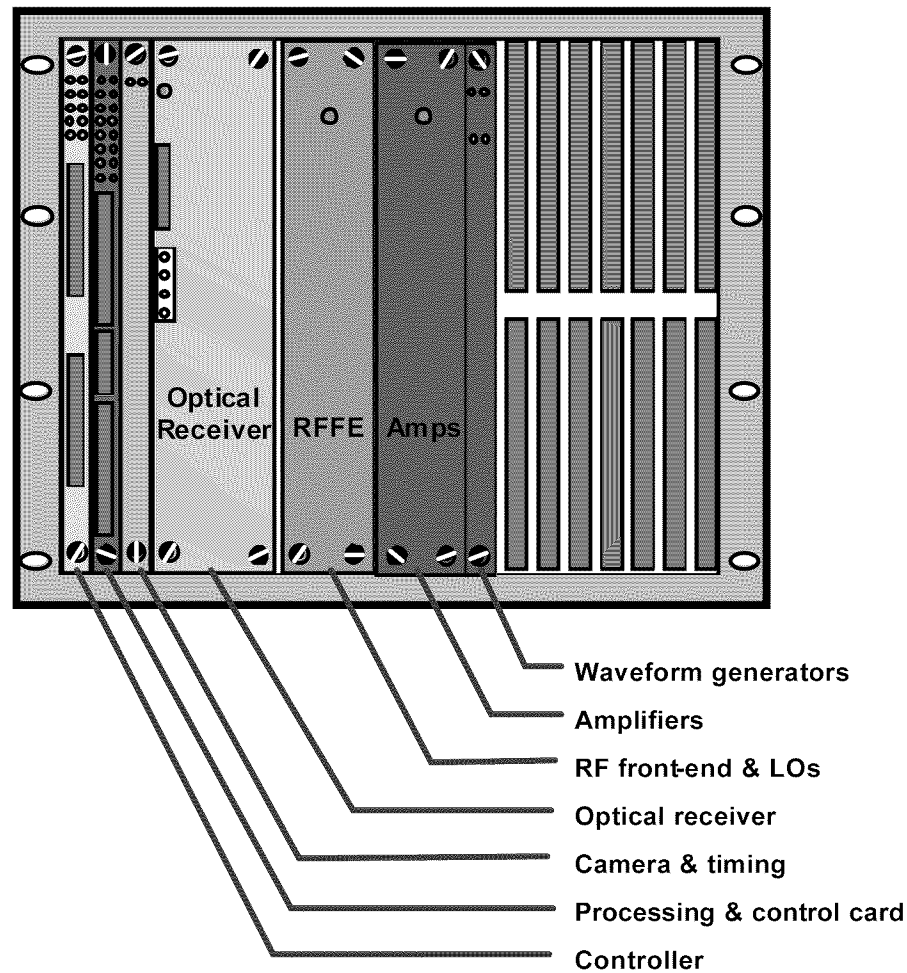
Power amplifiers

* Including test equipment

AOP Production Conceptual Configuration

Size reduced from ½ rack in AOP2 demonstration to ½ single 6U chassis:

- AWGs reduced to single chip for PRN codes
- Synthesizers reduced to fixed LOs
- Amplifiers reduced to single card
- No output data storage, data sent to radar post processing in real time



Post Processing & Control Subsystem (PCS)