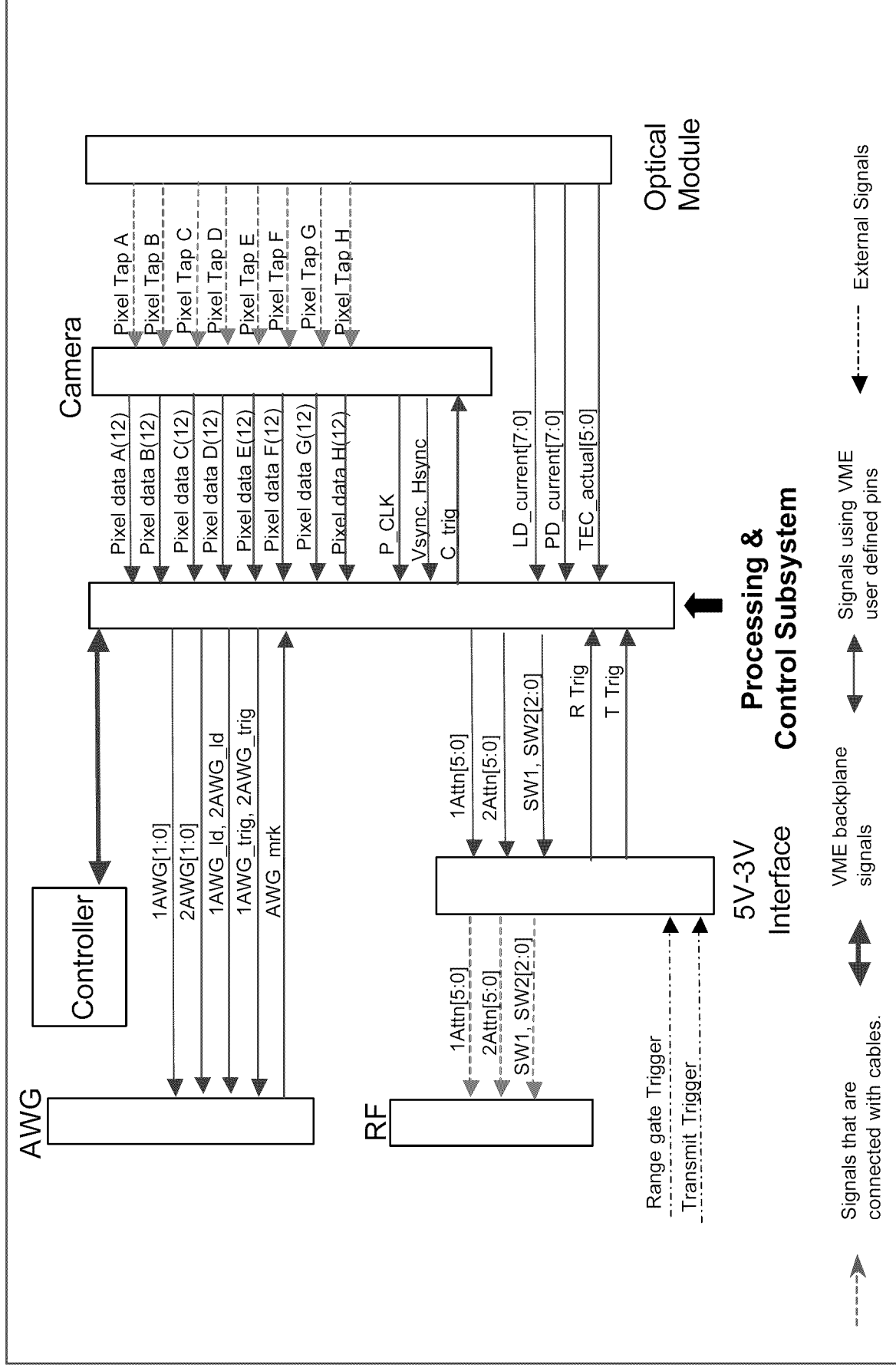
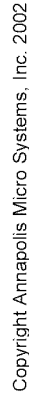


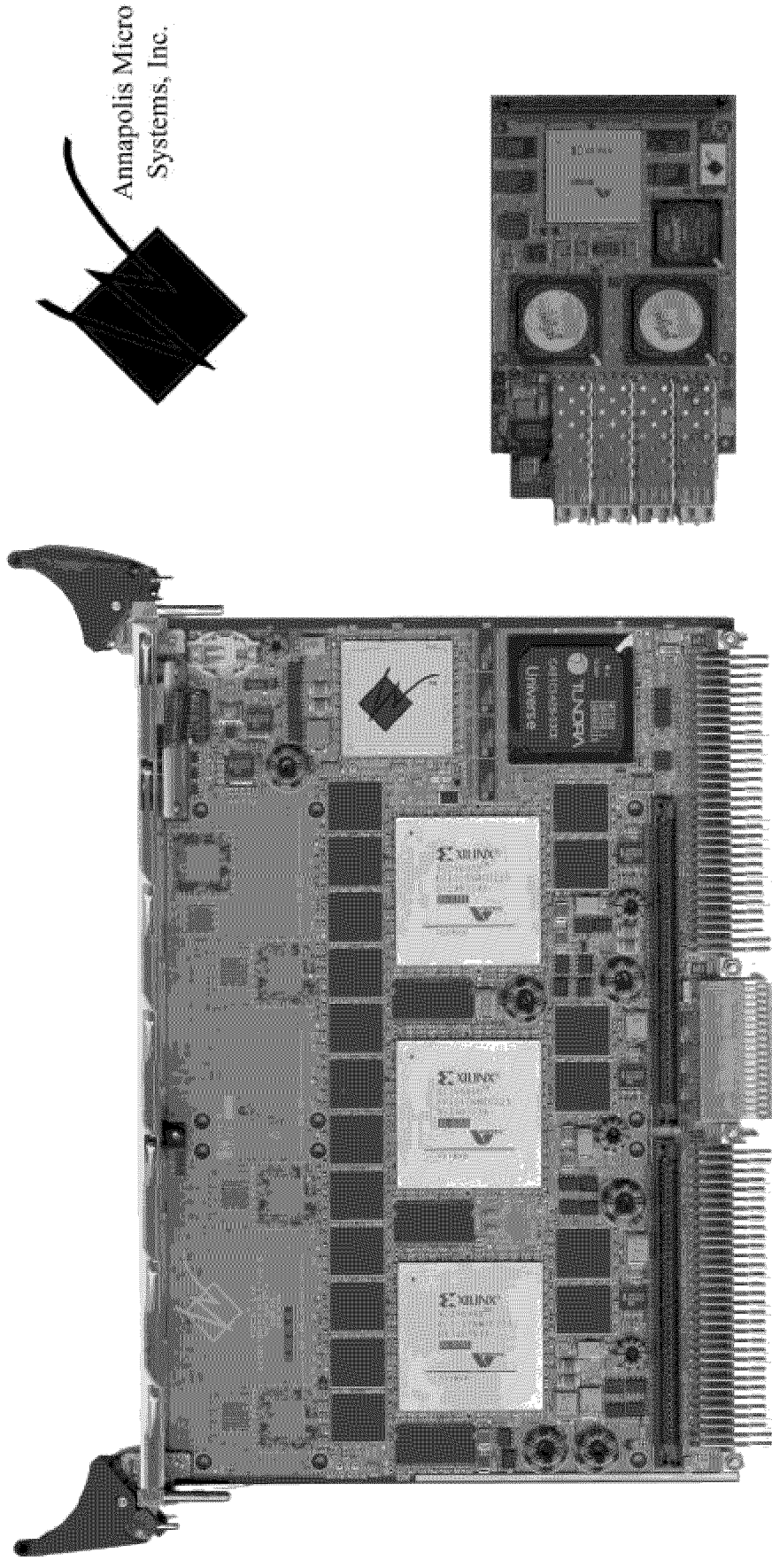


WILDSTAR™ II for VME



WILDSTAR™ II for VME & Fibre Channel 2 I/O Card

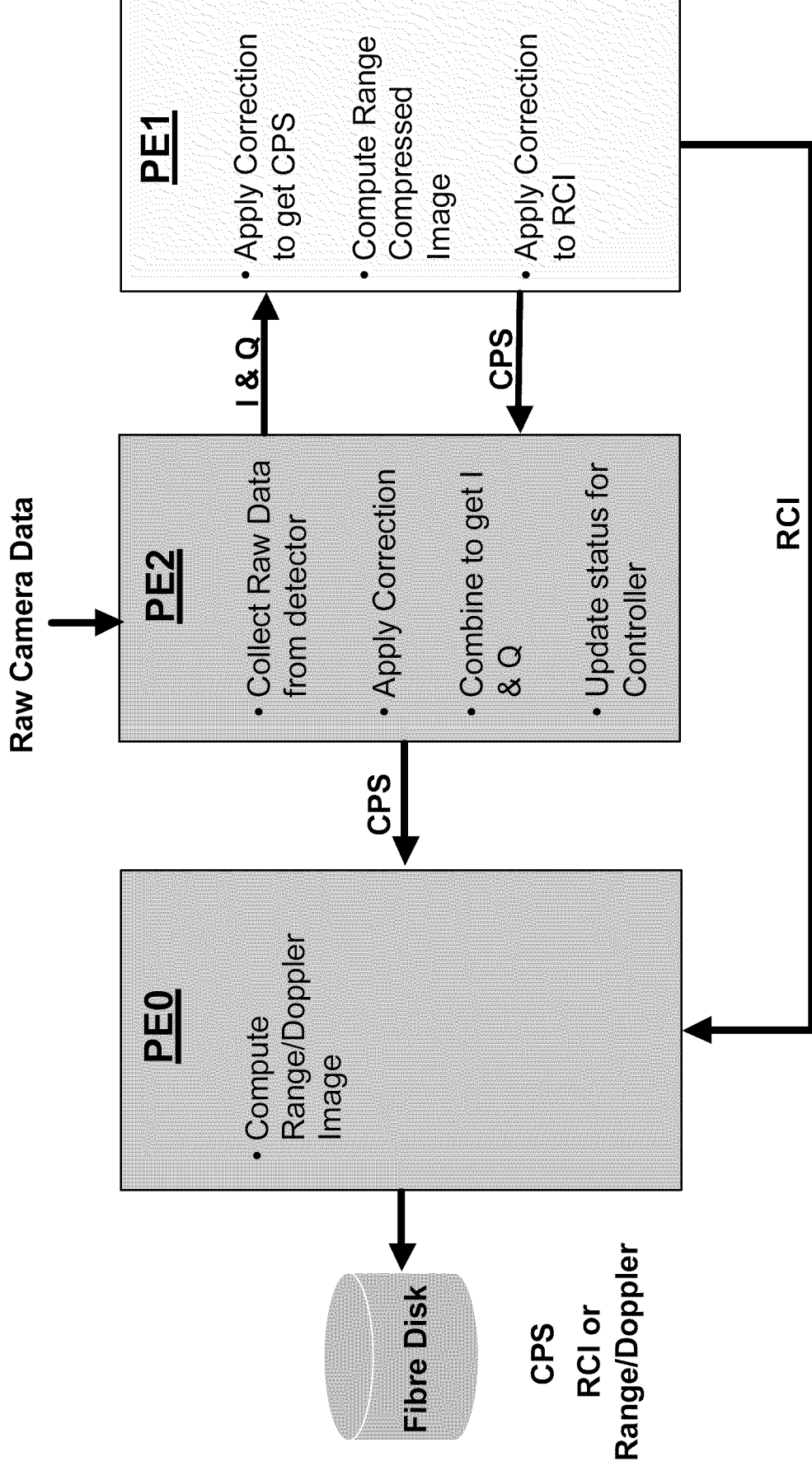
ESSEX

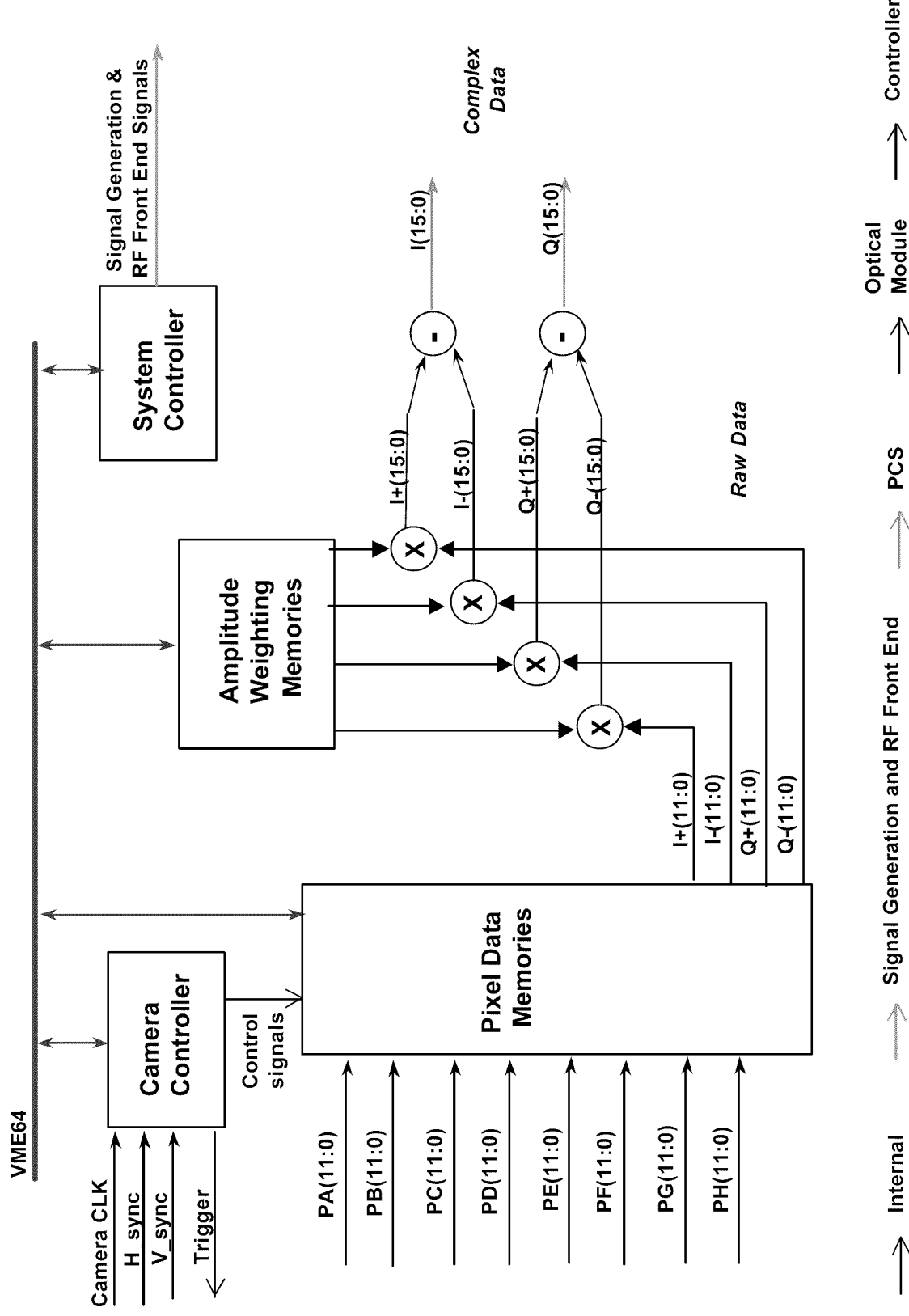


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WILDSTAR™ II FPGA card

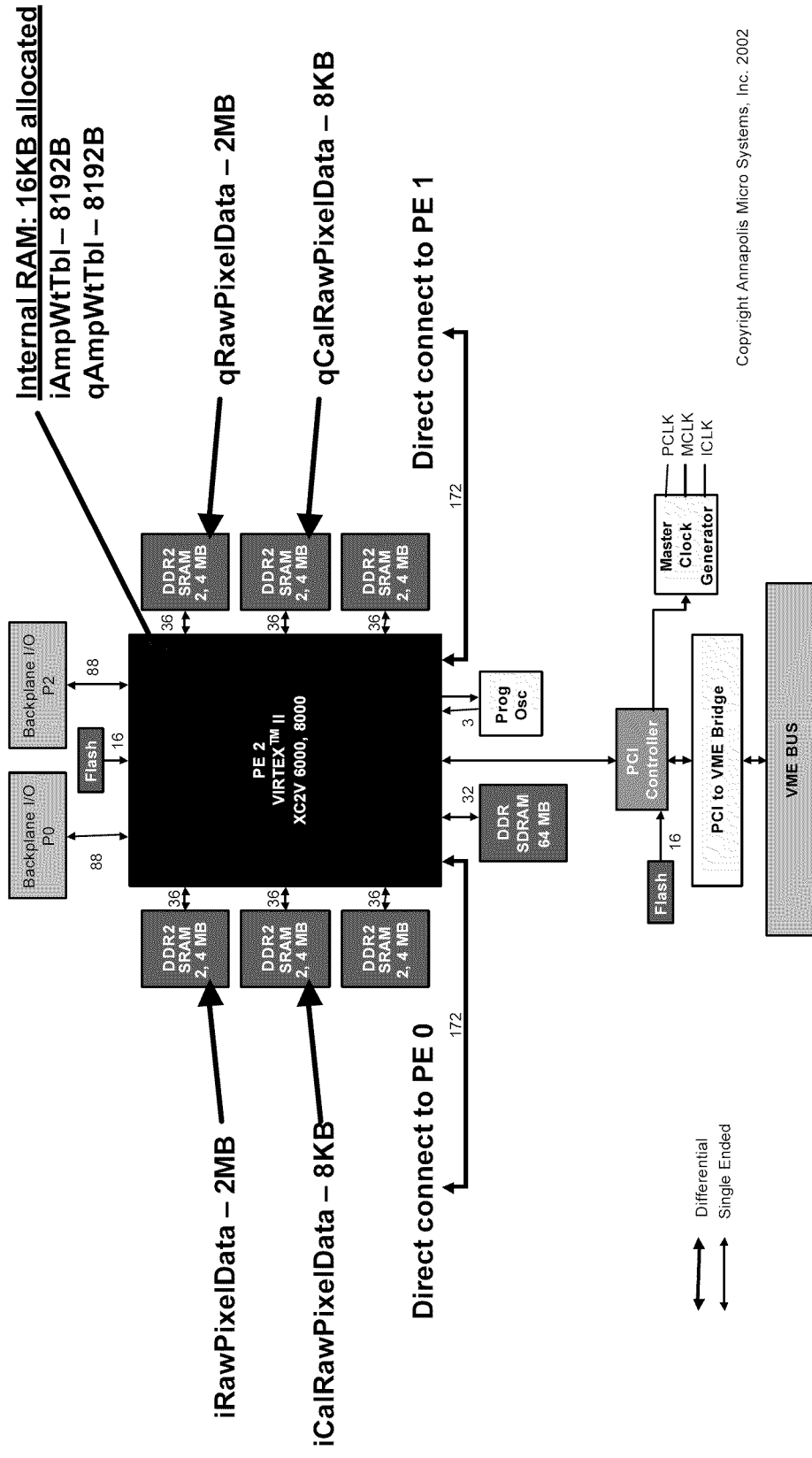
***Fibre Channel 2 I/O Card
daughter card***



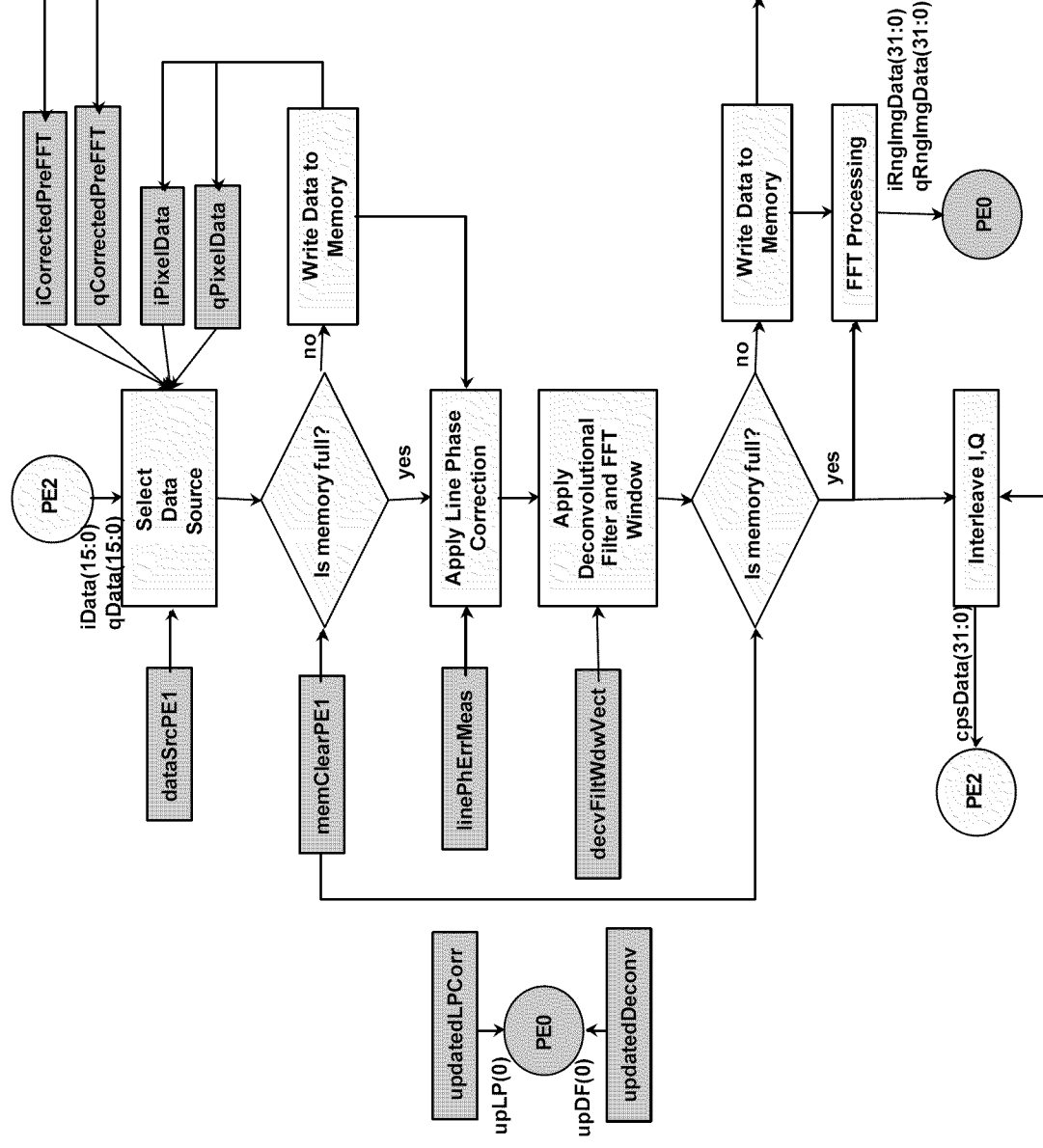


PE2 Allocated Memory Diagram

ESSEX

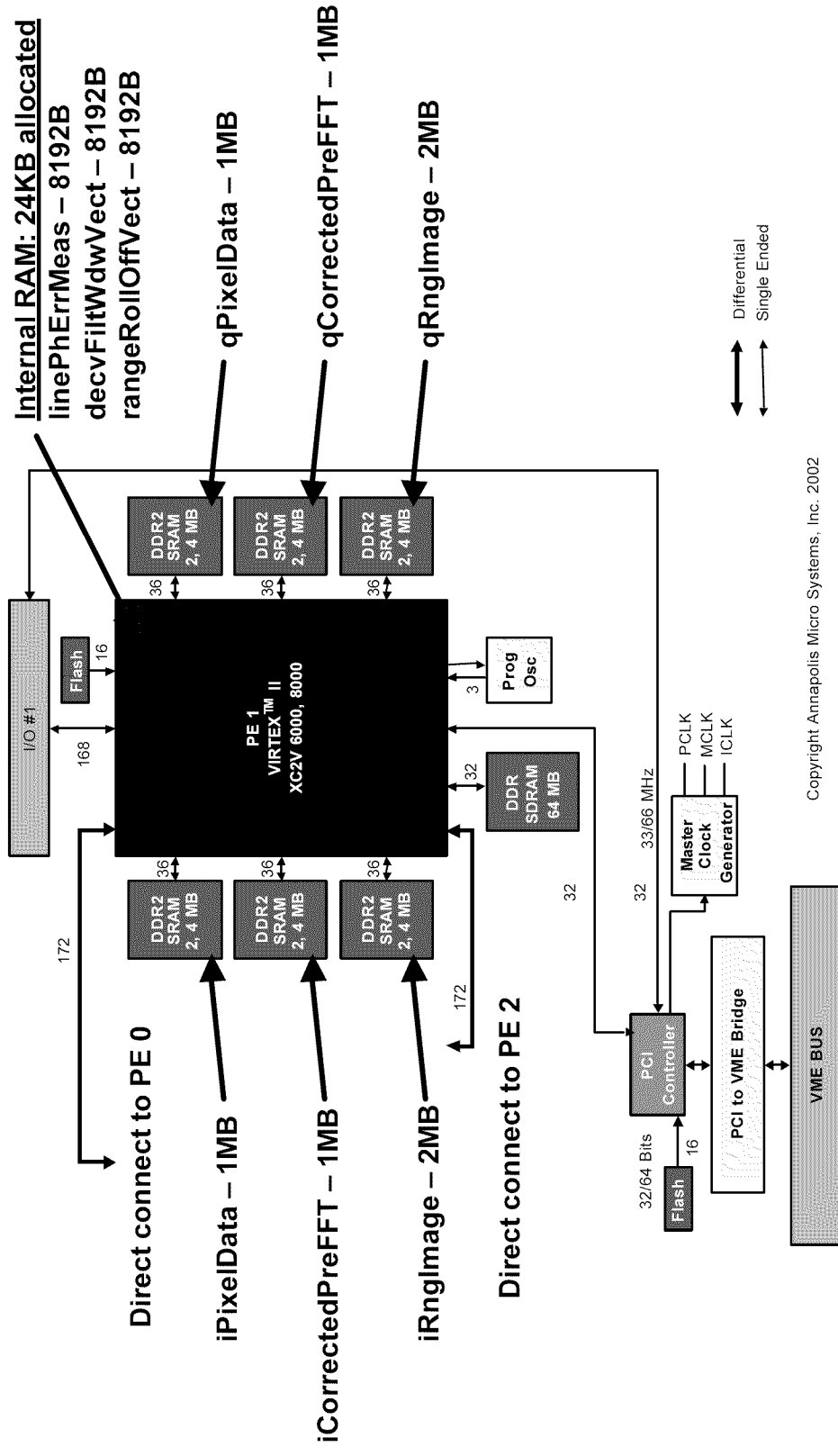


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PE1 Allocated Memory Diagram

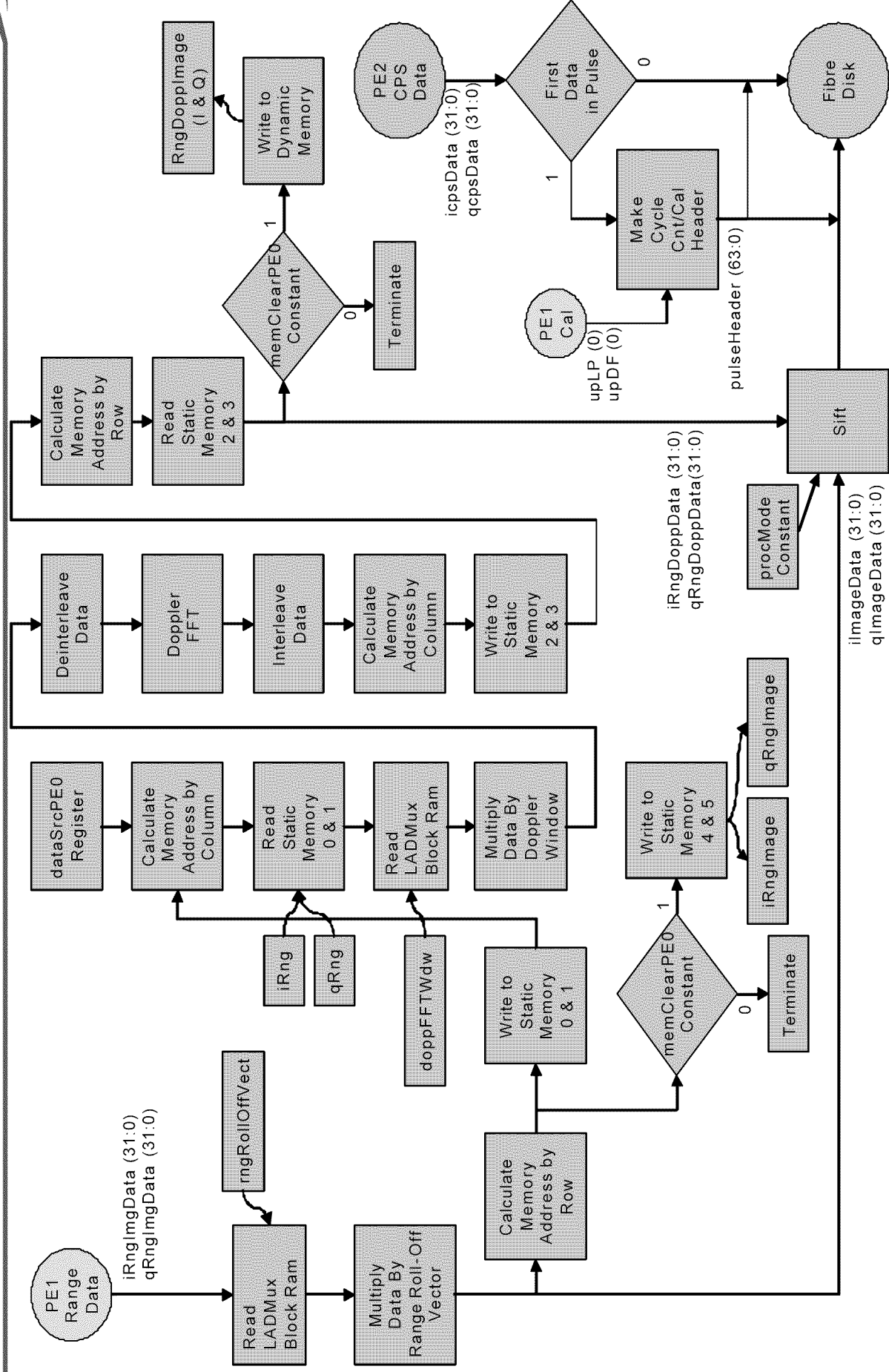
ESSEX



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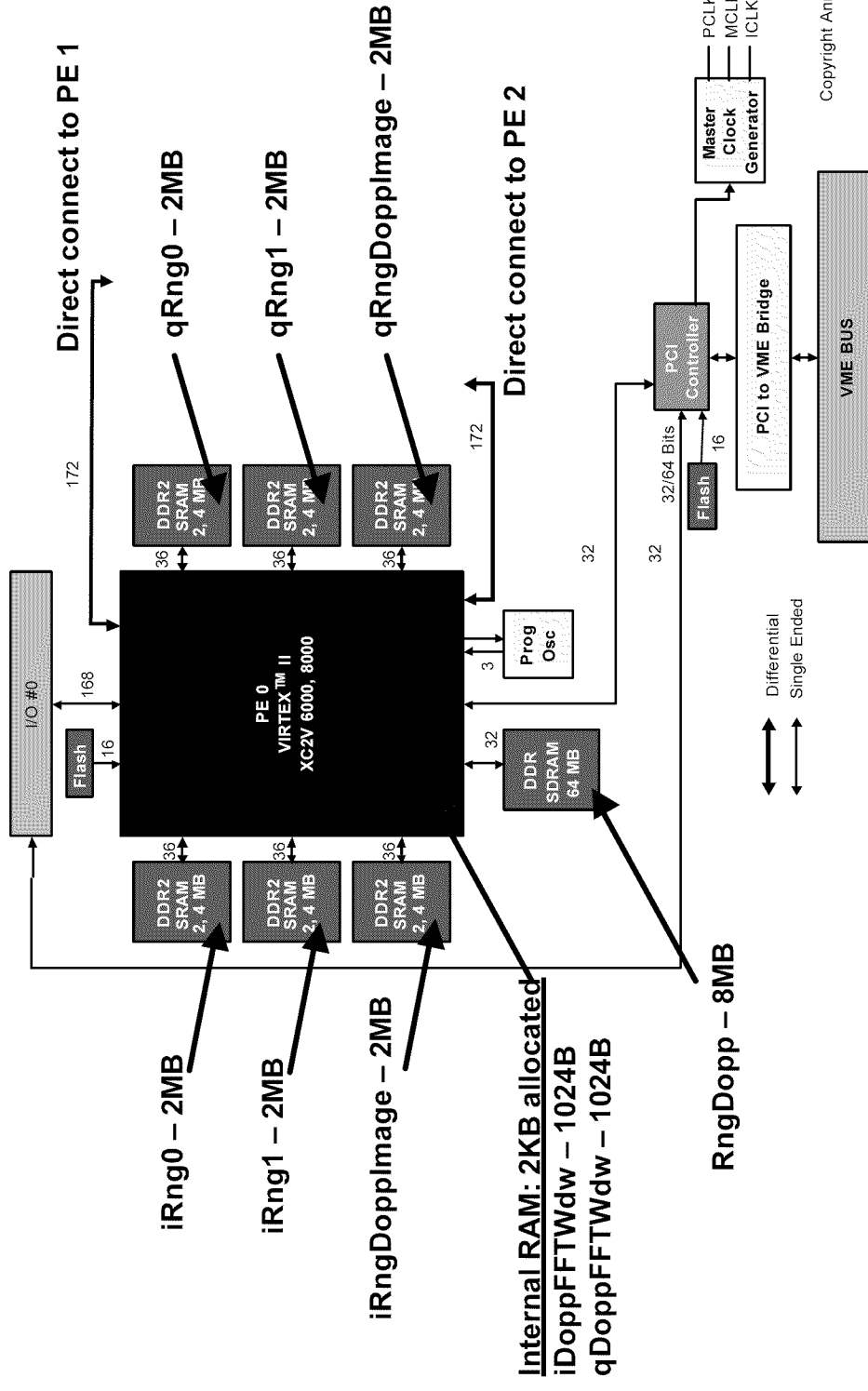
PE0 Functional Diagram

ESSEX



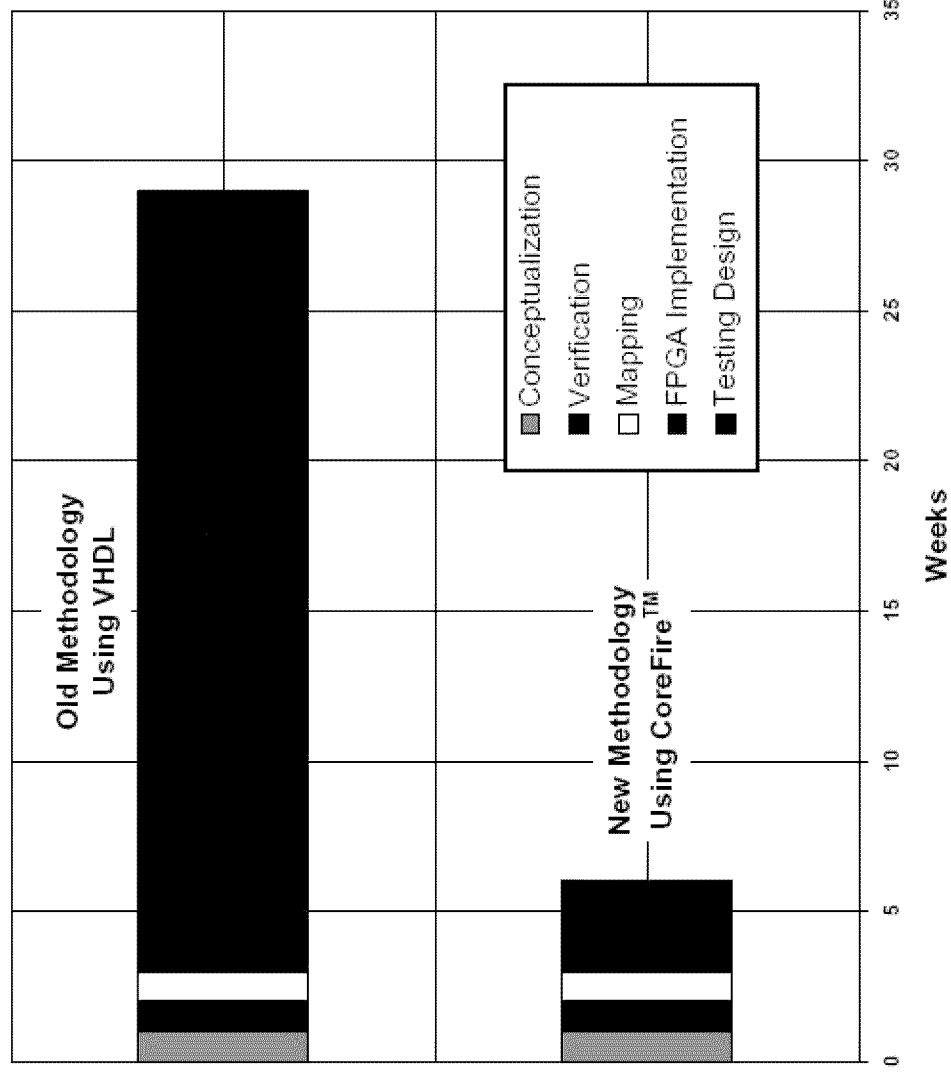
PE0 Allocated Memory Diagram

ESSEX

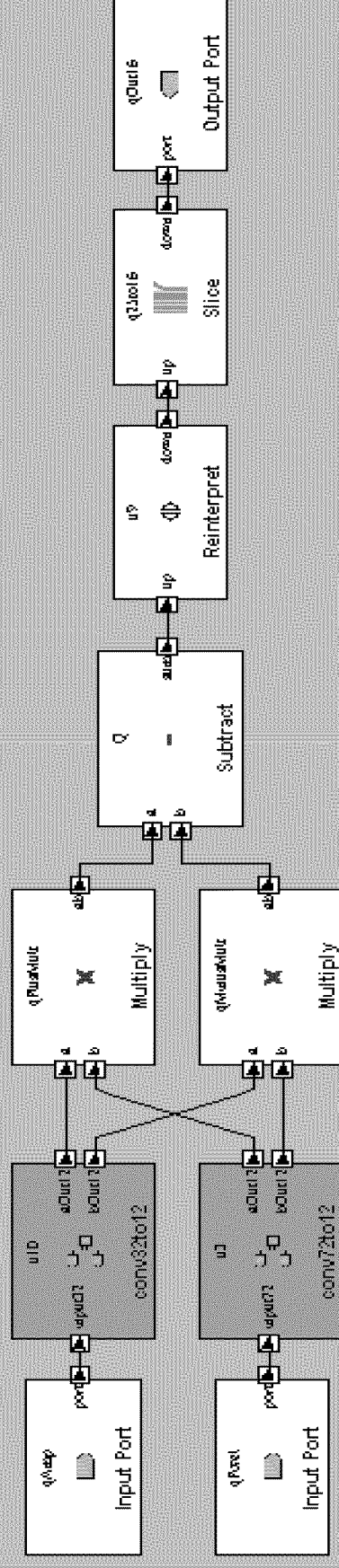
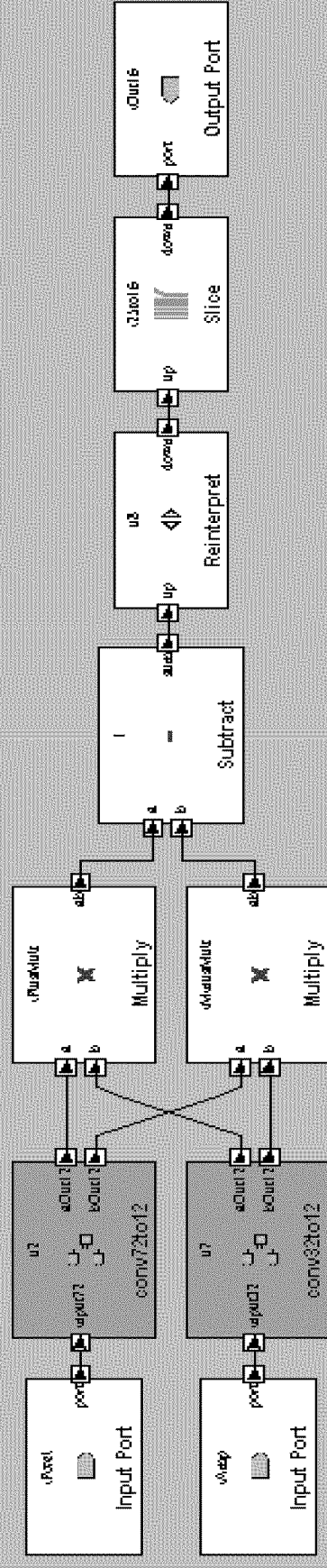


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FPGA Design Time: CoreFire™ vs. VHDL



ampCorrCombine Macro Amplitude Correction and I/Q Combine



PCS Testing: CoreFire Debugger

ESSEX

CoreFire™ Application Debugger includes windows for monitoring and manipulating data flow

CoreFire Debug - PeTarget.Pel

File View Options Help

Pass 1 Update none Step 10 Clear

Name	Value	Status	Pass	Ready	Enabled	Cycle	iDataPost..	iSInt	qDataPost..	qSInt	writeAddr...	iDirectFFT	iNegPre	qDirectFFT	qNegPre
iDataPosiFFT32	0	Invalid	0	true	☒	1	??	-2	??	0	0	??	??	??	??
iSInt	-3	Valid	0	true	☒	2	??	2	??	-1	1	??	-2	??	0
qDataPosiFFT32	0	Invalid	0	true	☒	3	??	-1	??	3	2	??	-2	??	1
qSInt	-2	Valid	0	true	☒	4	??	-2	??	-5	3	??	-1	??	3
writeAddress	16	Invalid	0	true	☒	5	??	8	??	4	4	??	2	??	5
iDirectFFT	0	Invalid	0	true	☒	6	??	-4	??	2	5	??	8	??	4
iNegPre	5	Valid	0	true	☒	7	??	-2	??	0	6	??	4	??	-2
qDirectFFT	0	Invalid	0	true	☒	8	??	0	??	0	7	??	-2	??	0
qNegPre	4	Valid	0	true	☒	9	??	-2	??	-4	8	??	0	??	0
						10	??	0	??	-2	9	??	-2	??	-4
						11	??	2	??	1	10	??	0	??	2
						12	??	2	??	-4	11	??	2	??	1
						13	??	1	??	7	12	??	-2	??	4
						14	??	28	??	-5	13	??	1	??	7
						15	??	2	??	0	14	??	0	??	5
						16	??	-3	??	6	15	??	2	??	4
						17	??	-5	??	-7	16	??	3	??	-6

10:20 AM PE Reset Total 30 Cycle 20

PeTarget.Pel - Register Viewer

Help

Update single

numPix LAD 1038 (0x00000040e)
0 Read 255 Again

numPix_div_by2 LAD 1028 (0x000000404)
0 Read 127 Again

iData - Memory Viewer 32 bits

File Set Help

Address 0 Dwords 0 Format Single

Address	0	1	2	3
0	196606	-65537	-262136	65534
4	65534	131074	1	-196606
8	131067	-196603	-65533	131070
12	-131072	-65529	0	524284
16	393211	-327683	-196599	196607
20	65534	-131068	-327680	6
24	-131074	327683	-131074	393216
28	655349	65535	65537	262140
32	196607	599817	-65536	65538
36	-131075	-131068	-65536	-327674
40	-458747	327680	262142	-65536
44	65535	-65533	0	-458748
48	-262135	-65535	65537	65532

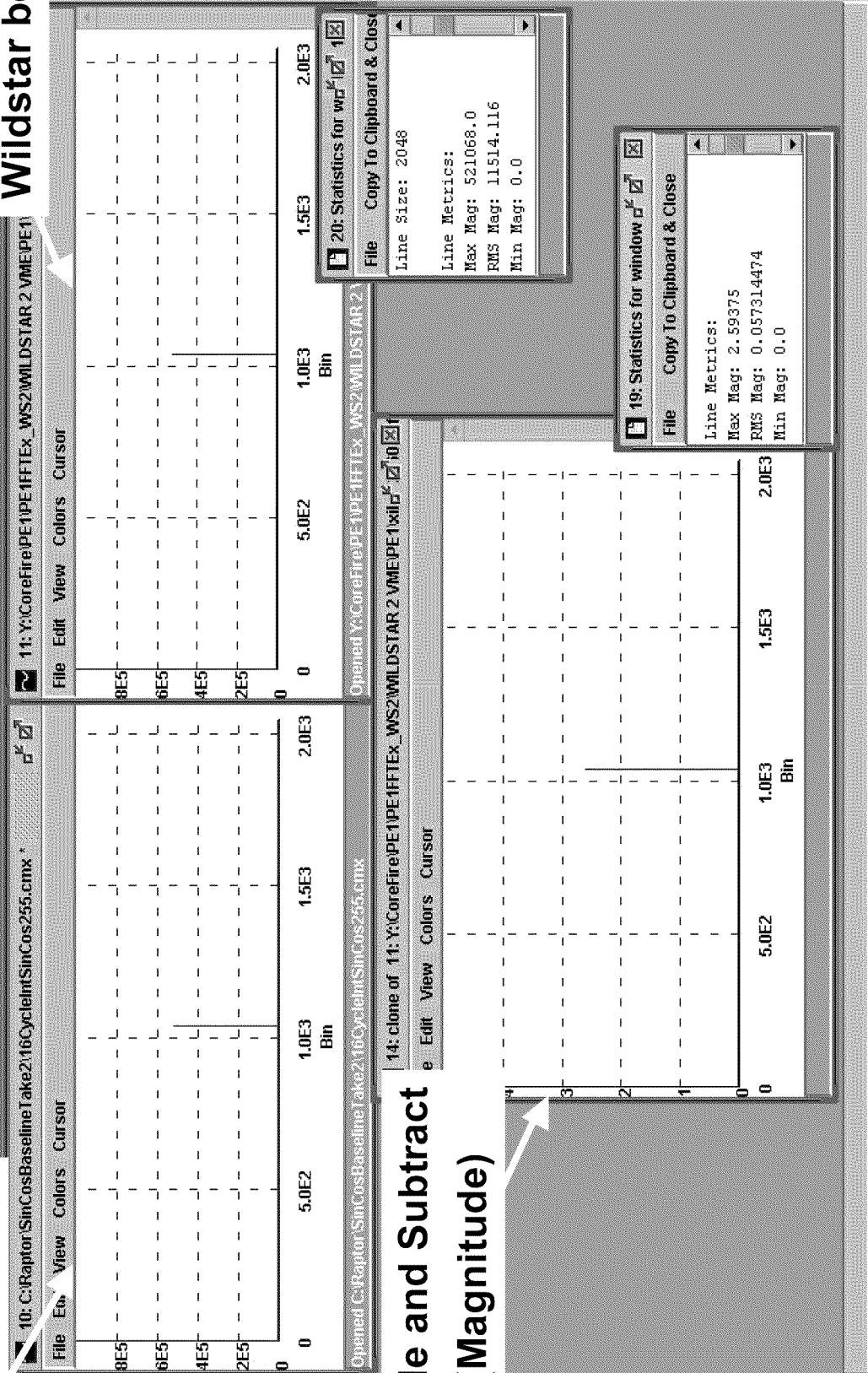
View 0(0x0) for 128 DWORDS.

Wildstar II FFT Example

ESSEX

FFT done in SW

FFT done on
Wildstar board



Scale and Subtract
(Magnitude)

Peak to RMS = 139 dB

- Essex has been able to implement an extremely complex, computationally intensive radar processing task in:
 - Embedded optical hardware and
 - Embedded DSP/FPGA hardware
- This approach saves space, development time, software, development costs and maintenance costs.
- The AOP hardware allows the use of new arbitrary classes of waveforms for improved ballistic missile discrimination.

ESSEX

Wrap-up / Questions