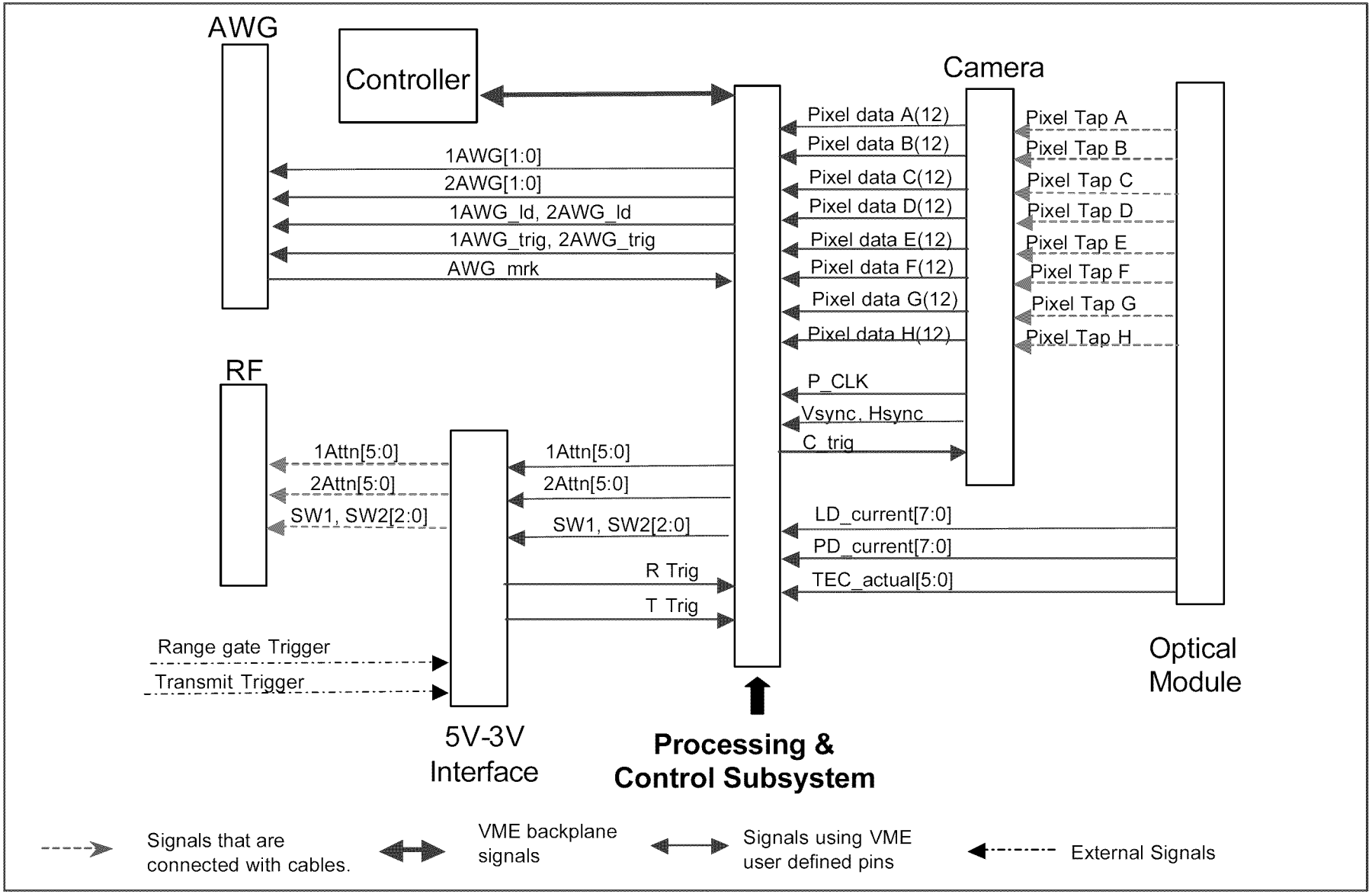
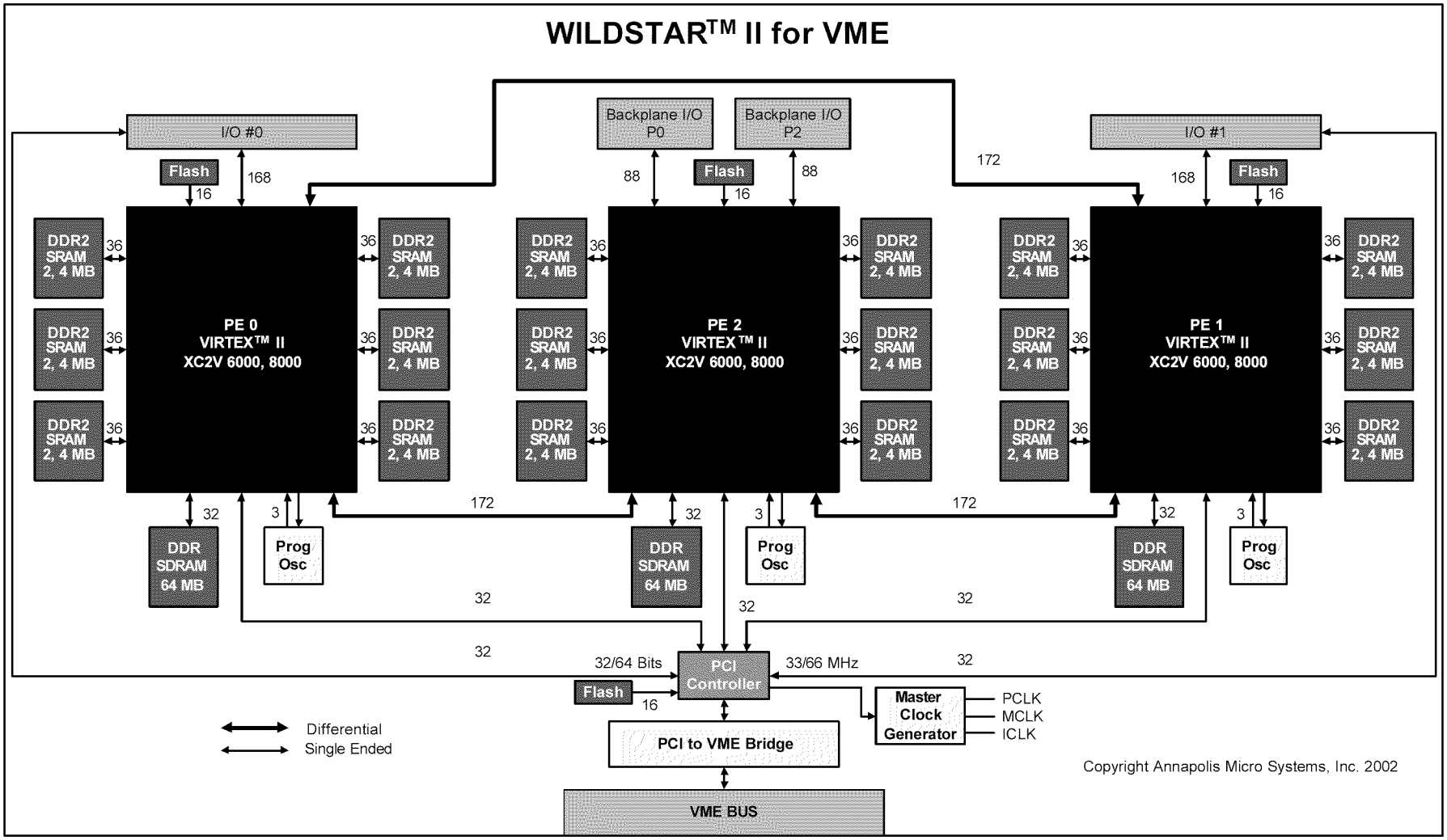
PCS External Interfaces



FPGA based reconfigurable computing board



WILDSTAR™ II for VME & Fibre Channel 2 I/O Card

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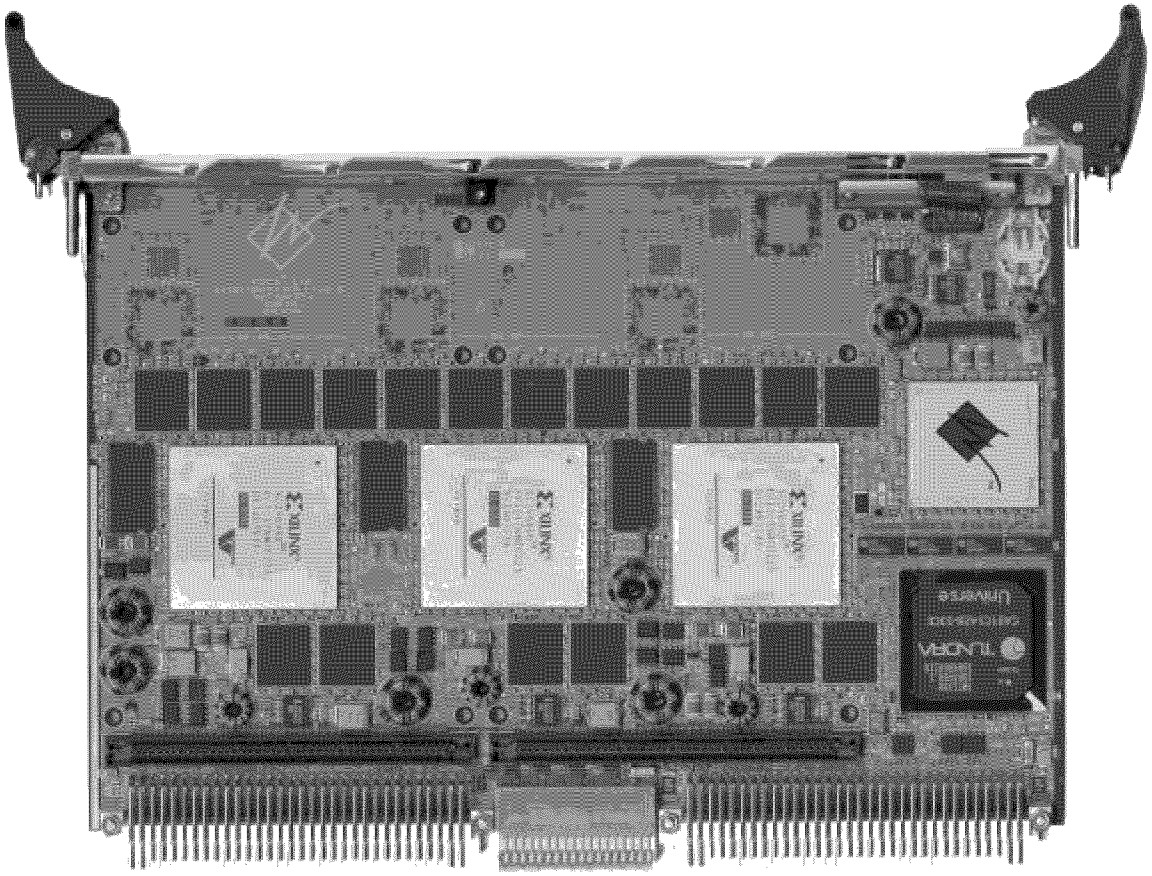

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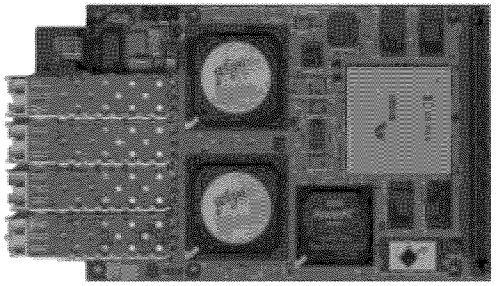
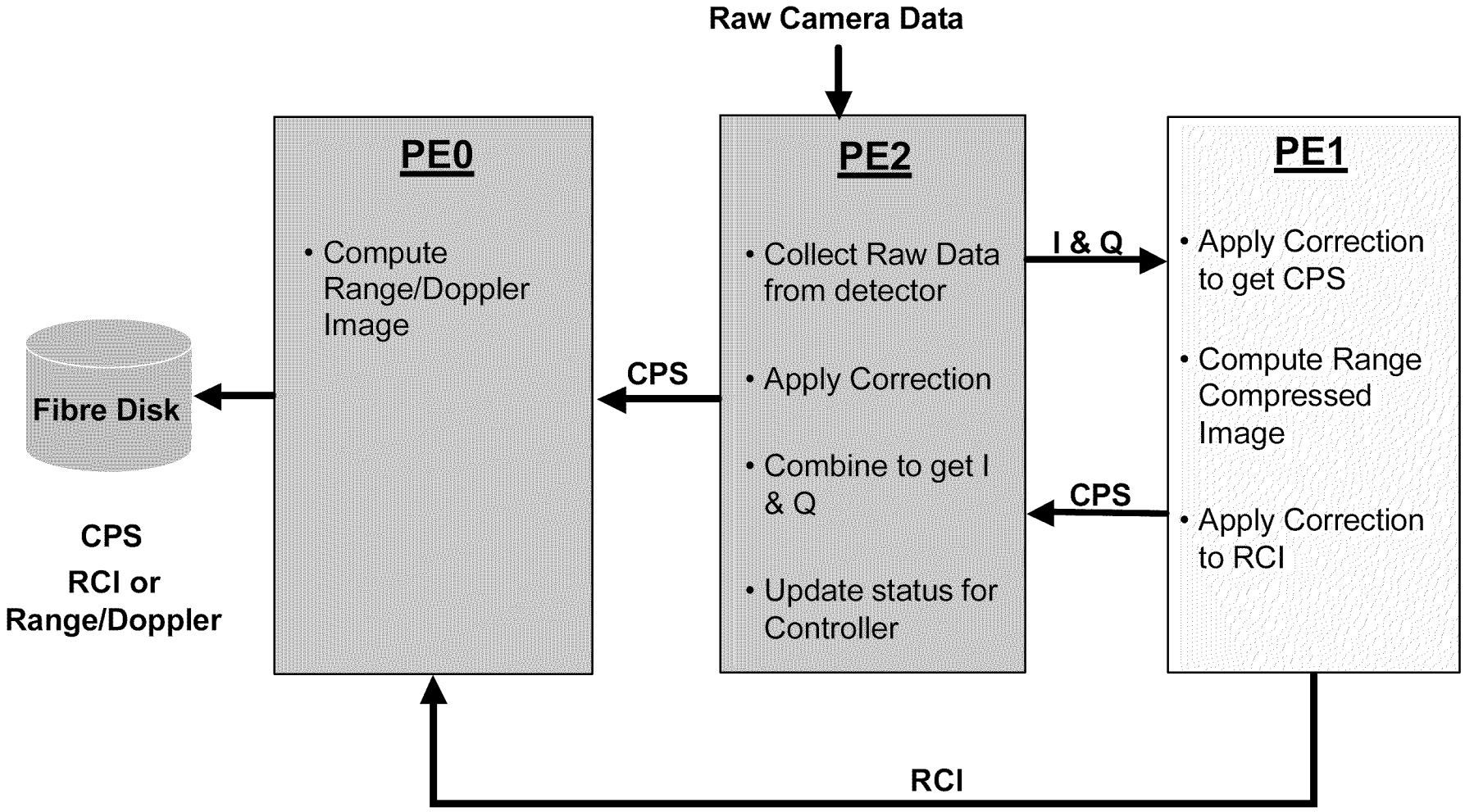


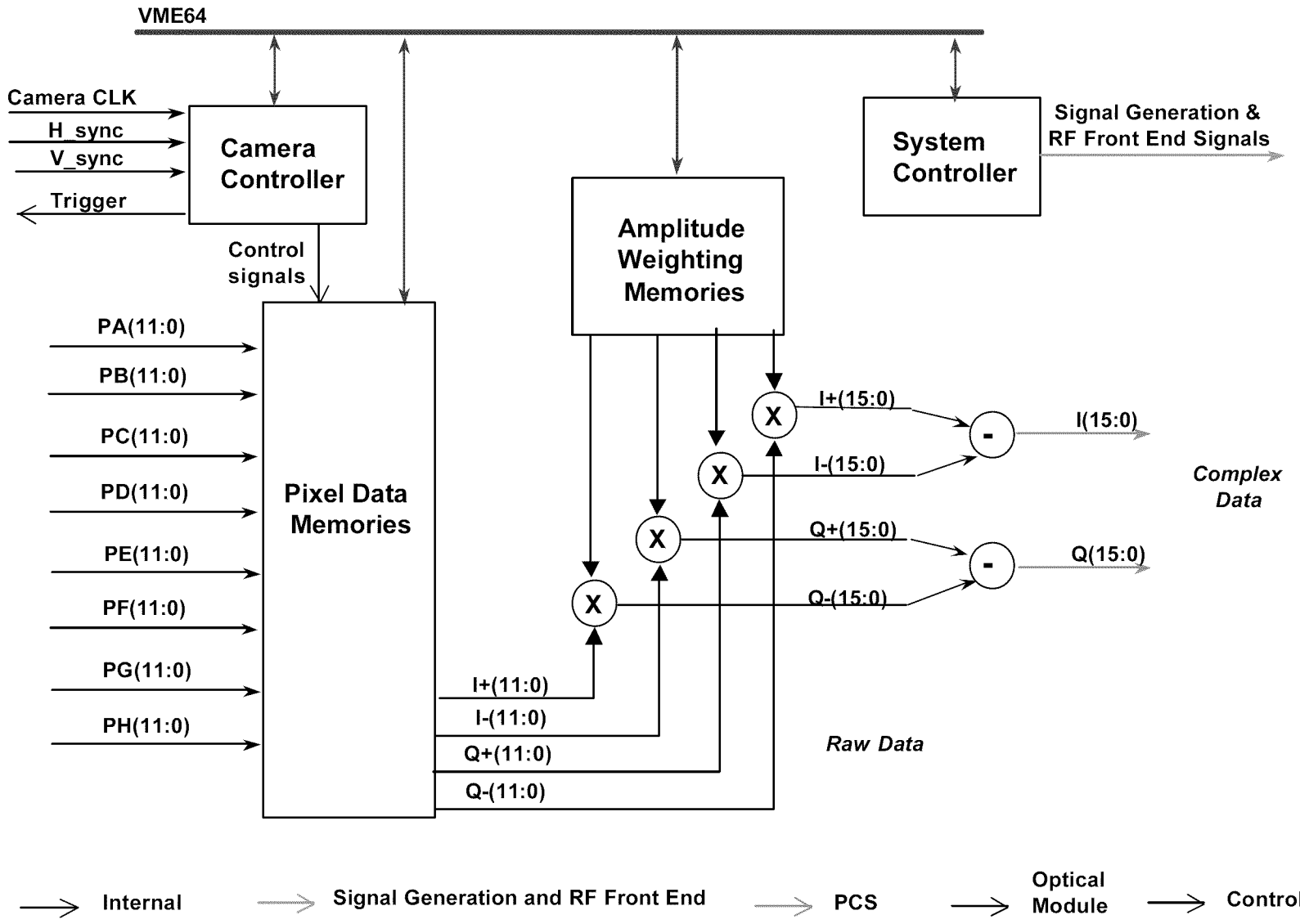
WILDSTAR™ II FPGA card

Fibre Channel 2 I/O Card daughter card

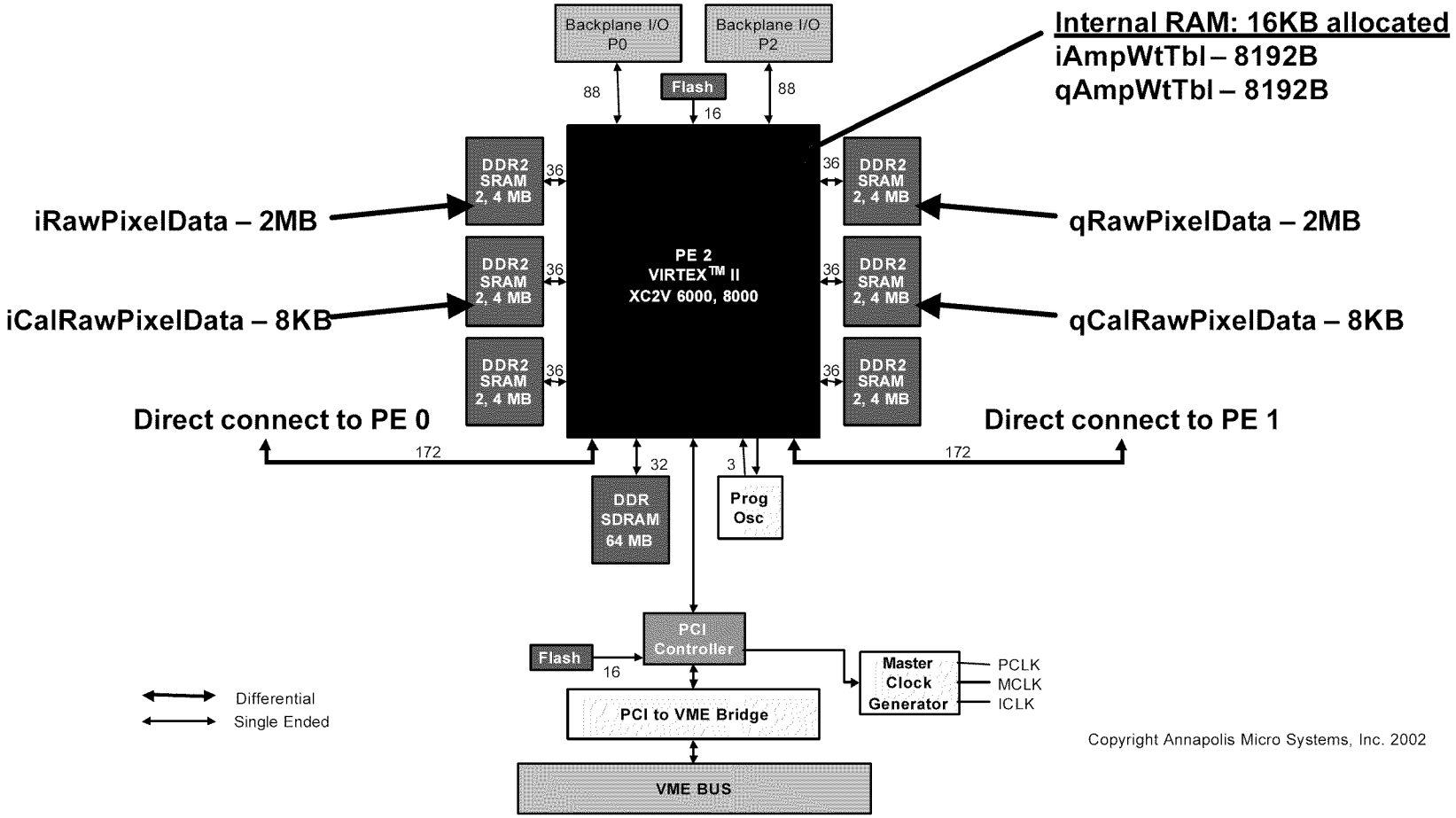
Internal PCS Interfaces



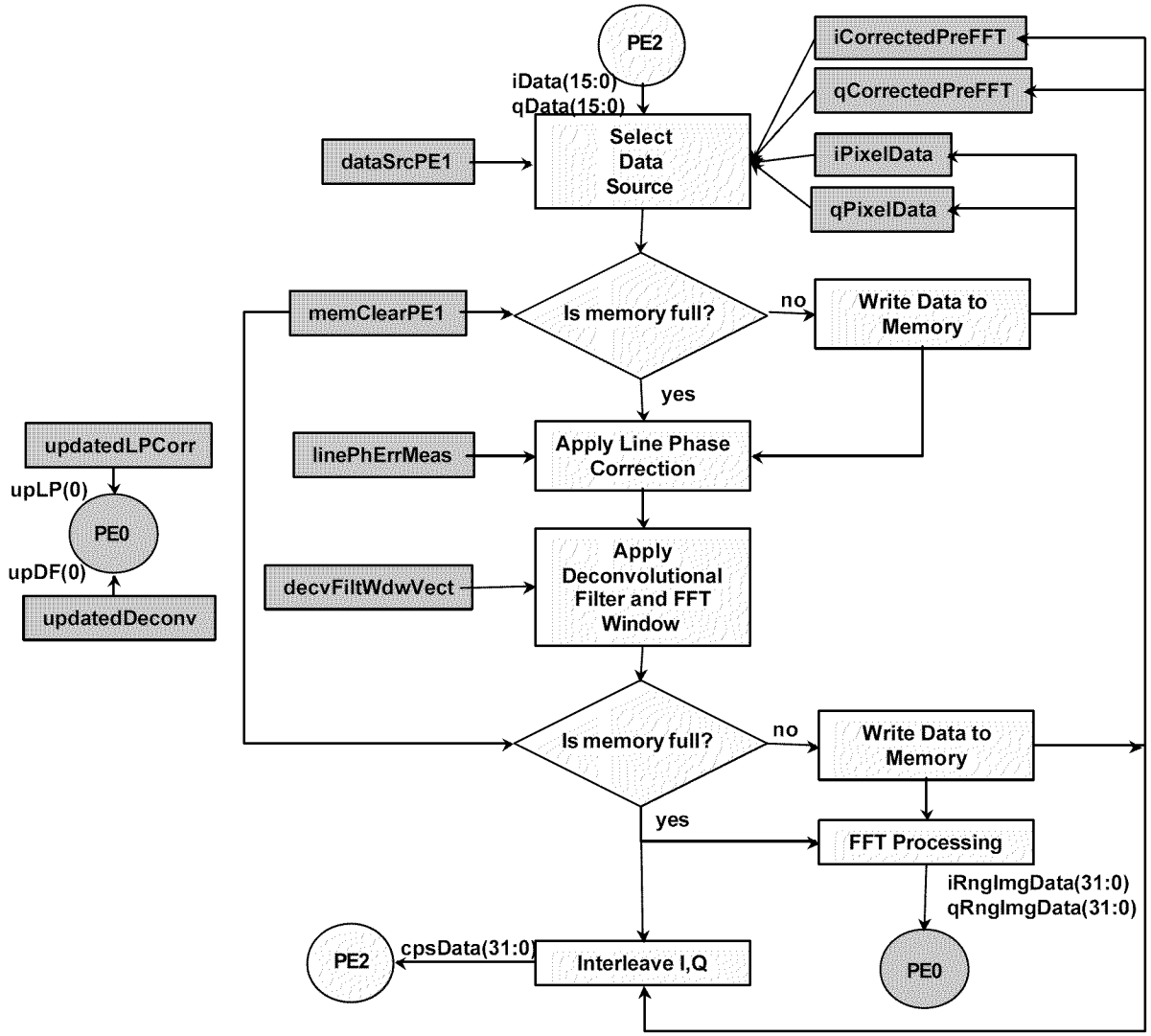
PE2 Data Processing



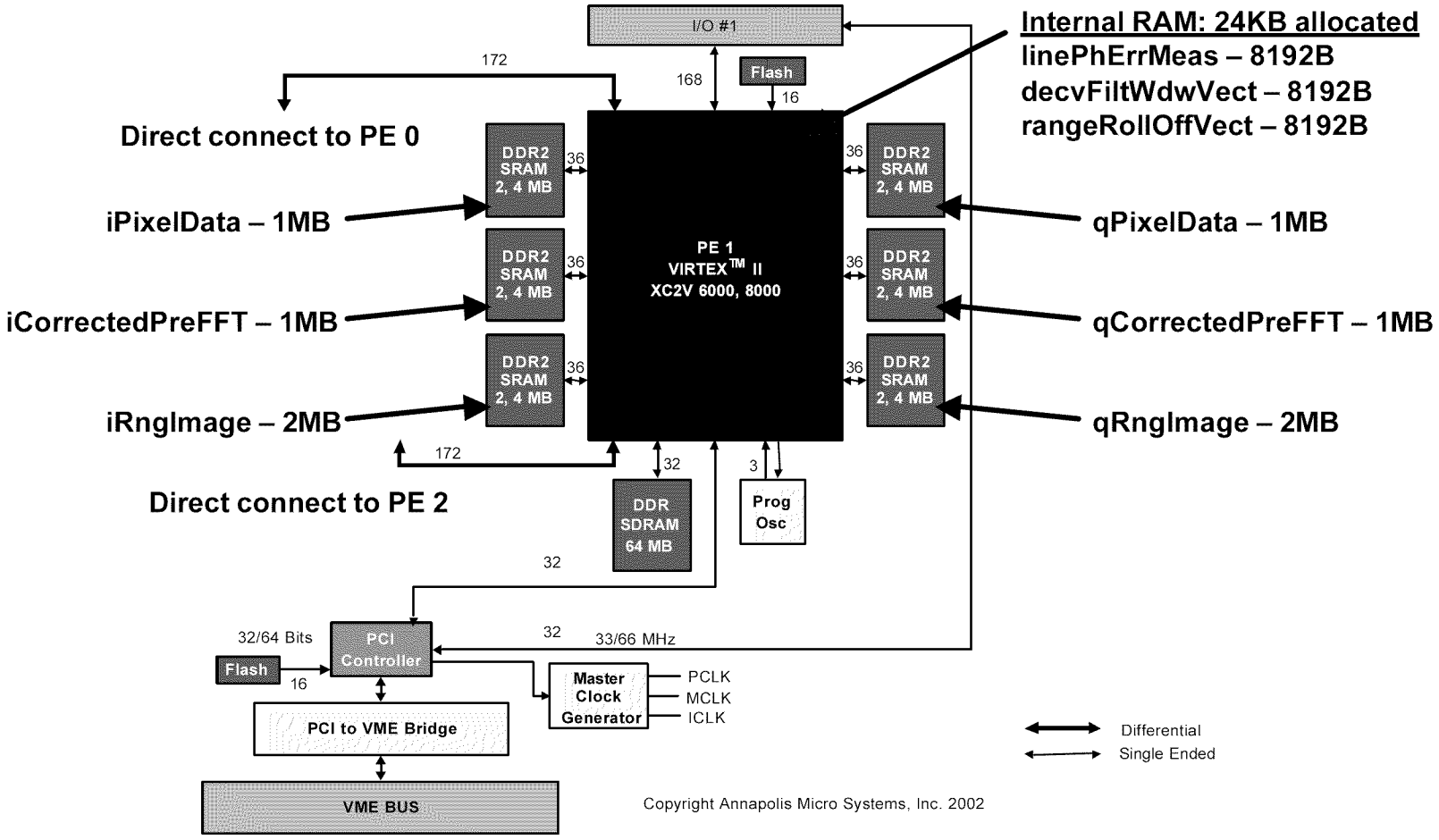
PE2 Allocated Memory Diagram



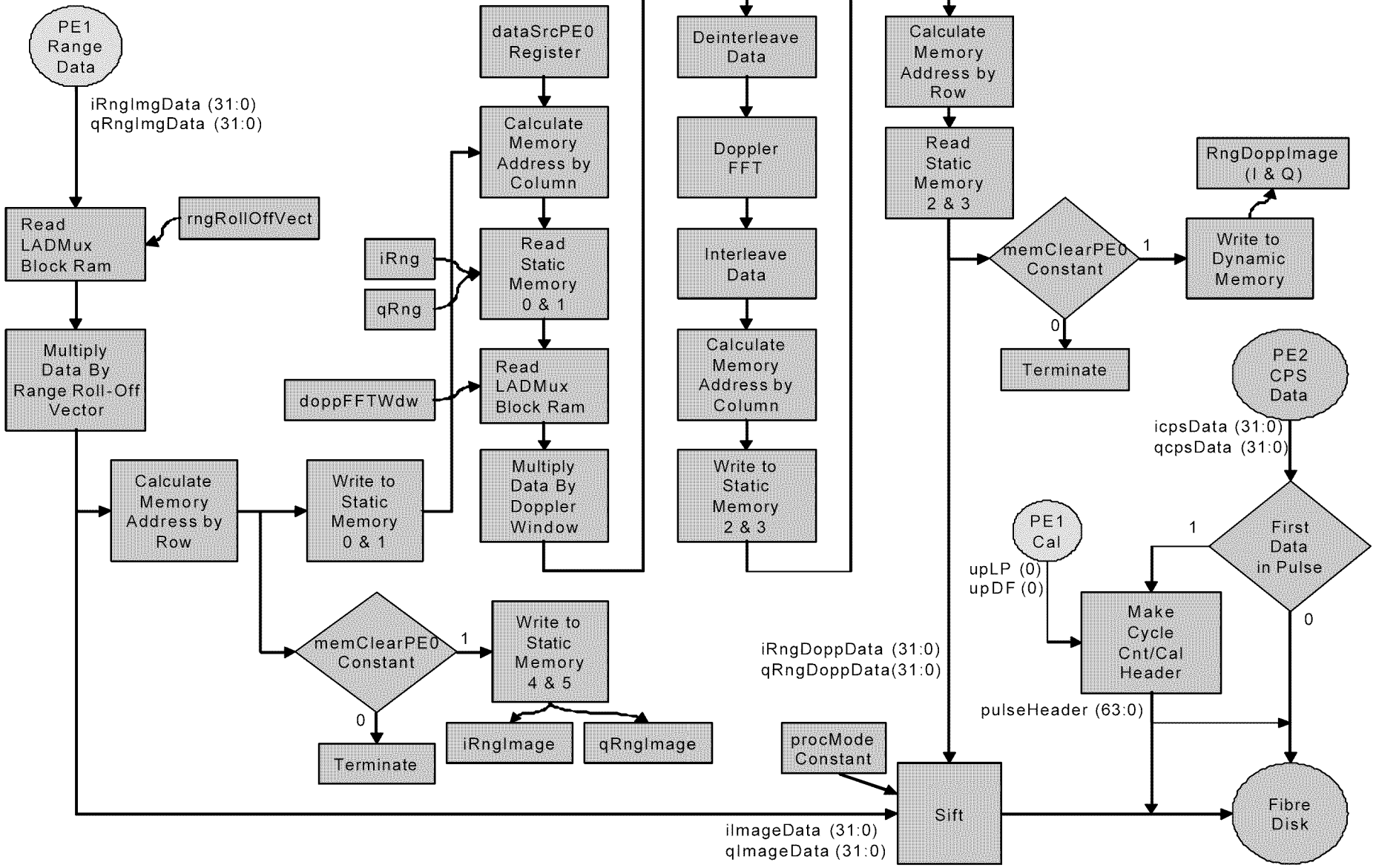
PE1 Functional Flow Diagram



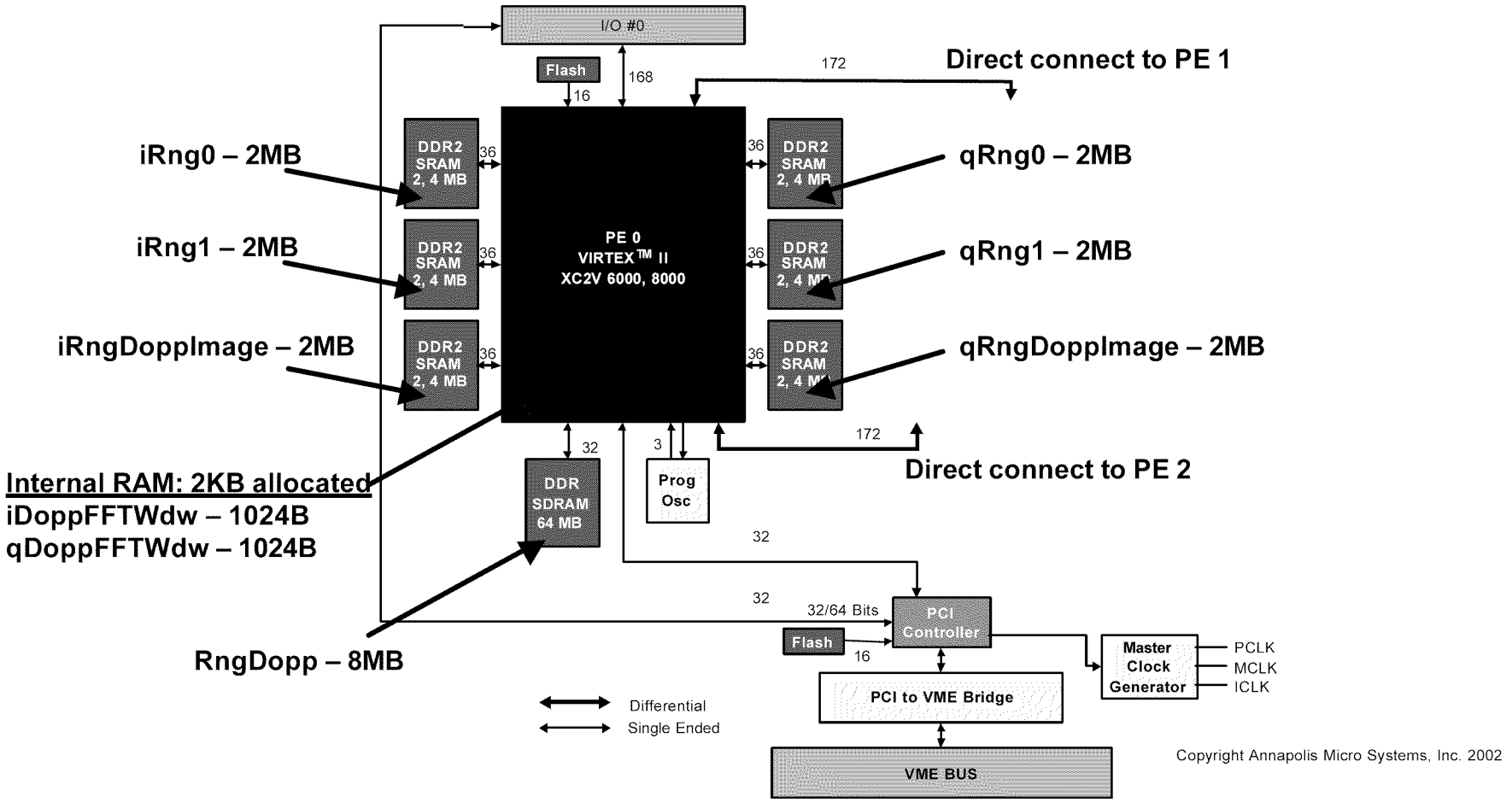
PE1 Allocated Memory Diagram



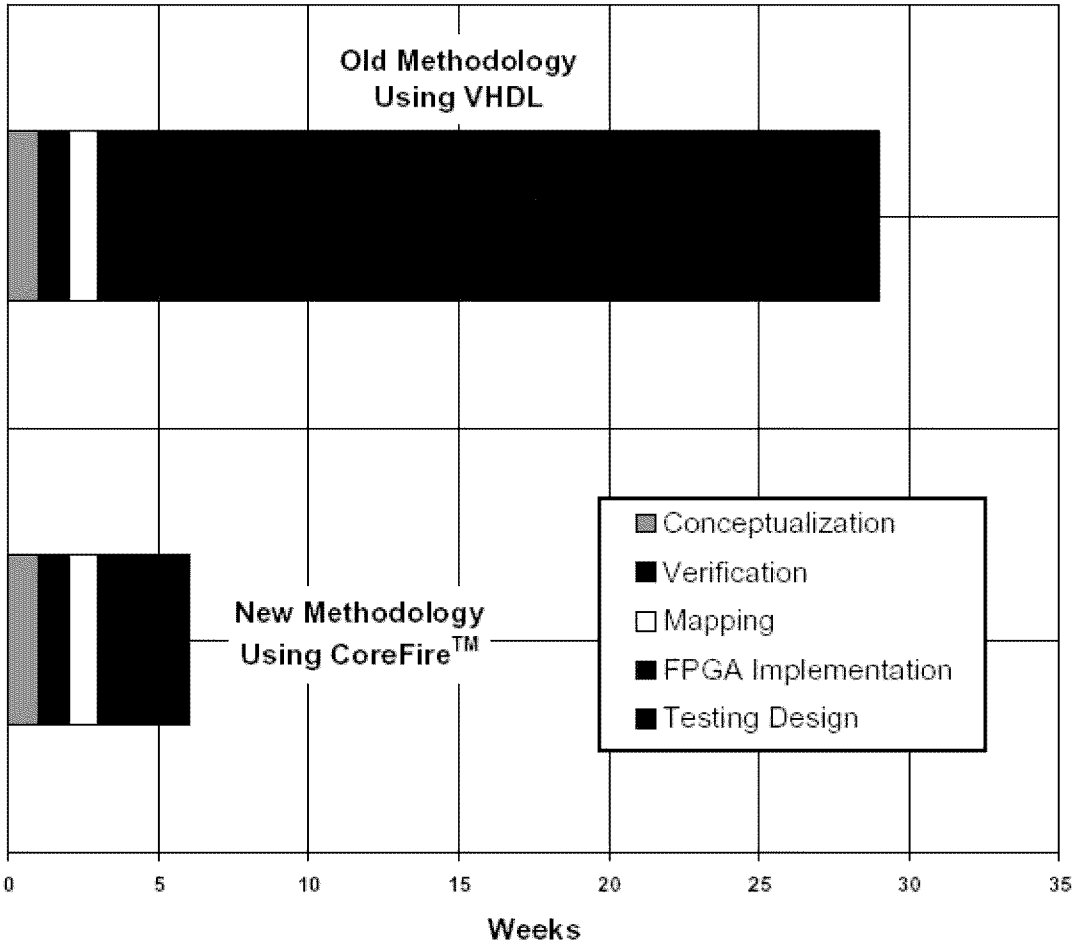
PE0 Functional Diagram



PE0 Allocated Memory Diagram



FPGA Design Time: CoreFire™ vs. VHDL



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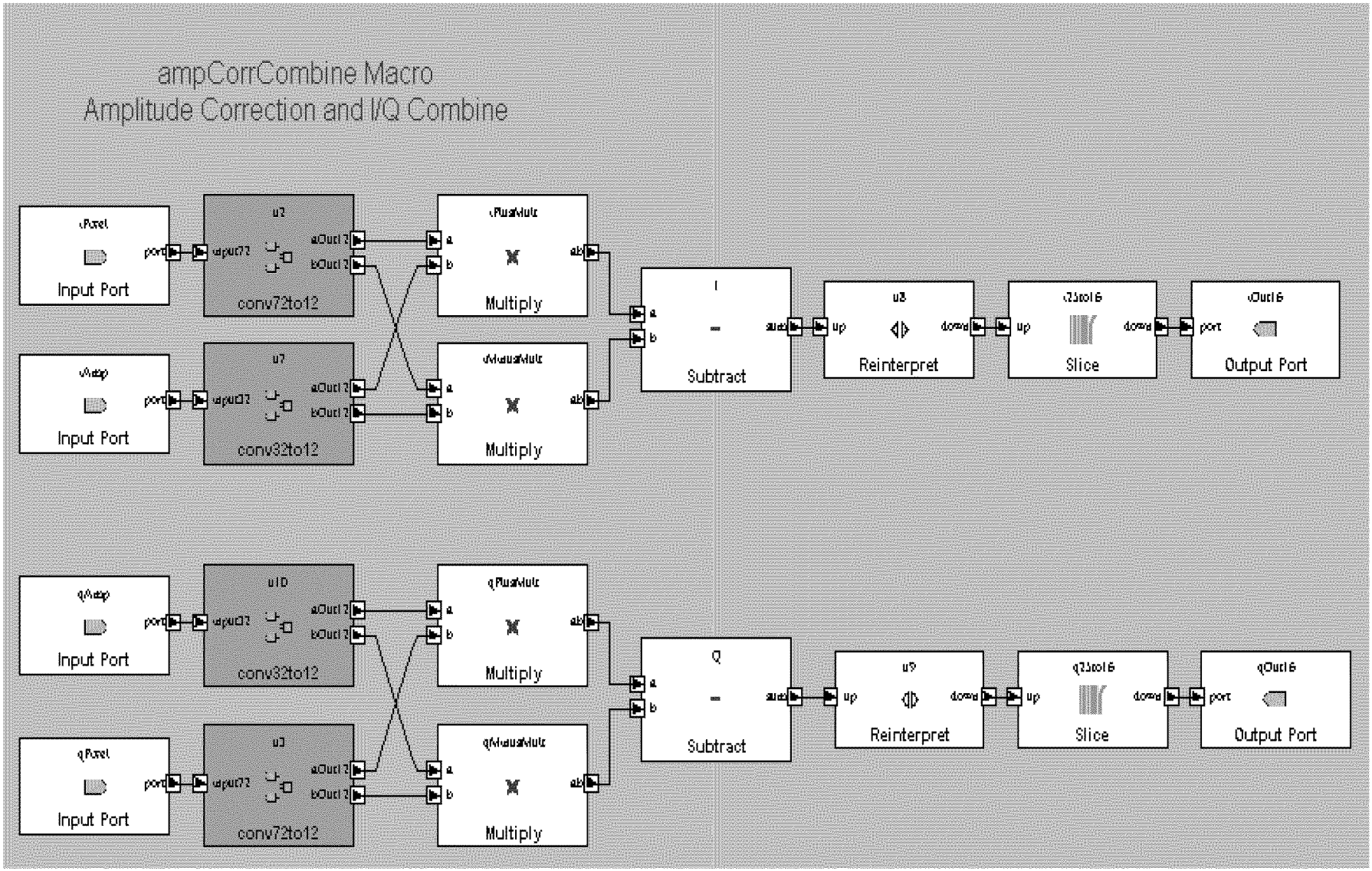
Corefire Example



PCS Testing: CoreFire Debugger

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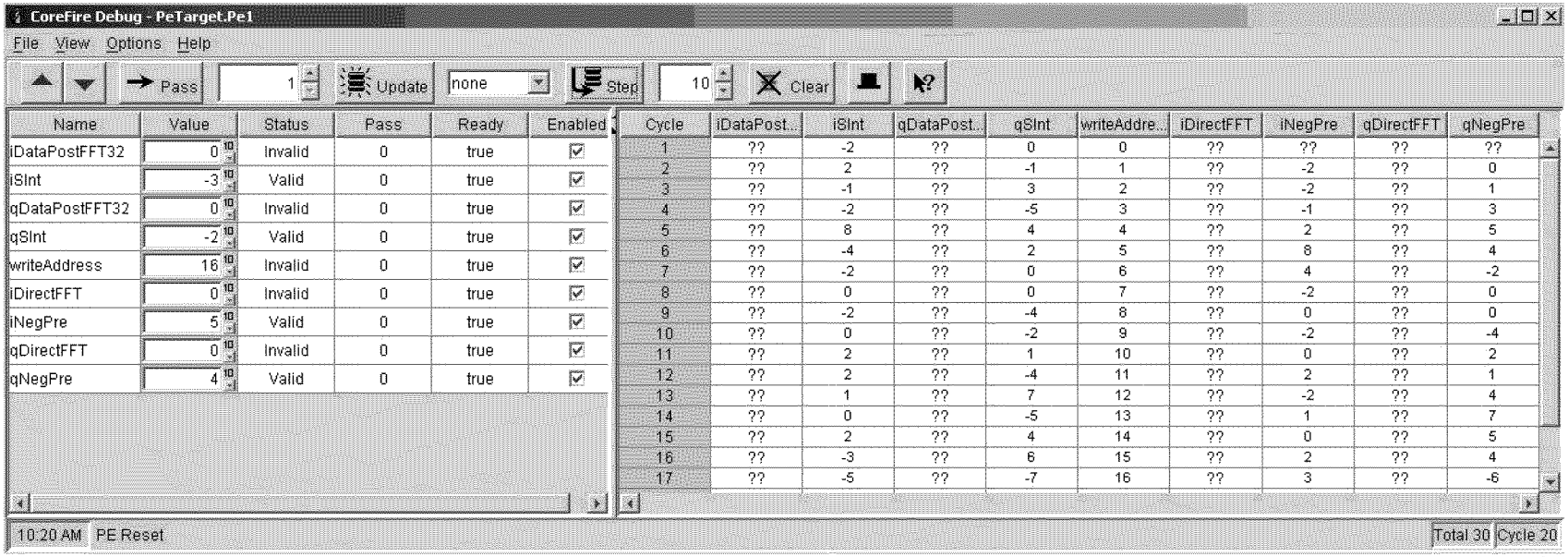
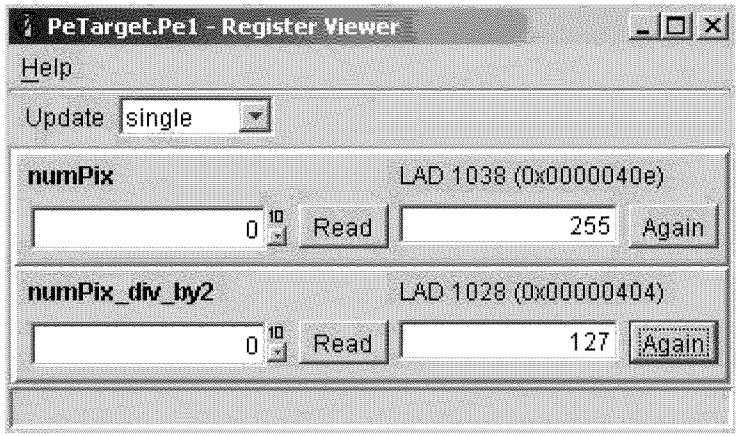
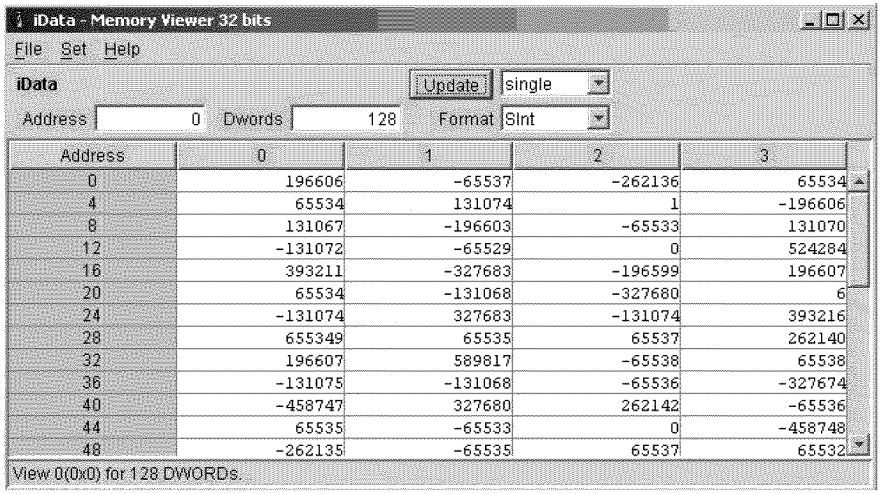
CoreFire™ Application Debugger includes windows for monitoring and manipulating data flow







Wildstar II FFT Example

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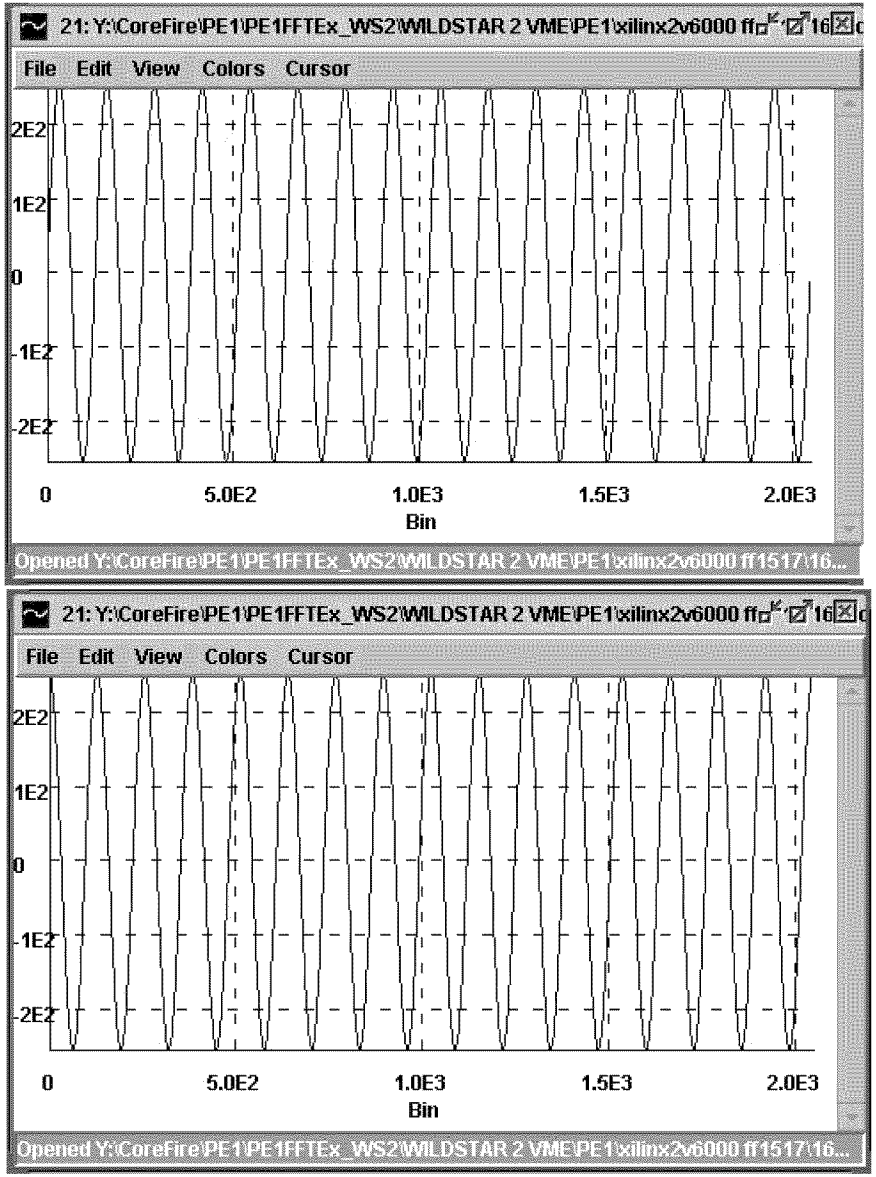
FFT Example Scenario

- CoreFire project for PE1
  - Data read from memory on Wildstar II board
  - FFT operation
  - Data written to memory on Wildstar II board
- Java program
  - Data read from file
  - Data written to memory on Wildstar II board
  - Data read from memory on Wildstar II board
  - Data written to file
- CoreFire Debugger
  - Kicks off the Wildstar II board processing
  - Memory and register viewers show data during the processing
- IView Tool
  - Compare output data file with expected results



Wildstar II FFT Example

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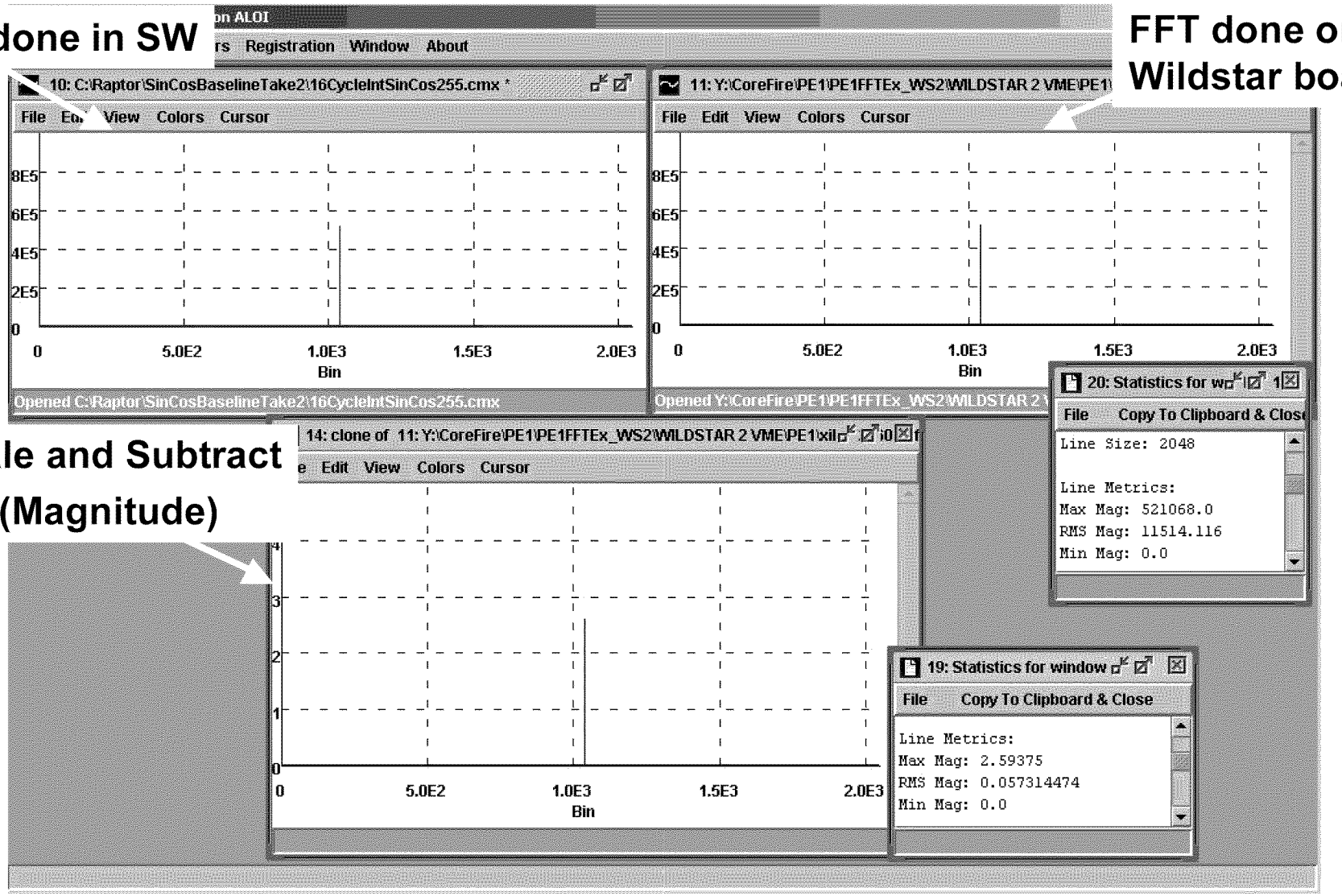
FFT done in SW

FFT done on Wildstar board



Scale and Subtract (Magnitude)

Peak to RMS = 139 dB

Conclusions

ESSEX

- **Essex has been able to implement an extremely complex, computationally intensive radar processing task in:**
  - **Embedded optical hardware and**
  - **Embedded DSP/FPGA hardware**

- **This approach saves space, development time, software, development costs and maintenance costs.**

- **The AOP hardware allows the use of new arbitrary classes of waveforms for improved ballistic missile discrimination.**

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Wrap-up / Questions