The growth of gallium arsenide on Si(100) by molecular-beam epitaxy[1]

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The growth of GaAs on Si(100) directly and with Ge buffer layers has been carried out sequentially under ultra high vacuum conditions in a double-ended III–V and group IV molecular beam epitaxy system. These heterostructures were examined by cross-section transverse emission microscopy, Rutherford backscattering, X-ray diffraction, and photoluminescence spectroscopy.

Dislocation densities were observed to be high ($\geq 10^9$ cm^{-2}) near both the GaAs–Si and the Ge–Si interfaces and to decrease to $\sim 5 \times 10^8$ cm^{-2} a few micrometres from these interfaces. No dislocations were observed to originate at the GaAs–Ge interface, but the threading dislocations existing in the Ge buffer layer were found to propagate across this interface without significant deviation. The crystalline quality of the GaAs grown on Ge buffer layers was comparable with that grown on Si directly. However, GaAs has not yet been grown on the highest quality Ge buffer layers obtainable.

La croissance de GaAs sur Si (100), directement et avec des couches tampons de Ge, a été effectuée de façon séquentielle sous des conditions d'ultravide dans un système double, III–V et groupe IV, d'épitaxie à jets moléculaires. Ces hétérostructures ont été examinées par microscopie électronique en transmission des sections transversales, par diffusion Rutherford, par diffraction des rayons X et par spectroscopie de photoluminescence.

On a observé que les densités de dislocations étaient élevées ($\geq 10^9$ cm^{-2}) au voisinage des deux interfaces, GaAs–Si et Ge–Si, et qu'elles diminuaient à environ 5×10^8 cm^{-2} à quelques micromètres de ces interfaces. On n'a pas observé de dislocations originant à l'interface GaAs–Ge, mais on a trouvé que les dislocations vis existant dans la couche tampon de Ge se propagent à travers cette interface sans déviation appréciable. La qualité cristalline que GaAs obtenu par croissance sur des couches tampons de Ge était comparable à celle qu'on obtient par croissance directement sur Si. On a toutefois pas encore réalisé la croissance de GaAs sur des couches tampons de la plus haute qualité disponible.

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1. Introduction

In recent years, an icnreasing number of molecular-beam epitaxy (MBE) groups have attempted to grow device-quality GaAs epilayers on Si substrates (1–3). The incentives to produce such material are easily understood: advantage could then be taken of the superior speed, lower switching power, and opto-electronic properties of GaAs while retaining the lower cost, higher mechanical strength, and larger available diameter of Si substrates. Hybrid integrated circuits might also become feasible, with GaAs circuits fabricated on epilayers grown on selected areas of very large scale integration (VLSI) Si chips.

In spite of the 4.1% lattice mismatch between Si and GaAs, GaAs on silicon metal oxide semiconductor field-effect transistors (MESFET) and light-emitting diodes (LED) have been fabricated with good device characteristics (4, 5). However, lasers fabricated with this material have not been capable of continuous-wave (CW) operation at room temprature, although pulsed operation has been reported (6). This indicates that the quality of GaAs grown on silicon substrates is still inferior to that grown directly on a GaAs wafer. Further efforts to optimize the conditions of growth of the GaAs epilayers on Si are still being made in many laboratories.

One method being used to improve the GaAs quality is the deposition of a Ge buffer layer on the Si wafer before the GaAs growth, either by MBE (6) or chemical vapour deposition (CVD) (7). Ge buffer layers have potential advantages, because Ge has an excellent lattice match to GaAs and it alloys with Si over the whole range of concentration. This makes it possible to study graded SiGe layers and to separate polar–nonpolar interface effects from lattice mismatch effects.

Other methods of improving the GaAs quality have included using wafers cut a few degrees off the (100) orientation (1, 2) and using strained-layer superlattices to reduce the number of threading dislocations (1, 8).

At the Microstructural Sciences Laboratory at the National Research Council of Canada, we have brought into operation over the past year an MBE machine that has some properties well suited to the study of this GaAs–Si growth. It has two growth chambers; one equipped to produce Si, Ge and SiGe alloy films; and the other, GaAs, GaAlAs, and GaInAs. The chambers are interconnected via their respective preparation chambers, so that 3 in. (1 in. = 2.54 cm) diameter substrates can be transported between them in ultra high vacuums (uhv). High-temperature heating stages in the Si growth and preparation chambers allow substrates to be heated to 1150°C, a capability useful for the cleaning of Si substrates and one not usually available in conventional GaAs MBE machines. In this paper, we report on our first experiments aimed at optimizing the parameters for the growth of GaAs on Si and on Ge buffer layers on Si.

It is often difficult to compare the quality of GaAs on silicon material presented in the literature, because a report usually includes only one or two methods of material analysis. We will

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give the results of four characterization techniques and discuss how they compare with each other.

2. Experimental

2.1. Layer growth

Three inch (7.62 cm) diameter Si(100) wafers were individually treated in an ultraviolet ozone reactor for 3000 s to remove hydrocarbon contamination and then inserted promptly into the entry lock of the Si chamber. The resulting oxide, ~2 nm thick[2], was removed in the Si growth stage by heating first to 950°C for 10 min and then to 900°C for a further 10 min in the presence of a small Si flux (≤ 0.01 nm·s^{-1}). Ge buffer layers, when used, were grown at 500–600°C at a growth rate of ~0.5 nm·s^{-1} to a total thickness of ~1 μm.

The wafer heating power was then gradually reduced to avoid thermal slip. Transfer to the GaAs chamber was initiated as soon as the wafer temperature fell below 350°C. The transfer procedure required 5–10 min. The pressure in the chambers during this period was $2-5 \times 10^{-10}$ Torr, mostly due to H_2 (1 Torr = 133 Pa).

In a simulation of this growth interruption, a Si epilayer was grown on a Si surface after a 30 min period at $T \leq 150$°C. No evidence of growth anomalies were observed at the interruption interface.

In the GaAs chamber, the wafer was heated to 600°C to remove adsorbed gases. For direct growth on Si, it was then cooled to ≤300°C and about 10 nm of GaAs was deposited (9). Subsequently, growth was at 500–600°C and consisted of a 100–200 nm buffer, a superlattice of 5–10 periods of 6 nm AlAs and 6 nm of GaAs, and finally the GaAs layer, 1–2 μm thick. The growth rate was ~0.2 nm·s^{-1} using As_4.

2.2. Characterization techniques

Cross-section transmission electron microscopy (XTEM) was used as a means of investigating the nature and distribution of defects in the epitaxial films. The samples were prepared by mechanical dimpling and fast atom beam milling. They were examined in a Philips EM400 microscope operating at 120 kV.

The Rutherford backscattering (RBS) channeling measurements were made using a 1.6 MeV $^4He^+$ beam.[3] The backscattered ions were detected at ~180° using a large annular surface-barrier detector. This allowed low fluences to be used, minimizing beam damage to the material. Channeled yield measurements were made with the incident beam aligned along the ⟨100⟩ axial channel normal to the surface. In selected cases, random orientation yields were measured by tilting a few degrees away from the normal and rotating the target to average over all azimuths.

X-ray diffraction measurements were carried out using a Philips 1820 single-crystal diffractometer with Cu Kα radiation.

The photoluminescence (PL) excitation source was a HeNe laser (633 nm). Detection was by the conventional phase-locked technique using a 0.5 m spectrometer and a Si photodiode. All spectra were obtained at 5 K. The excitation intensity was 200 W·cm^{-2}.

[2]The AES profiling was done by S. Ingrey, Bell Northern Research.

[3]The van der Graaf accelerator at the Physics Department, University of Guelph, Guelph, Ont., was used for the analyses.

TABLE 1. Epilayer parameters

Wafer number	Layers	Growth T (°C)	GaAs thickness (μm)
37	GaAs–Si	560 ± 25	3.0
61	GaAs–Si	560	1.5
62	GaAs–Ge–Si	560	1.5
64	GaAs–Si	560	1.1
66	GaAs–SL–Fe–Si	560	2.0
66E	Ge–Si	560	1.5 (Ge)
67	n-GaAs–Si	560	1.4

3. Results and discussion

A total of 10 GaAs layers were grown in the present series of experiments. The six on which data are presented are listed in Table 1. Layer no. 66E was obtained by etching the GaAs layer from no. 66 using a 5:1:1 mixture of H_2SO_4:H_2O_2:H_2O.

In most cases the GaAs surfaces showed fairly smooth and uniform morphology, as observed by optical microscopy at X1000, although features thought to be related to stacking faults could be seen. Thicker GaAs films grown on GaAs substrates in the same growth series showed p-type background doping at $\sim 1-2 \times 10^{15}$ cm^{-3}, identified by PL to be carbon.

Photoluminescence spectra are shown in Fig. 1 for material from wafers nos. 37 and 66. The main peaks are associated with bound excitons (1.505 eV) and the band-to-acceptor transition consistent with the carbon impurity (1.495 eV). Note that these energies are different from those reported by Fischer *et al.* (1). Layers grown at higher temperatures than that used for nos. 37 and 66 give energies in better agreement with these authors. The photoluminescence intensity is typically 50–100 times lower than that observed for GaAs grown on GaAs substrates. Nonradiative recombination at lattice dislocations is believed to be responsible for this decrease. The intensity and relative peak heights are both observed to vary considerably among the samples. No major significance is to be attached to the differences between the peak amplitudes in Figs. 1*a* and 1*b*.

A point worth noting is the absence of a peak corresponding to recombination involving a Ge acceptor. This is in contrast to the results reported by Fischer *et al.* (9), and can be attributed to the presence of the GaAs–AlAs superlattice close to the GaAs–Ge interface. Such superlattices are known to be effective in retarding surface-borne impurities such as carbon.

Single-crystal X-ray diffraction spectra of water no. 61 showed line broadening, indicative of a rather high average dislocation density. The mean density D of dislocations within the epilayer could be estimated from the FWHM of the (400) Bragg reflection β by using the expression $D = \beta^2/9b^2$, where b is the effective Burgers vector of the dislocation network (10). In the above case, this yielded a value of $\sim 10^9$ cm^{-2}. No comparable broadening was observed from nos. 37 or 66, which are believed to contain substantially fewer dislocations.

Figures 2 and 3 show [110] XTEM bright-field images from epilayers (epi) nos. 37 and 66, respectively. Figure 2 displays typical features observed in GaAs epilayers grown on nominal (100)Si (1). The dark contrast band at the interface arises from the misfit dislocation network due to the 4.1% lattice mismatch

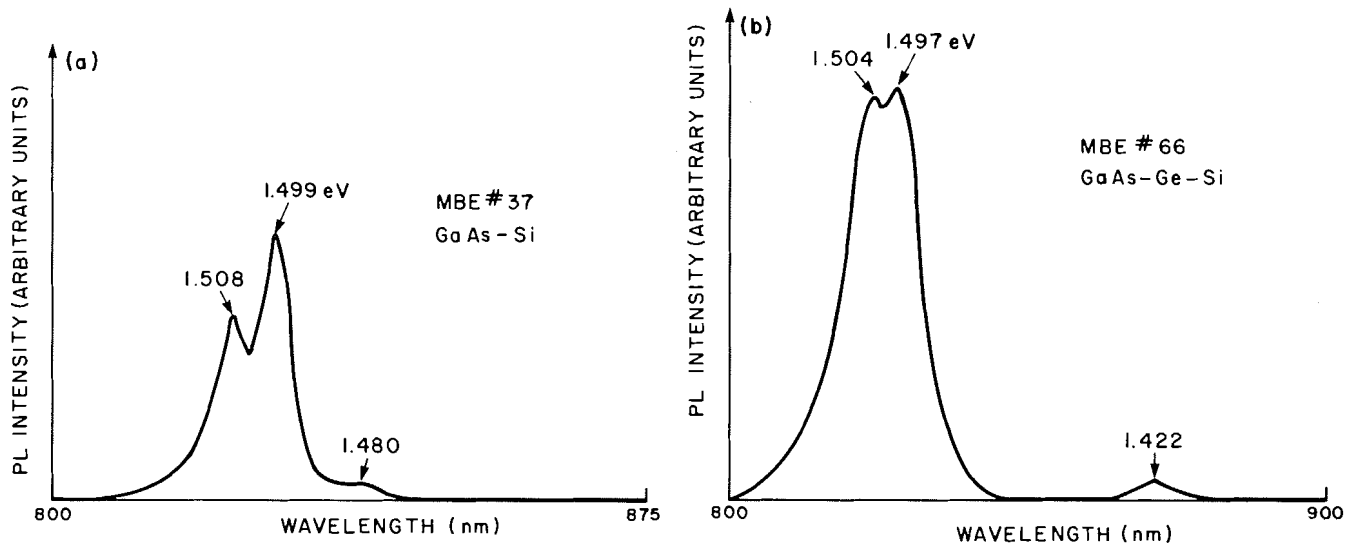

FIG. 1. (*a*) The PL spectrum at ~5 K for no. 37. The origin of the peak at 1.480 eV is unknown. (*b*) The PL spectrum at ~5 K for no. 66. Note the absence of a peak due to a Ge acceptor. The origin of the peak at 1.42 eV is unknown.

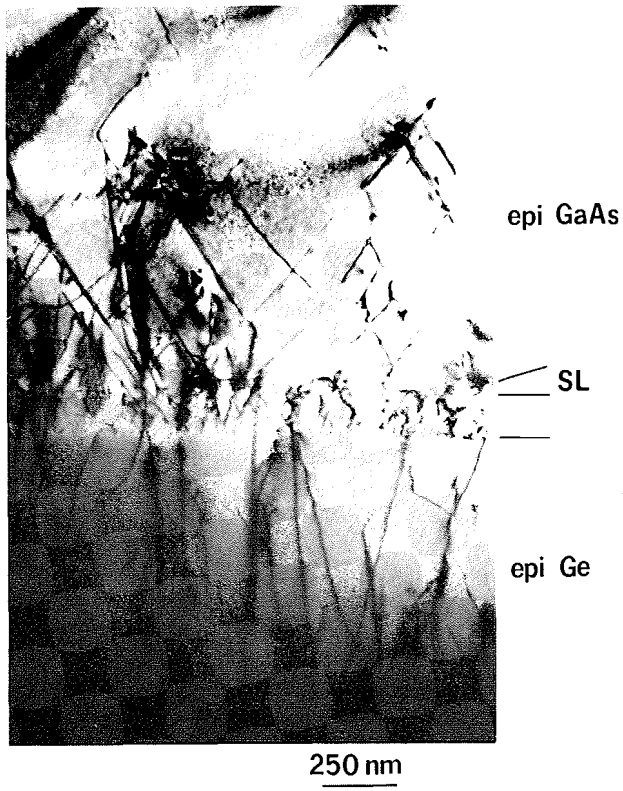

FIG. 2. An (110) XTEM micrograph of sample no. 66. The layer labelled SL is a six-period GaAs–AlAs superlattice.

between GaAs and Si. Stacking faults and threading dislocations are observed throughout the epilayer. The defect density is, however, reduced substantially away from the interface and is estimated to be $\sim 5 \times 10^8$ cm^{-2} at the surface. The result of introducing an intermediate Ge layer can be seen in Fig. 3. In the Ge epilayer, a high density ($\geq 10^9$ cm^{-2}) of threading dislocations originating at the Si–Ge interface propagates toward the surface. No stacking faults are seen in the Ge epilayer. Most of the threading dislocations propagate across the GaAs–Ge interface with little perturbation. This result

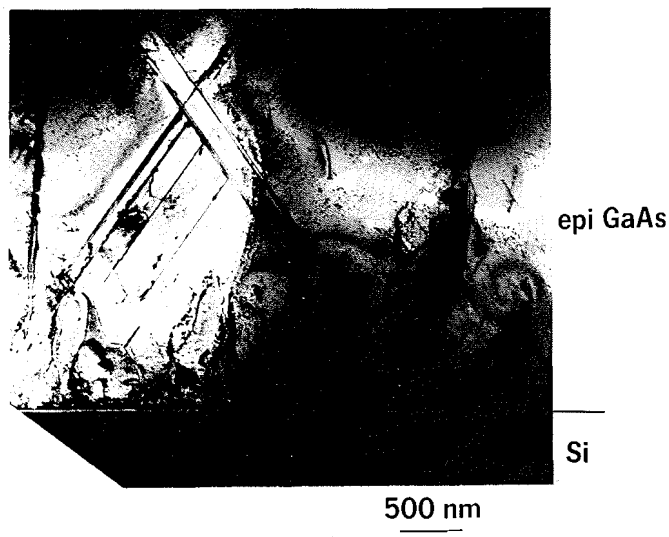

FIG. 3. An ⟨110⟩ XTEM micrograph of sample no. 37.

suggests that there is little strain at this interface. The overall crystalline quality of the GaAs epilayer is comparable for the two samples.

Figures 4–6 illustrate the RBS channeling data obtained from some of the samples examined with other techniques. Curve (a) in all three figures is the backscattering spectrum obtained from a 3.5 μm thick GaAs epilayer deposited on a (100)GaAs substrate. This sample (no. 30) exhibits a significantly lower dechanneling rate than any of the GaAs or Ge layers deposited on the Si substrates. The χ_{min} (the ratio of channeled yield to random yield measured in the near-surface region) is 4.0%, which is very close to that expected for a perfect GaAs crystal under these experimental conditions. This spectrum is, therefore, a reasonable benchmark.

In Fig. 4, spectra from three samples where the GaAs was deposited directly onto the silicon substrate are compared with the reference spectrum. Curves (c) (sample no. 61) and (d) (sample no. 64) not only have a much larger dechanneling rate but χ_{min} is ~6.5% in both cases. This increase is due to both

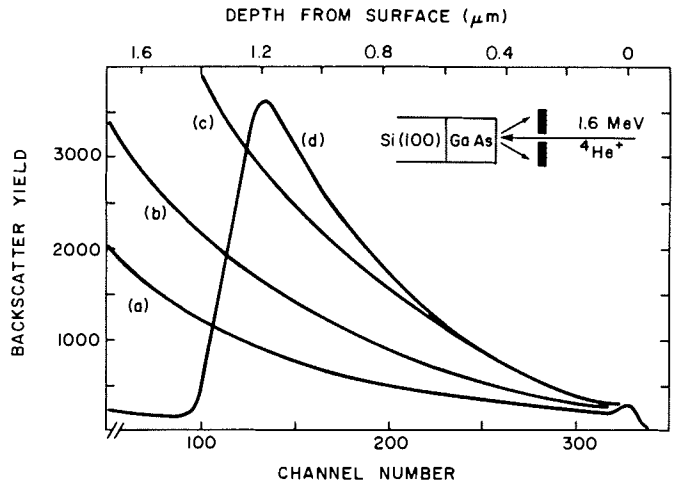

FIG. 4. A 180° Rutherford backscattering spectra of 1.6 MeV $^4He^+$ incident along the normal ⟨110⟩ direction of different epilayers. The spectra illustrate the different dechanneling rates observed for different defect densities. The epilayers are as follows: (a) 3.5 μm epilayer of GaAs on GaAs(100), (b) epilayer no. 66., (c) epilayer no. 61, and (d) epilayer no. 64.

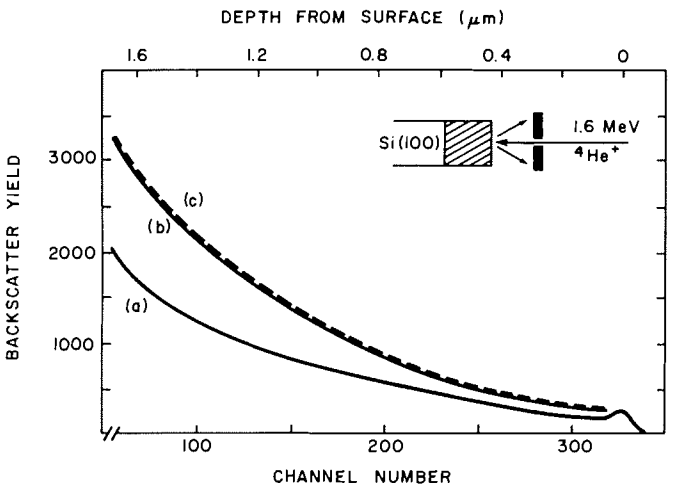

FIG. 5. A 180° Rutherford backscattering spectra of 1.6 MeV He^+ incident along the normal ⟨100⟩ direction of different epilayers are as follows: (a) 3.5 μm epilayer of GaAs on GaAs(100), (b) epilayer no. 66, and (c) epilayer no. 37. Note the GaAs epilayers grown on a buffer Ge epilayer and directly onto the Si(100) substrate give the same dechanneling rate.

stacking faults and dislocations. The rapid increase in dechanneling rate with depth is related to the increase in density of dislocations on approaching the interface. Curve (b) (no. 37) is indicative of our best GaAs on Si(100) grown to date, but it still shows a significant additional dechanneling compared with curve (a).

Figure 5 compares the dechanneling rates for samples where the GaAs was deposited directly onto the Si(100) (curve (c); no. 37) or an intermediate Ge layer (curve (b); no. 66). The two examples exhibit essentially the same dechanneling rate, and χ_{min} ~4.8%. (Note that the overall thickness of the epilayers (i.e., GaAs or Ge plus GaAs) is approximately the same in these two layers.) A rough calculation of the dislocation density based on the RBS results (11) yields values in the range 10^8–10^9 cm^{-2} for the two samples, in agreement with the XTEM results.

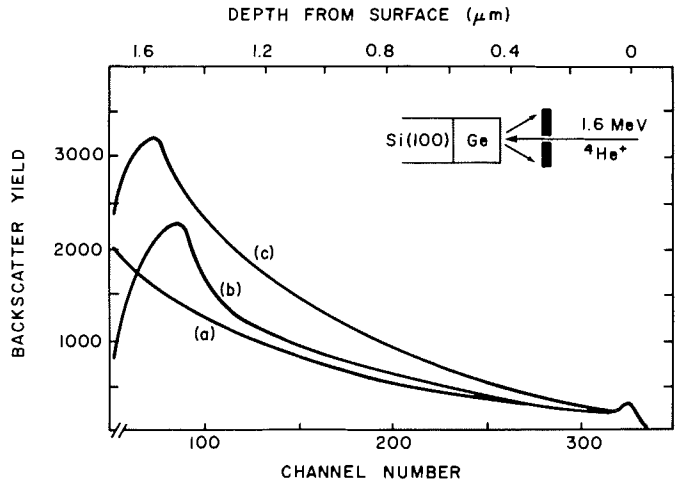

FIG. 6. A 180° Rutherford baekscattering spectra of 1.6 MeV HE^+ incident along the normal ⟨100⟩ direction of different epilayers. The epilayers are as follows: (a) 3.5 μm epilayer of GaAs on GaAs(100), (b) 1.5 μm epilayer of Ge on Si(100), and (c) etched Ge layer of sample no. 66 (i.e., GaAs epilayer removed). Note that unfortunately, the Ge epilayer upon which the GaAs epilayer was deposited was not typical of the best Ge layers grown to date.

The crystalline quality of the Ge layer no. 66E has been examined by selectively etching off the GaAs from no. 66 and repeating the measurement. Figure 6 compares sample no. 66E, curve (c), with a previously grown Ge epilayer (no. 23) on Si(100), curve (b). The dechanneling rate of no. 66E is significant higher, indicating that the Ge layer onto which the GaAs was deposited was, unfortunately, not the best attainable. Deposition onto no. 23 would have likely improved the quality of the GaAs layer significantly. Note also that the large density of misfit dislocations at the Si–Ge interface is clearly indicated by the dramatic rise in the dechanneling rate.

4. Conclusions

The GaAs epilayers grown on Si(100) substrates in these experiments have substantially higher dislocation and stacking-fault densities than those grown on GaAs substrates. The dislocation density decreases markedly with distance from the initial interface, but even in our best epilayers it is ~10^8 cm^{-2} after a few micrometres of growth. Comparable dislocation densities and variations occur in Ge films grown directly on Si, indicating that the overall lattice mismatch probably determines the epilayer defect structure.

Thus far, the GaAs layers grown on Ge buffer layers have not been significantly better than those grown directly on Si. However, GaAs has not yet been grown on the best Ge layers we have obtained. Ge epilayers annealed to 700°C for 30 min have been shown by XTEM to have a substantially reduced defect density, $\leq 10^7$ cm^{-2}.[4] GaAs grown on such layers should show corresponding improvement.

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