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SOI-Based Silicon Quantum Dots Contacted by Self-Aligned Nano-Electrodes

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ABSTRACT

In this paper we present a novel approach to fabricate single-electron devices utilizing different self-organization and self-alignment effects. Silicon quantum dots (QDs) are obtained employing reactive ion etching (RIE) into a silicon-on-insulator (SOI) substrate with a self-assembled etch mask. Electrodes with nanometer separation are fabricated and aligned to the QDs by means of a controlled electromigration process. The tunneling rates of the devices are defined by the native oxide covering the silicon QDs and can be adjusted by self-limiting thermal oxidation. The devices show clear Coulomb blockade behavior as well as Coulomb staircase features. In some samples also a gate influence is present giving rise to Coulomb diamonds in the differential conductance diagram.

INTRODUCTION

The current development in electronics leads to smaller and smaller structures already reaching the sub-100 nm region. In this regime new physical phenomena like the single-electron tunneling effect [1] become important. A device making use of this new effect is the single-electron transistor (SET), which attracted much interest in the last two decades [2-4,8,15]. It combines a reduction in size with a reduced power consumption and thus lower heat production. For SETs operating at room temperature, small conductive islands are needed. One candidate for these small islands are semiconductor quantum dots (QDs) [2,8].

The fabrication of SETs involves three major tasks. Firstly, one has to produce small conducting islands or QDs. This can be achieved by different approaches such as Stranski-Krastanov epitaxy [5,6], dry etching [7,8] or by means of chemical methods [2,3,9]. Secondly, one has to fabricate nano-electrodes with a separation of only a few nanometers. Approaches to this task include conventional e-beam lithography [3,10], shadow evaporation [2,11], electrochemical plating [12,13] and electromigration [4,14]. Finally, the islands or QDs have to be positioned between the electrodes such that the separation between the island and the two electrodes results in an adequate tunneling resistance. Since the tunneling rate depends exponentially on the distance, this task is particularly difficult. Solutions to this problem include linker molecules which bind to colloids or QDs deposited from a solution [2,3], and the utilization of an oxide formed either on the island or on the electrodes [15].

In this paper we introduce a novel approach to fabricate SETs making use of a combination of three different self-organization and self-alignment effects. Quantum dots are patterned into a silicon-on-insulator (SOI) substrate with a self-organized etch mask. On top of the QDs nano-electrodes are defined and self-alignment to the present QDs is achieved with an electromigration process. The well defined native oxide of the silicon QDs is used as a tunneling barrier. Further control on the tunneling barriers is obtained by using self-limiting thermal oxidation [7], which allows to adjust the oxide thickness and thus the tunneling rates.

SAMPLES & EXPERIMENTS

In a first series of experiments, QDs with a size of 50 or 20 nm were obtained as shown in the schematic overview of the fabrication process given in figure 1. As substrate we used a SIMOX-SOI wafer with a top silicon layer of 50 nm, which we thinned down to 20 nm in an isotropic CF_4 plasma for our 20 nm QD samples. The samples were treated with aminosilane [3-(2-aminoethylamino)propyltrimethoxysilane] (APTS) diluted in deionized water (1:2000) for 5 min and baked at 120 °C for 30 min [3]. During this procedure the silane groups replace the hydroxyl (-OH) previously adsorbed on the native SiO_2 forming a siloxane bond while the amino groups act as an adhesion agent for gold particles. Thereafter the samples were immersed for 24 hours into a commercially available solution of gold colloids with a diameter of 50 and 20 nm, respectively. After rinsing and drying the gold particles had arranged in a sub-monolayer, which served as an etch mask in the following reactive ion etching (RIE) process. CF_4 was used as etch gas for its anisotropic behavior, and the etch time was chosen so as to yield an etch depth of about 70 or 30 nm, respectively. After removing the gold mask with a wet chemical etch in an aqueous I_2KI solution, we obtained 50 or 20 nm silicon QDs on an insulating SiO_2 layer. In addition, some of our samples were thermally oxidized for 3 hours in an oxygen atmosphere at 820 °C. This self-limiting thermal oxidation process [7] leads to an increased thickness of the SiO_2 layer covering the QDs.

On top of the QDs a 100 nm wide wire and two side gate electrodes were defined into a bi-layer polymethylmethacrylate (PMMA) resist employing electron beam lithography (EBL). After evaporation of 5 nm Ti and 25 nm Au for the 50 nm QDs and 3 nm Ti and 13 nm Au for the 20 nm QDs a lift-off was performed in 1-methyl-2-pyrrolidone. The structures were further contacted via standard photolithography.

A controlled electromigration process [16] was performed to create a gap of only a few nanometers in the previously defined metal wire. Therefore a voltage was applied to the wire and steadily increased until the conductance dropped about a defined fraction. Then the voltage was reduced, and the procedure repeated until the desired conductance was reached. Because the metal film of the wire is locally dilated by the QDs, the cross-sectional area is reduced leading to a higher current density. By this mechanism the wires preferentially break at positions of QDs resulting in a self-alignment effect.

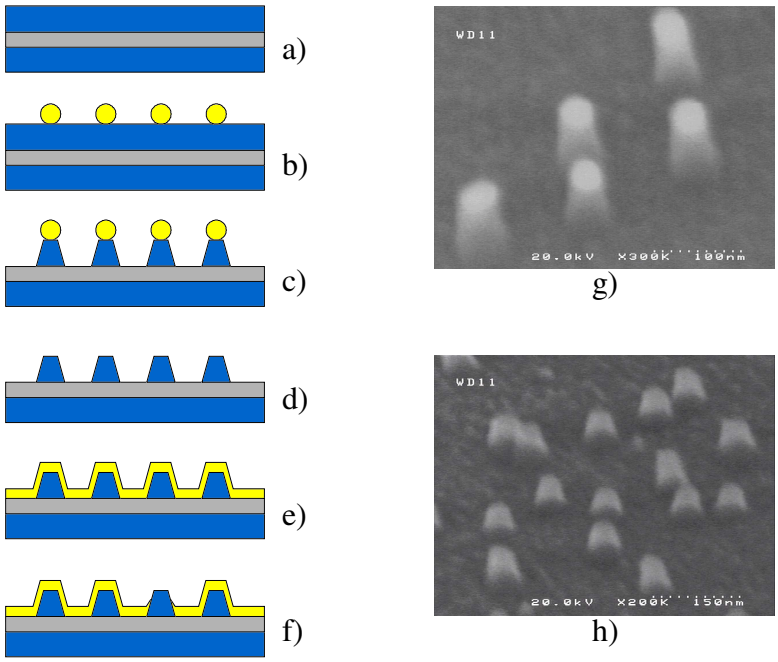

Figure 1: Schematic overview of the fabrication process: SOI substrate (a), self-assembly of gold colloids (b), RIE process (c), gold etch (d), patterning of contacts (e) and electromigration (f). SEM micrographs of silicon QDs before (g) and after (h) gold mask removal.

The electromigration process was typically performed in a liquid helium cryostat at a temperature of 4.2 K. Directly after breaking the contact, I(V)-measurements were conducted to electrically characterize the devices. A source-drain voltage was applied and the source-drain current was measured with a Keithley SMU with an accuracy of about 1 pA. For extended measurements a gate voltage was connected to the side and/or the back gates with an additional SMU.

RESULTS & DISCUSSION

First, samples with 50 nm QDs were measured after electromigration at 4.2 K. Besides tunneling current behavior or open contacts, many devices showed I(V)-curves with current suppression around zero bias due to Coulomb blockade. The plateau was typically between 50 and 140 mV wide. In addition, some contacts also showed a Coulomb staircase with several steps. In figure 2 an exemplary I(V)-trace is depicted together with an orthodox theory [1] fit, extended to account for a nonlinear tunneling resistance. As can be seen, the measured curve agrees reasonably well with the calculation. From the calculation an island capacitance of 3.1 aF is extracted, which allows us to estimate the size of the island assuming the capacitance to be the self-capacitance of a sphere. The resulting diameter of the island is calculated to be 56 nm, which is in good agreement with our device dimensions.

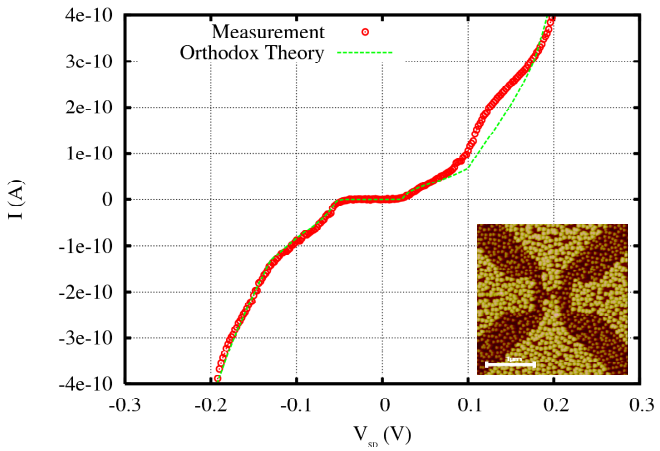

Figure 2: Measured I(V)-curve (circles) showing a Coulomb staircase and corresponding orthodox theory calculation (dashed line). Inset: AFM scan of a typical device after electromigration.

Besides these devices a few contacts showed Coulomb blockade with a much wider plateau of up to 400 mV and more. These I(V)-curves can not be fitted by the orthodox theory with a reasonable size for the silicon QDs. They are assumed to be due to small metal islands created during the electromigration process, which also happens on samples with no silicon QDs present.

Next we applied a gate voltage to the side gates as well as to the back gate, while keeping the source-drain voltage at a fixed value (10 mV), and measured the source-drain conductance. Figure 3 shows an exemplary measurement where one can clearly see the conductance modulation typical for a SET device.

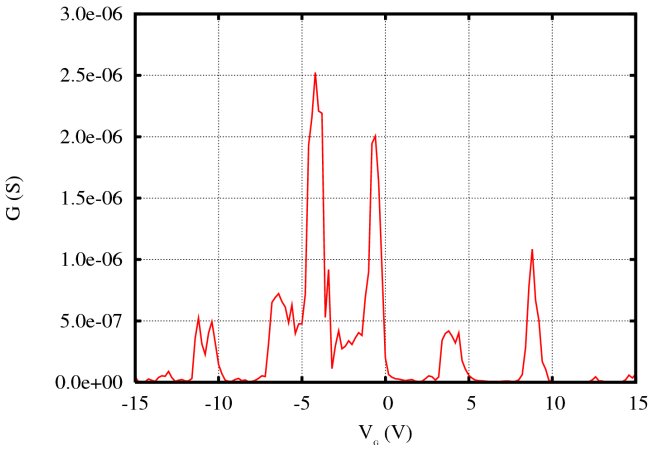

Figure 3: Conductance plotted against gate voltage at a constant source-drain voltage of 10 mV. A nearly periodic conductance oscillation can be seen.

By collecting $I_{SD}(V_{SD})$-curves for different gate voltages, calculating their numerical derivatives and assigning a corresponding color (brightness), one gets a 2-dimensional plot of the differential conductance also known as "stability diagram", which is shown in figure 4. The dark diamond shaped areas mark stable configurations of the device where the number of electrons on the island is constant and no current can flow. Because of their shape they are referred to as "Coulomb diamonds". From these measurements the gate capacitance can be calculated to be about 0.035 aF, which is very low and desired to be higher. Unfortunately, not even all devices show this kind of gate dependence, which implies that the gate efficiency has to be further improved.

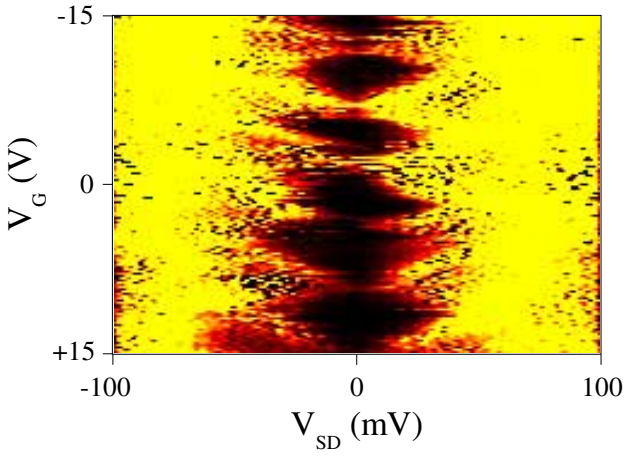

Figure 4: Differential conductance dI/dV_{SD} plotted versus source-drain and gate voltage. Dark colors correspond to low, bright colors to high differential conductance. Coulomb diamonds are clearly visible.

Besides the samples with 50 nm QDs covered by native oxide, also a few samples with 20 nm QDs, and samples which were additionally oxidized were investigated. The measurements on samples with 20 nm QDs mostly show I(V)-traces with a wider plateau of 130-200 mV, which is consistent with theory. Experiments on samples with 50 nm QDs and additional thermal oxidation at 820 °C yield a higher number of functional contacts. Another difference to the non-oxidized samples was the typically lower current and higher resistance of the devices after electromigration. The self-limiting thermal oxidation thus appears to be a suitable way to adjust the tunneling resistance.

CONCLUSIONS & OUTLOOK

We have introduced a novel method to fabricate single-electron devices utilizing a combination of different self-assembly and self-alignment effects. These self-organizing techniques comprise a convenient way to adjust the device parameters. The island capacitance can be controlled by the SOI thickness and the diameter of the gold particle etch mask, whereas

the tunneling resistance can be adjusted by self-limiting thermal oxidation. Our devices show Coulomb blockade, Coulomb staircases and Coulomb diamonds, which are the typical characteristic of SETs.

Future work will include further reduction of the QD size to realize higher operation temperatures and the improvement of the gate efficiency.

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