Solid-State Electronics Vol. 29, No. 8, pp. 807–813, 1986
Printed in Great Britain

0038-1101/86 $3.00 + 0.00
Pergamon Journals Ltd

THE ROLE OF THE DEVICE SURFACE IN THE HIGH VOLTAGE BEHAVIOUR OF THE GaAs MESFET

T. M. BARTON AND P. H. LADBROOKE
GEC Research Laboratories, Hirst Research Centre, Wembley, Middlesex, U.K.

(*Received* 1 *July* 1985; *in revised form* 21 *November* 1985)

Abstract—Two dimensional computer simulation of the GaAs MESFET in the presence of a uniform surface charge predicted initial gate–drain avalanche voltages at variance with experiment in two respects:

(a) The dependence of initial avalanche voltage upon gate length was weak compared with that evident in practice.

(b) The absolute values of voltage were smaller by a factor of typically 3 than those observed experimentally.

Examination of the potential and charge distributions revealed, even at low gate–drain potentials, electric fields near the drain end of the gate of sufficient magnitude to cause field emission. Electrons emitted in a direction parallel to the GaAs surface may occupy states in the forbidden band, which would result in a dynamic excess of charge residing on the surface immediately adjacent to the drain end of the gate. Inclusion of this effect in the computer model resulted in a simulated device behavior which is now similar to that found in practice.

NOTATION

A constant
B ionisation coefficient (cm^{-1})
F_o ionisation coefficient ($V \cdot cm^{-1}$)
E_c energy of conduction band edge
E_f Fermi energy
E_v energy of valence band edge
h mesh spacing
I^* ionisation integral
k Boltzmann's constant
l position variable along a path
n free electron density
n_i free electron density in intrinsic GaAs
N_C effective density of states in the conduction band
N_D doping level in the n-layer
N_{SS} density of occupied surface states (cm^{-2})
N_{SS}' excess density of occupied surface states (cm^{-2})
q electron charge
r cylindrical co-ordinate (radial)
T absolute temperature
V_{DSB} initial drain–source avalanche voltage
V_{GDB} initial gate–drain avalanche voltage
x Cartesian coordinate
y Cartesian coordinate
∇ gradient operator
$\nabla.$ divergence operator
ε permittivity of GaAs
θ cylindrical coordinate (angle)
μ_n electron drift mobility
ϕ potential
ϕ_b barrier height
ϕ_c potential at conduction band edge ($= E_c/q$)
ψ_{fn} quasi-Fermi level, expressed as a potential ($= E_F/q$)

1. INTRODUCTION

The maximum gate–drain potential, or "breakdown" voltage, of a GaAs MESFET is a limiting large-signal parameter which is important in a number of circuit applications. In digital circuits, the breakdown voltage is important because the short gate lengths required for high-speed operation may mean that the device cannot withstand even low supply voltages (less than 5 V). In microwave power applications, the product of the open channel current and the breakdown voltage is an indication of the maximum power that can be delivered by the device [1]. For this reason it is necessary to be able to describe quantitatively the effect of material and device structure factors on the breakdown voltage.

A schematic representation of the drain characteristics of a typical MESFET is given in Fig. 1. When the device is pinched off, little or no drain current flows at low drain–source potentials. As the source/drain potential is increased, excess current appears in the drain, and at high enough drain–source potentials catastrophic failure results. It is generally accepted that the excess current is due to impact ionisation in the gate–drain region [2–5]. There is extensive experimental evidence to support this view, the most graphic of which is the observation of light emission from the drain edge of the gate in the space between the gate and the drain [2].

The breakdown voltage of the FET is dependent upon the product of the channel doping density and the channel thickness (the doping–thickness product). Devices with a higher doping–thickness product tend to have a

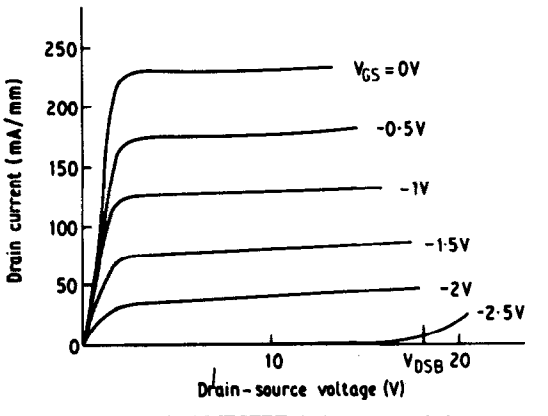

Fig. 1. Typical MESFET drain characteristics.

lower breakdown voltage [3, 5, 6]. Bulk deep states in the channel region also have an effect upon the measured breakdown characteristics when they ionise under high field conditions. In the case of electron traps, an extra centre of positive charge is created in the depletion region, thus increasing the positive ion density and reducing the breakdown voltage. Above a certain limit (typically 1.5 μm), the gate–drain spacing appears to have little or no effect upon the breakdown voltage under pinched conditions. As long as the depletion region does not reach the drain, this contact has little effect on the breakdown voltage because the undepleted channel region effectively screens the depletion region from the drain contact under zero-current conditions.

An important, but previously underemphasised, factor governing the breakdown voltage is the length of the gate [6–9]. Figure 2 shows this dependence for some Cornell University power FETs [7,8]. In these experiments, breakdown was taken to mean the gate–drain voltage for the onset of avalanche multiplication, where "onset" in turn means that the "soft" drain current reached a value of $\simeq I_{DSS/25}$. To make such a measurement, the FET was pinched off, the drain–source voltage was increased, and the gate voltage was increased (negatively) until the sum of the two was a maximum at the stated current criterion: this maximum sum was taken to be the initial gate–drain avalanche voltage, V_{GDB}. Over the range 0.2–2.0 μm in Fig. 2, the breakdown voltage is proportional to the gate length for these particular devices. Except for the simulation by Wroblenski *et al.* [10] (Fig. 9), the possibility that the breakdown voltage could be dependent upon gate length has not been addressed [4, 5].

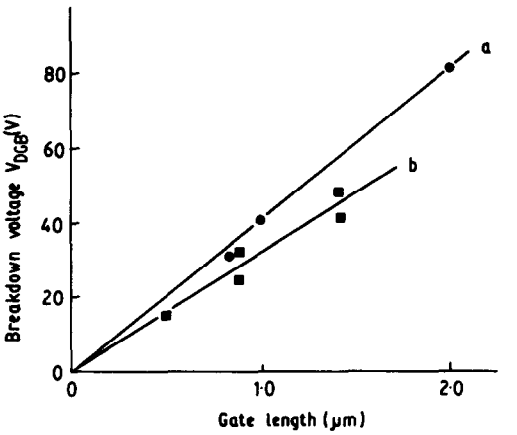

Fig. 2. Breakdown voltage vs gate length of some Cornell power FETs: (a) from Tenedorio [8] and (b) Fu [7].

Finally, there is often scatter in the breakdown voltages of nominally similar devices even in experiments where every effort is made to control device dimensions, layer doping profiles, and fabrication process steps [9].

2. RESULTS OF EARLY SIMULATIONS

The modelling scheme used in this paper is described in the Appendix. An equipotential plot for the device in Fig. 3, without surface charge, appears in Fig. 4. This has a form similar to those shown by other authors [3,5]. The extension of the depletion region toward the drain from the end of the gate varied roughly in proportion to the gate–drain potential. If the source and the drain were held at the same voltage, and the gate bias voltage stepped from zero volts, the width of the depletion region varied as predicted by simple one dimensional theory (for sufficiently long gate lengths) and the device pinched off at the correct potential. When surface charge was added to the model, a depletion region was induced under the surface with a width which is the same as predicted by simple one-dimensional theory.

To test the dependence of the breakdown voltage upon the gate length, three devices of a similar geometry to that shown in Fig. 3 were simulated. The only difference between the devices was the lengths of the gates, which were 0.5, 1.0 and 2.0 μm. The devices all had a doping density of 1.0×10^{17} cm^{-3} and a surface charge density of 1.0×10^{12} cm^{-2}, corresponding to a band bending of approximately 0.8 V at the surface. The channel depth was 0.2 μm, and the buffer was modelled

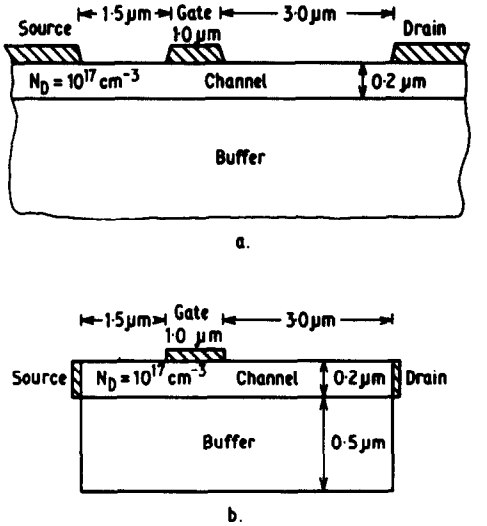

Fig. 3. Typical device used in simulations: (a) device geometry, (b) model geometry.

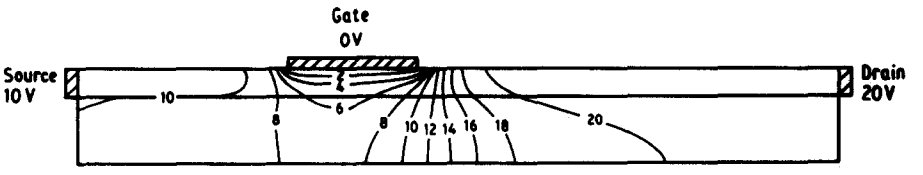

Fig. 4. Equipotential plot of the device of Fig. 3 with V_{gd} = 20 V.

to a depth of 0.5 μm below the channel–buffer interface. The source–gate and gate–drain spacings were 1.5 and 3 μm, respectively.

All three devices were found to break down at less than 10 V compared with the 20 or 30 V commonly measured experimentally for a 1.0 μm gate length device. In addition, and most importantly, no significant dependence of the breakdown voltage upon the length of the gate could be found from the simulations.

3. RE-EXAMINATION OF THE MODEL

When the charge distribution on the gate is examined, charge densities are found which, even at low gate–drain potentials, are extremely high. Figure 5 shows a plot of the electric field normal to the gate of a 1 μm device at a gate–drain potential of 20 V. The singular region predicted by Wasserstrom, McKenna and Lewis [11–13] at the ends of the gate is clearly visible. The field has a magnitude greater than 1000 kV cm^{-1} over the first 500 Å from the drain end of the gate.

The implication is that the field singularities discussed by Wasserstrom *et al.* do not exist in the real device. While the numerical techniques used here predict a field magnitude of 4500 kV cm^{-1} at the drain end of the gate, and somewhat less at the source end, an analytic solution to Poisson's equation would result in an infinite field at those points. (The detailed value of the field at the drain edge of the gate obtained from the simulation is an artefact of the mesh spacing, which was approximately 25 monolayers of GaAs in the present work. With the form of potential given by eqn (A9) of the Appendix, a finite value for the field results from finding the gradient in potential over the first mesh interval.)

It seems likely, therefore, that there is some effect which counteracts the singularity. One possibility is that, due to fabrication technique, and perhaps image force lowering, the edge of the gate is not sharp on a microscopic scale as commonly modelled, but has some curvature as in Fig. 6. From Fig. 5, however, the radius of curvature of the gate end would have to be at least 500 Å to keep the incident field below 1000 kV cm^{-1}, and even greater to result in lower fields. Such a large curvature is unlikely in practical devices.

A second possible mechanism by which the effects of the singular fields at the edge of the gate may be counteracted is the one which is presented as the main result of this paper. The magnitude of the electric field at the drain end of the gate along the section A–A of Fig. 7 results in a band diagram as shown in Fig. 8(a). An electron at the metal Fermi energy has only to tunnel a distance of about 20 Å to reach the conduction band of the semiconductor.

Comparing Fig. 8(a) with the band diagram along the section B–B, the gate-to-surface interface, a different phenomenon can be postulated. The diagram of Fig. 8(b) shows the band diagram along the surface of the device from the drain edge of the gate.

There is evidence that the surface of GaAs may contain as many as 10^{14} cm^{-2} available electron states [14,15]. For an electron tunneling from the metal Fermi energy, some of these states would lie in closer spatial proximity to the drain edge of the gate than would states in the conduction band [see Fig. 8(b)]: hence we assume an electron may tunnel between the gate and one of these states. Once electrons have tunnelled into surface states, they may do one of several things. They may tunnel into surface states of the same energy or make transitions into states of different energies. They may also tunnel through to the conduction band and be transported to the drain. Electrons already in the conduction band may recombine into surface states, and those already there may recombine into the valence band.

Irrespective of the processes involved in the movement of electrons onto and off the surface, electrons tunnelling from the gate will result in a net density of charge at the surface near the drain end of the gate which is in excess of that due to Fermi-level pinning.

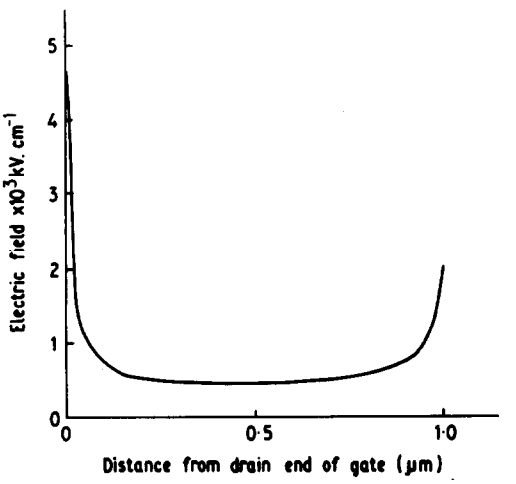

Fig. 5. Normal electric field distribution along the gate.

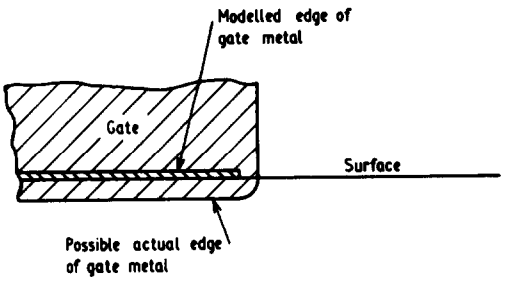

Fig. 6. Possible radius of curvature at ends of gate metal.

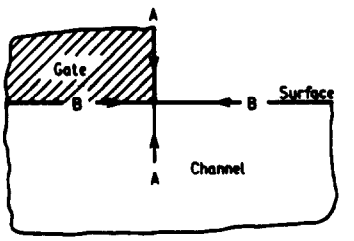

Fig. 7. Axes along which the band diagrams of Fig. 8 lie.

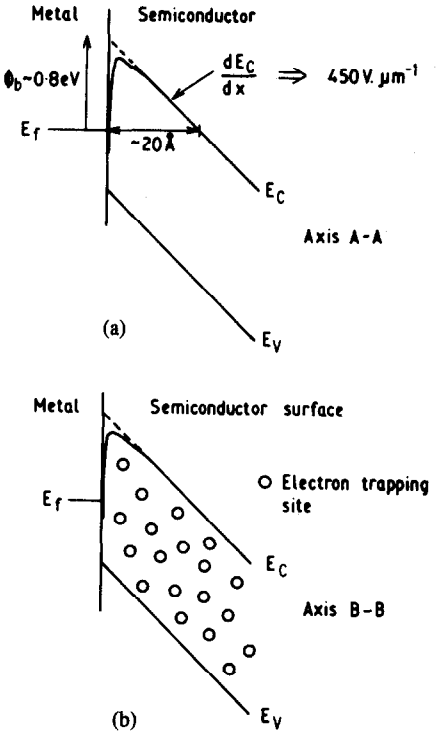

Fig. 8. Band structure (a) into bulk of device along axis AA of Fig. 7, and (b) along device surface, axis BB.

Figure 9 sketches the charge distribution in a device with excess surface charge. The field incident upon the drain edge of the gate will be reduced by the presence of the excess charge. To a lesser extent this surface charging effect will also occur at the source end of the gate.

4. SIMULATION OF EXCESS SURFACE CHARGE

The density and distribution of excess surface charge is dependent upon the spatial and energy distribution of states on, or in close proximity to, the semiconductor surface, the capture and emission properties of these states and upon the band-structure at the gate–semiconductor interface.

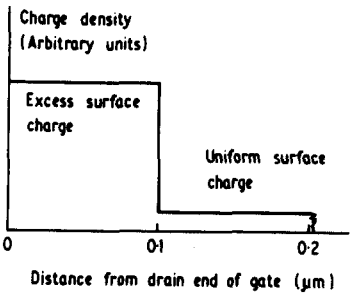

Fig. 10. Distribution of excess surface charge commonly used in model.

It is likely that the band structure on the surface around the drain edge of the gate is dissimilar from that of the "bulk" surface for several reasons. First, the density of allowed states in the conduction and valence bands may be altered by the intense fields in this region (the Franz–Keldysh effect). Second, surface superlattice effects may alter the band structure of the surface [16]. Finally, it is possible that metal wavefunctions may penetrate up to several lattice spacings into the semiconductor. Pseudo-potential calculations [14,15] for the GaAs surface and metal–semiconductor interfaces have indicated that metal wavefunctions may penetrate up to several angstroms into the semiconductor and that "bulk" lattice properties are not attained for several lattice spacings.

Given the prohibitive time that would be required to write a simulation program to solve the excess surface charge problem self-consistently, an approximate solution was sought by modifying the existing model. Solutions were obtained for a series of fixed surface charge distributions. Although this method does not yield exact solutions, it does provide insight into the effect of excess surface charge on the breakdown behaviour. A typical assumed distribution is rectangular, extending 0.1 μm from the drain end of the gate with electron densities ranging from 10^{12} to 1.4×10^{13} cm^{-2}. Triangular distributions yielded similar results.

Figure 11 is a plot of the gate electric field distribution for several values of surface charge on a 1.0 μm gate

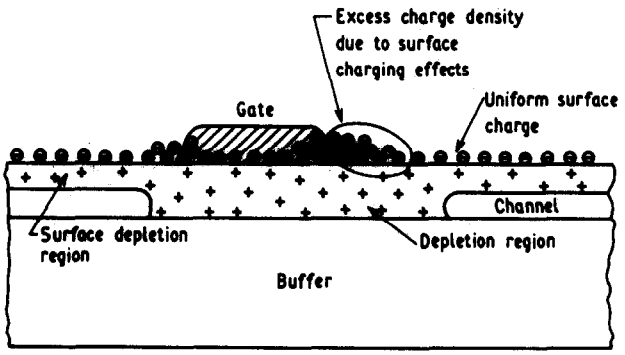

Fig. 9. Charge distribution throughout the device under pinched conditions.

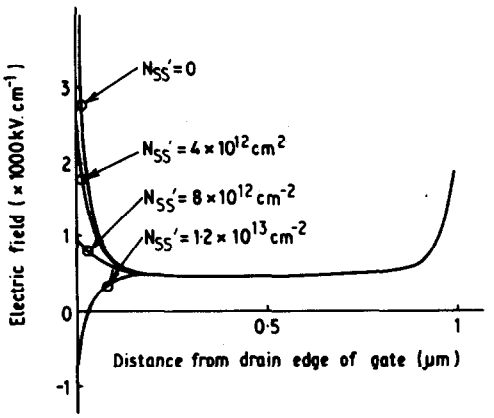

Fig. 11. Electric field distribution on gate for various magnitudes of surface charge, of the distribution in Fig. 10.

FET with a gate–drain potential of 20 V. At lower values of surface charge, the singularity at the drain end of the gate is still in evidence. As the density of excess surface charge is increased, however, the magnitude of the electric field gradually decreases until, at an electron density of 1.0×10^{13} cm^{-2}, the electric field at the drain end of the gate is practically zero. Higher values of surface charge result in a reversal of the direction of the field at the end of the gate.

This last observation points to the possibility of a self-regulating mechanism of the excess surface charge. If the density of charge on the surface is low, tunnelling will occur from the gate metal into surface states. If, on the other hand, the density of filled surface states is too high, the field on the drain end of the gate will reverse. Electrons will then move from the surface onto the gate, reducing the density of the surface charge. On this basis, the charge on the surface adjacent to the gate might be expected to adjust in sympathy with that on the gate, resulting in a component of field parallel to the surface of a magnitude less than that required for field emission.

For the purposes of the present investigation, the amount of surface charge was varied to obtain as uniform a gate charge distribution as possible. This criterion arises from associated work [9] on the correspondence between experiment and an analytic theory of the GaAs MESFET under pinched channel conditions [9]. In this theory the depleted channel/surface/gate is treated as a closed-charge system, and an approximate Green's function method is used to determine the induced gate charge. Varying degrees of suppression of the gate-edge singularity can be accommodated in this model, depending principally upon whether the channel is treated in a "thin channel" approximation, or a "thick channel" approximation. In the latter case, the induced gate charge is found to be uniform, and it is this case which predicts gate–drain breakdown (initial avalanche) voltages in agreement with experiment. (In fact, it was this theory which prompted the systematic practical search for gate–drain breakdown proportional to gate length.) Against this background, the criterion of an essentially uniform gate charge was adopted for the present computational study. Thus, for a given gate–drain potential, the magnitude of the excess surface charge was adjusted to yield the flattest possible gate charge distribution, and the ionisation integral evaluated. The procedure was repeated for increasing gate–drain potential until breakdown was reached.

This procedure resulted in an entirely different device behaviour compared with the case where excess surface charge was not included. The breakdown voltage of the 1.0 μm gate device was now found to be 28 V, which is similar to the commonly observed breakdown voltages of these devices. The 0.5 and 2.0 μm gate devices broke down at voltages of 17 and 62 V, respectively. The dependence of the breakdown voltage upon the gate length is plotted in Fig. 12, along with those of the Cornell University power FETs [7,8]. The addition of excess surface charge to the model results in a predicted behaviour which is comparable to that found in real devices.

5. DISCUSSION AND CONCLUSION

The work described here reveals little about the processes which may be responsible for the movement of charge onto and off the device surface or the rate at which this occurs. Nevertheless it demonstrates the importance of the surface in determining GaAs FET characteristics in the low current, high voltage, limit. Uncontrolled surface effects may be responsible for the variation in breakdown voltage sometimes found between nominally identical devices. Similarly, differences in the breakdown characteristics of passivated and unpassivated devices may in part be due to changes in surface states associated with the passivation process. Rate-dependent surface effects may explain the discrepancy that is sometimes found between the power predicted by the product of the open channel current and the breakdown voltage of the device, and the power that is actually measured under microwave conditions.

In conclusion, simulation of the breakdown behaviour of the GaAs FET with uniform surface charge, and

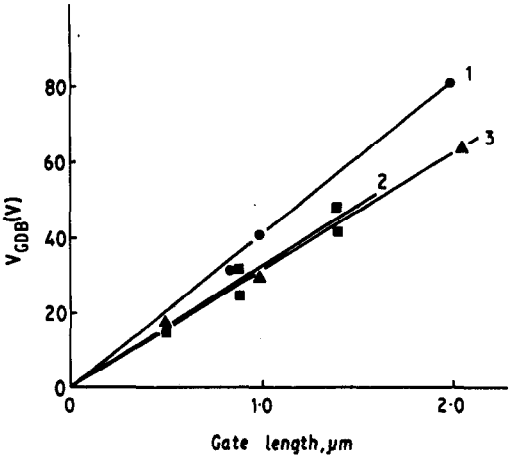

Fig. 12. Breakdown voltage of model with excess surface charge, vs gate length. ● (1) From Tenedorio $N_D = 8 \times 10^{22}$ m^{-3} [8]. ■ (2) From *Fu*, $N_D = 8 \times 10^{22}$ m^{-3} [7]. ▲ (3) From Computer Model, $N_D = 1 \times 10^{23}$ m^{-3}.

under pinched conditions, bears little relation to measured device characteristics. This has been shown to be due, at least in part, to the high electric field which forms at the drain end of the gate. It has been proposed that as this high field region forms in the real device, electrons tunnel off the gate into surface states, thus giving rise to a charge density on the device surface which is locally in excess of that caused by Fermi-level pinning. Simulations including this excess surface charge have shown that it results in a reduction of the field and a simulated behaviour which is similar to that of practical devices.

Acknowledgements — Part of this work was carried out at the University of New South Wales, Sydney, Australia. The support of the Radio Research Board of Australia, and of the Joint Microelectronics Research Centre, is gratefully acknowledged.

REFERENCES

1. J. V. Dilorenzo and W. R. Wisseman, *IEEE Trans. Micro. Th. Tech.* **MTT-27**, 367–378 (1979).
2. R. Yamamoto, A. Higeshisaka and F. Hasegawa, *IEEE Trans. Electron. Dev.* **ED-25**, 567–573 (1978).
3. J. P. R. David, J. E. Sitch and M. S. Stern, *IEEE Trans. Electron. Dev.* **ED-29**, 1548–1552 (1982).
4. W. R. Curtice, *8th Biennial Cornell Electrical Engineering Conf. Proc.* 209–222 (1981).
5. W. R. Frensley, *IEEE Trans. Electron. Dev.* **ED-28**, 962–970 (1981).
6. H. M. Macksey and F. H. Doerbeck, *IEEE Electron Dev. Lett.* **EDL-2**, 147–148 (1981).
7. S. Fu, Ph.D. thesis, Cornell University, Ithaca, NY (1983).
8. J. Tenedorio, Ph.D. thesis, Cornell University, Ithaca, NY (1982).
9. C. Lowe, Ph.D. thesis, Cornell University, Ithaca, NY (1984).
10. R. Wroblenski, G. Salmer and Y. Crosnier, *IEEE Trans. Electron Dev.* **ED-30**, 154–159 (1983).
11. E. Wasserstrom and J. McKenna, *Bell Syst. Tech. J.* **49**, 853–877 (1970).
12. J. A. Lewis and E. Wasserstrom, *Bell Syst. Tech. J.* **49**, 1183–1194 (1970).
13. J. A. Lewis, *Bell Syst. Tech. J.* **49**, 1483–1490 (1970).
14. W. F. Croyden and E. H. C. Parker, *Electrocomponent Science Monographs* **2**, Gordon and Breach Science Publishers, London, 1981.
15. S. G. Louie, J. R. Chelikowsky and M. L. Cohen, *J. Vac. Sci. Technol.* **13**, 790–797 (1976).
16. P. J. Stiles and J. Cole, *J. Vac. Sci. Technol.* **14**, 1094–1095 (1977).
17. K. B. Whiting, *IEEE Trans. Micro. Th. Tech.* **MTT-16**, 889–891 (1968).
18. J. W. Duncan, *IEEE Trans. Micro. Th. Tech.* **MTT-15**, 575–582 (1967).

APPENDIX

A.1 *Formulation of the computer model*

It is possible to make a significant simplification to the modelling scheme given the condition under which breakdown occurs. We consider the steady state only ($\partial/\partial t = 0$). The breakdown of interest is impact ionisation occurring when the device is pinched off, implying that the current density in all parts of the device is zero until breakdown is reached, i.e.

$$J_n = 0. \tag{A1}$$

It follows that the divergence of the current density is also zero,

$$\nabla \cdot J_n = 0. \tag{A2}$$

The current density equation is

$$J_n = nq\mu_n \nabla \psi_{fn}. \tag{A3}$$

Substitution of the zero current condition, eqn (A1), gives the result that the quasi-Fermi level is constant throughout the device, that is

$$\nabla \psi_{fn} = 0. \tag{A4}$$

These results allow both the current density and continuity equations to be omitted from the solution.

The quasi-Fermi level, ψ_{fn}, is found by solution of the equation

$$n = N_c \exp \frac{q}{kT}(\psi_{fn} - \phi_c) \tag{A5}$$

in the non-depleted regions of the channel near the drain and source contacts, where it is assumed that all of the donor atoms are ionised, and thus $n = N$. This gives two values for ψ_{fn}, one found from the source potential, the other from the drain. The channel is divided into two regions, one from the source contact to the middle of the depletion region, the other from the drain contact to the middle of the depletion region, and Poisson's equation

$$\nabla^2 \phi = \frac{q}{\varepsilon}\left\{ n_i \exp\left[\frac{q}{kT}(\phi - \psi_{fn})\right] - N_D \right\} \tag{A6}$$

may be solved by applying the local value of the quasi-Fermi level in each region. Of course, one expects the electron quasi-Fermi level to be continuous throughout the entire device, with significant gradients in ψ_{fn} only in regions of deep depletion. Recognition of this fact allows the use of the computational scheme employed here since the gradient in ψ_{fn} is unimportant in those regions where it is not evaluated — there are no electrons there anyway.

The buffer region of the device is modelled as an undoped region. The current density is assumed to be zero, as the number of available carriers is small and, under conditions of zero drain current, there is no injection from the channel into the buffer. Thus in the buffer region, eqn (A5) reduces to Laplace's equation

$$\nabla^2 \phi = 0. \tag{A7}$$

Equations (A5), (A6) and (A7) are solved for the device geometry of Fig. A1. The source, gate and drain are modelled as equipotential boundaries to which external voltages are applied. Zero normal electric field is assumed on the sides and bottom of the buffer. All electric field lines starting on positive charges (the depletion region) will then terminate on negative charge within the structure.

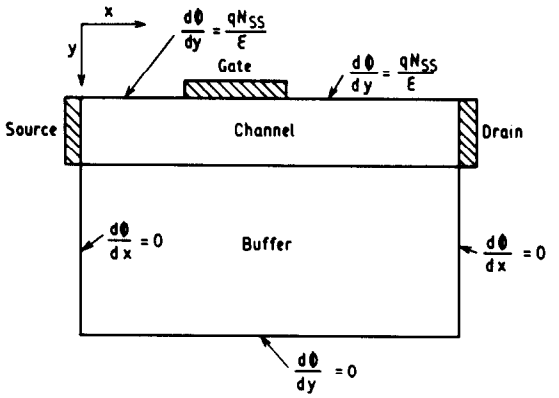

Fig. A1. Geometry of the computer model, showing boundary conditions.

The charge induced in states on the GaAs surface by Fermi-level pinning is modelled by assigning a value to the normal component of electric field, given by

$$\frac{\partial \phi}{\partial y} = \frac{qN_{ss}}{\varepsilon}. \tag{A8}$$

A five point finite difference method is used to solve eqns (A5), (A6) and (A7) throughout the device.

A.2 *Treatment of the gate-end singularity*

Work by Wasserstrom, Lewis and McKenna [11–13] has indicated the presence of a singularity in the field function at the edges of the gate metal. The accuracy of the usual finite difference representation of Poisson's equation is degraded near the singularity due to the associated rapid changes in field.

Two methods are available for minimising this error. The first employs an analytic expression for the potential function in the region very close to the singular point. It can be shown [13,17,18] that the potential, expressed in polar coordinates has the form

$$\phi = Ar^{1/2} \sin \frac{\theta}{2} \tag{A9}$$

where r is the radial distance from the end of the gate, and the angle θ is measured from the gate metal. The expression may be applied directly to calculate the potentials of the finite difference grid nodes closest to the ends of the gate.

The approximation can only be applied when the device surface supports no charge. Surface charge destroys the angular symmetry implied by the boundary conditions of a charge free surface by introducing a normal component of electric field at the surface.

The second method, which is the one used here, is to superimpose a finite difference grid with a smaller nodal spacing over the main grid, as shown in Fig. A2. The mesh spacing in the high resolution grid is equivalent to approximately 25 monolayers of GaAs. Comparison of the field function with and without the smaller grid showed changes of up to 50% in the potential at some nodes near the end of the gate.

A.3 *Calculation of the ionisation rate*

It is not possible to investigate the dynamics of the breakdown phenomenon due to the assumption of zero current flow.

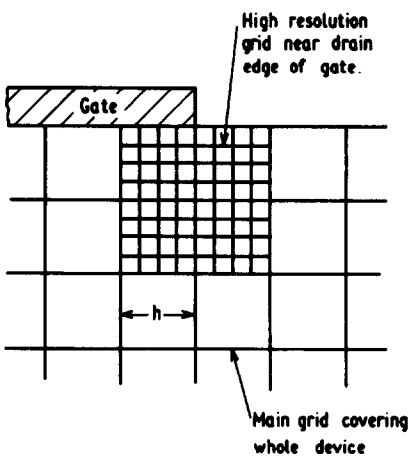

Fig. A2. High resolution grid, employed near drain edge of gate.

The ionisation rate along any path between gate and drain can instead be found from the ionisation integral,

$$I^* = \int_{\text{path}} B \exp\left[-\left(\frac{F_o}{F(l)}\right)^2\right] dl \tag{A10}$$

where l is a spatial coordinate along the path, $F(l)$ being the magnitude of the electric field at that point. This integral is highly dependent upon the magnitudes and spatial extent of the electric field along the path. The integral was evaluated for various paths between the gate and the drain starting at the drain end of the gate. A device was judged to be breaking down at the gate-drain potential for which the result of eqn (A10) first exceeded 0.99.

A.4 *Ionisation coefficients*

The integrand in eqn (A10), i.e. the electron ionisation rate, is an empirically deduced expression wherein the ionisation coefficients B and F_o are obtained by fitting the experimental ionisation rate data. A diversity of pairs of values (B, F_o) is available from the literature for GaAs. The results in this paper are based upon the values:

$$B = 3.5 \times 10^5 \text{ cm}^{-1}$$

$$F_o = 6.85 \times 10^5 \text{ V} \cdot \text{cm}^{-1}.$$

In order to examine the consequences of using alternative (and, apparently, as equally good) ionisation coefficients, calculations were made using:

$$B = 1.6 \times 10^5 \text{ cm}^{-1}$$

$$F_o = 5.51 \times 10^5 \text{ V} \cdot \text{cm}^{-1}$$

with the result that the predicted initial avalanche voltage increased by typically 15%. Such a change is of only secondary importance to the theme of this paper: of primary importance is the fact that the strong dependence of gate–drain breakdown voltage upon gate length is unaffected by the detailed values of B and F_o employed.