Standardized High Performance 640 by 512 Readout Integrated Circuit for Infrared Applications

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ABSTRACT

This paper describes a standardized high performance 640 by 512 readout integrated circuit [ROIC] for p-on-n detectors such as InSb, Heterojunction HgCdTe, QWIP, and InGaAs. The array is intended to support a wide range of systems through flexibility and advanced modes of operation. The ISC9803 uses a flexible, programmable, multistage pipelined architecture to achieve a state-of-the-art ROIC suitable for applications ranging from hand-held infrared viewers to high-speed industrial imaging systems. A simplified default mode directly supports single output NTSC or PAL operation. Using the programmable mode, the ISC9803 supports such advanced features as dynamic image transposition, dynamic windowing, multiple high-speed multiple output configurations, and signal 'skimming'. Both default and programmed modes support integrate-while-read and integrate-then-read snapshot operation, and variable gain. This array is part of the Indigo Systems family of standard ROICs that use a common architecture and electrical interface.

Keywords: ROIC, Readout Integrated Circuit, p-on-n detectors, InSb, HgCdTe, QWIP, InGaAs, Image Transposition, Windowing, Skimming, Integrate-While-Read, Integrate-Then-Read , Interlaced/Non-Interlaced

1. INTRODUCTION

The standardized high performance 640 by 512 readout integrated circuit (ISC9803) is designed to fill the diverse needs of the IR systems industry. Some systems require advanced features such as flexible integration control, dynamic image transposition, dynamic windowing, multiple outputs, and variable gain. Yet other systems require single output NTSC or PAL operation. System that utilize the recent advances in QWIP detector technology can require ROIC features specific to QWIPS. The 'Standard 640' advanced readout multiplexer was designed to accommodate these requirements. The Standard 640 operation is divided into two major modes of operation. The 'Default' mode which requires less pads to be externally connected but also limits the user to single output, full window, NTSC or PAL operation. The 'Command' mode requires more pads to allow access to the advanced features.

The Standard 640 is fabricated on the advanced 0.6 micron double poly, triple metal process which utilizes high speed CMOS transistors. The unit cells are on a 25um x 25um pitch. The expected operating temperature range is 40k to 300k. Input charge-handling capacity is $11e^6$ carriers.

The Standard 640 is the largest member of Indigo's family of standard ROICs. These include the Standard 128 [with both 30 and 38 micron pitch], the Standard 320 [with a choice of high well capacitance or low background ultra-wide dynamic range unit cells], and a highly flexible 512x1Linear array.

Prior to the introduction of Indigo's standard ROICs, detector manufacturers had no choice but to develop these highly complex, mixed signal ICs themselves or through contracted design houses. ROIC development is expensive and requires a specialized experience base to ensure success. Few organizations can afford such design teams or services and those that can are not motivated toward interface standardization. Under this scenario, third party users of IRFPAs (i.e. camera manufacturers and OEM integrators) have no second-source options. Smaller companies and academic institutions involved in detector material development cannot typically afford experienced ROIC design teams, limiting their work. This concept of standard, off-the-shelf, ROICs has brought several new paradigms to the infrared industry. Existing detector manufacturers can now develop FPA products without the cost, performance and schedule risk of ROIC design. Detector research and development organizations can extend their work, using complete IRFPAs. OEM users can buy IRFPAs from multiple

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sources without redevelopment efforts, benefiting from this emerging industry-standard interface. These users can purchase IRFPAs of varying detector materials with a common interface, allowing one camera design for multiple spectral bands.

2. DEFAULT MODE OPERATION

The default mode does not use on chip serial control register. When the chip is powered up, the device defaults to operation as a standard 640x512 format imager. In default mode, the Standard 640 operates with a single output, variable gain, full window, integrated while read timing, normal scan order, interlaced readout order, no reference output, with skimming, supporting only NTSC or PAL timing. This provides a simple interface that reduce external electronics and power dissipation in applications that do not require advanced ROIC features or high-speed performance. The default mode also supports QWIP operation by using a special biasing procedure. The total required interconnects for this mode of operation is 21.

Figure 1 is the Standard 640 block diagram for the default mode operation. The detector bias generator is adjustable using the VDETADJ pad. The unit cell uses a direct injection topology with an anti-blooming transistor. This signal is then addressed to a column bus and sampled onto a variable gain column amplifier. A skimming function is also provided to globally offset the output signal for high leakage current detectors such as QWIPs. The column amplifier is multiplexed to a single output. Also available is an on-chip temperature sensor. Power control is accomplished by applying a voltage to the IMSTR PAD.

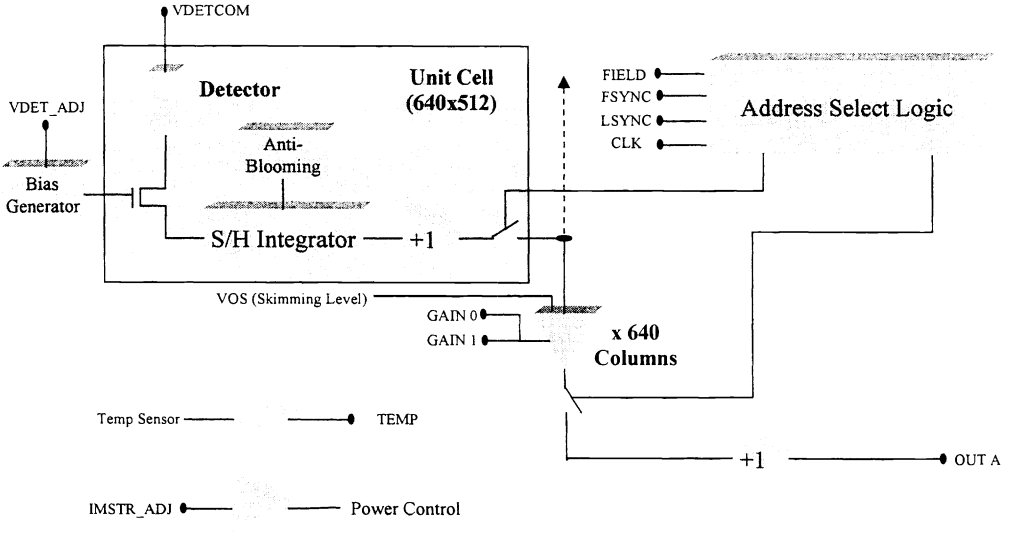

Figure 1- Standard 640 Block Diagram for Default Mode Operation

3. COMMAND MODE OPERATION

The command mode uses the on chip serial control register to control device modes. Figure 2 illustrates the serial control register. To operate in this mode the DATA pad must be used. This allows access to all the advanced features such as windowing, image transposition (invert/revert), multiple output, power bias control, gain select, and skimming. Master clock frequencies up to 5 MHz (10 MHz pixel output rate) with minimum window size can be supported when operating in the command mode. The required number of interconnects is 16-22 depending on the number of outputs and options invoked. Figure 3 shows the Standard 640 Block Diagram for Control mode operation. This block diagram is the same as the default mode diagram with the addition of all functions controlled by the on-chip serial control register. Data loaded into the control register determines the gain setting, detector bias setting, skimming disable setting, output mode, window size, window position, image transposition, and interlaced/non-interlaced readout order.

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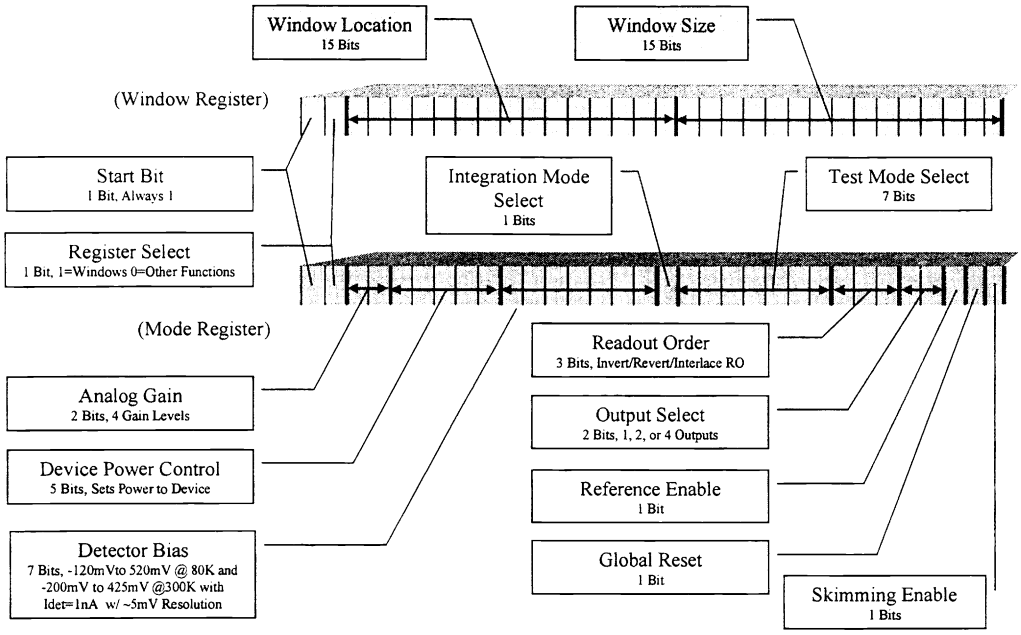

Figure 2- Standard 640 Serial Control Register

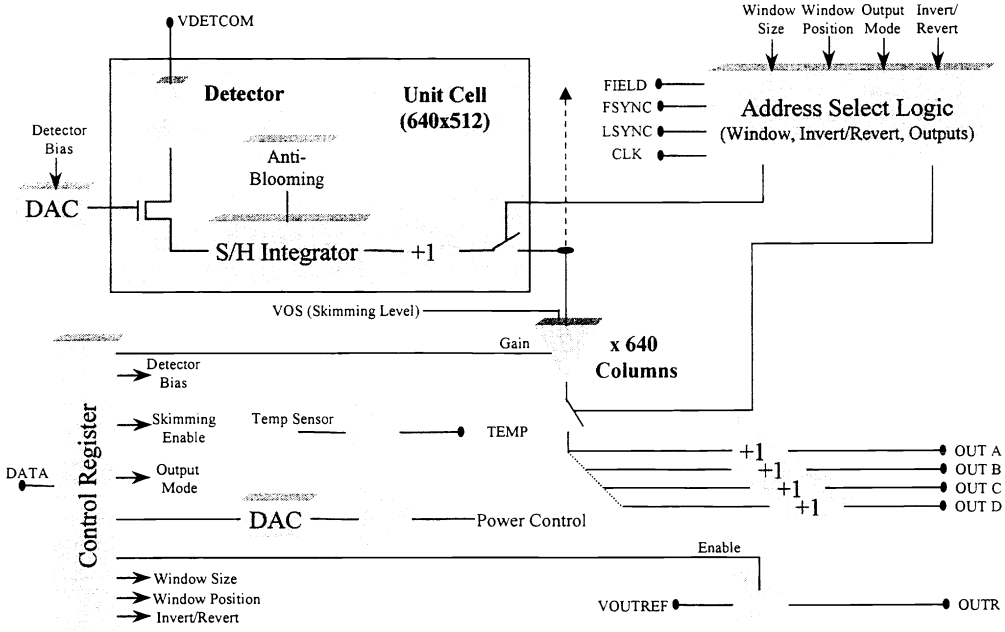

Figure 3 - Standard 640 Block diagram for Command Mode Operation

4. UNIT CELL

The Standard 640 uses a direct injection input circuit as shown in figure 4. Detector current flows through the input gate transistor and charges up the integration capacitor. The anti bloom gate keeps the input circuit from saturating. The voltage on the integration capacitor is sampled and multiplexed to the column amplifier. The detector bias voltage may be either

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controlled by a control register DAC in Command Mode or by applying a bias on the Vdet_adj pad when in Default mode. The approximate relationship between the Vdet_adj input and the detector bias is shown in Figure 5. The detector bias is also adjustable using the serial control interface. Adjusting the detector bias this way provides approximately 5 mV per count.

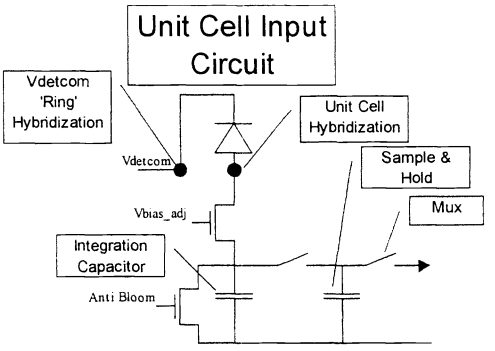

Figure 4 - Simplified Schematic of Standard 640 Unit Cell

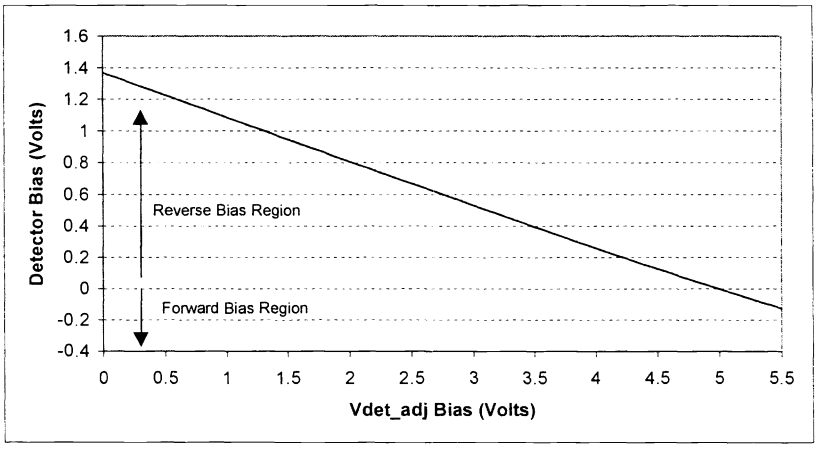

Figure 5 - Default Mode Detector Bias Adjustment Using Vdet_adj Bias.

5. COLUMN AMPLIFIER

The column amplifier shown in Figure 6 functions as a sample/hold, amplifier, and skimmer. The signal from the unit cell is sampled and held onto the column amplifier. The amplifier gain is controlled by the Gain0 and Gain1 pins when in default mode or by providing gain data to the serial control register when in command mode. The relative gain is adjustable form 1 to approximately 4. A global offset function (also known as skimming) is implemented with the column amplifier and is available in the default mode. To operate skimming, the Vos pad is biased to a voltage greater than the voltage on Vref pad. The voltage range for Vos is Vref to Vpos which corresponds to offsetting from 0 to 100% of full well. To disable skimming in the default mode, the Vos pad is tied to the Vref pad. In the command mode, the skimming function is disabled by setting the OE bit in the control register to 0. The column amplifier is also used to drive the output multiplexer bus.

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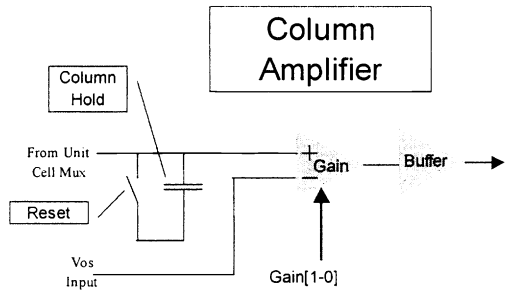

Figure 6 - Column Amplifier Block Diagram

6. OUTPUT BUFFERS AND MULTIPLEXER

The ISC9803 may be run using from one to four outputs. A reference output can also be enabled (not shown in figure). Routing of a given column amplifier to a given output buffer is accomplished through the output multiplexer. The maximum output data rate supported for full frame operation is 12.3MHz.

7. ASSOCIATING PIXEL WITH OUTPUTS & IMAGE TRANSPOSITION

The output selected for a given pixel is determined by the output mode selected. The Standard 640 supports one output, two outputs, and four outputs with or without an output reference. In order to invoke any output mode, other than single output with no reference output, the command register must be used. For single output mode, all pixels are readout through OutA. When using multiple outputs, pixels are assigned to an output, and will be read out through only that output, regardless of the image transposition (invert, revert), and windowing modes selected. Figure 7 illustrates the Standard 640 readout order for single output mode.

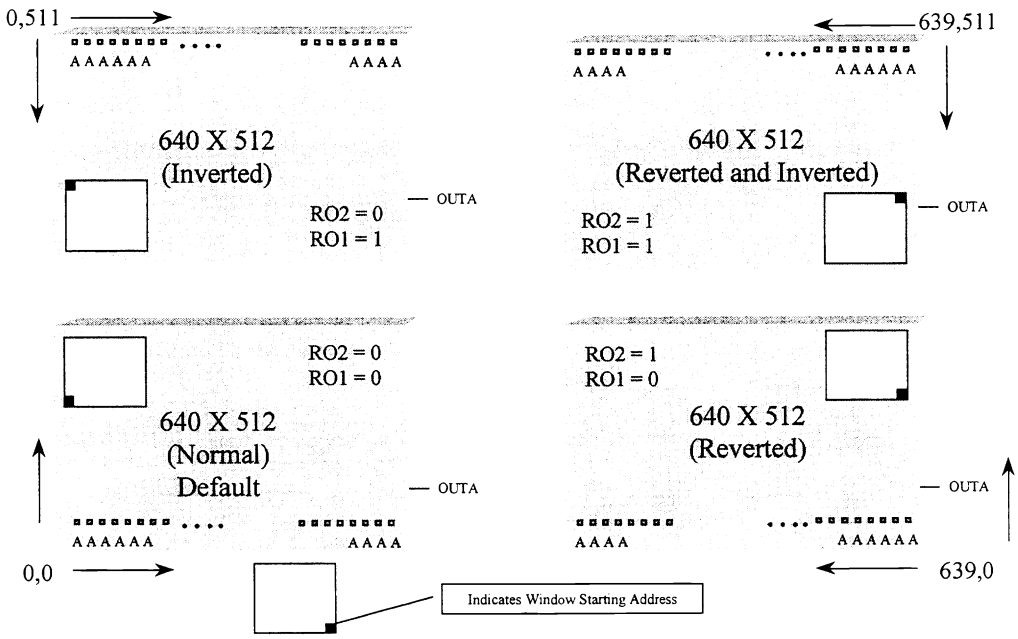

Figure 7 – Single Output Readout Order In Various Command Modes

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The lowest left hand pixel is defined as pixel [0,0] when in default mode. This pixel is the first pixel to be readout in the single output mode using all default settings for invert, revert, windowing, and interlaced non-interlaced modes. This mode of operation would be chosen for a normal 'inverting optic'. Given this type of optic, and by placing the bottom row [row 0] at the 'bottom' of a camera system, a 'normal' raster scan image will be presented.

When the invert/revert bits are programmed RO[2-1]= 01, the image is readout starting from [0,511] and finishes at [639,0]. This mode is shown in the upper left section of the above figure. When the invert revert bits are programmed RO[2-1]= 11, the image is readout starting from [639,511] and finishes at [0,0]. This mode is shown in the upper right section of the above figure. When the invert revert bits are programmed RO[2-1]= 10, the image is readout starting from [o39,0] and finishes at [0,511]. This mode is shown in the lower right section of the above figure.

When two outputs are selected, the first pixel is presented at OutA, and the second pixel is presented at OutB. Alternate pixels are presented at the A and B outputs respectively. See Figure 8.

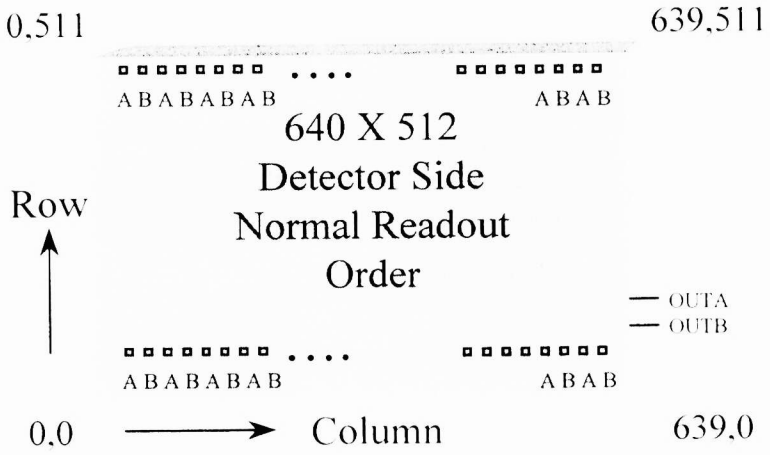

Figure 8 - Two Output Mode – Pixel Vs Output Assignments

When four outputs are selected, the first pixel is presented at OutA, the second pixel is presented at OutB, the third pixel at OutC, and the fourth at OutD. Alternating in four pixel increments, pixels are presented at the A,B,C, and D outputs respectively as shown in Figure 9.

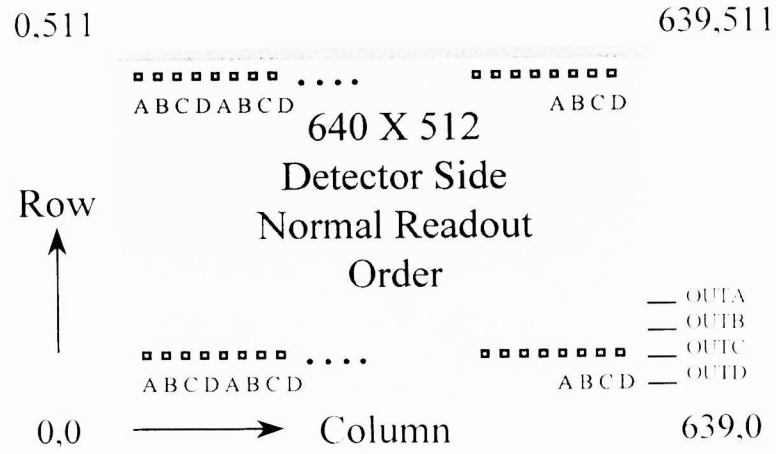

Figure 9 - Four Output Mode – Pixel Vs Output Assignments

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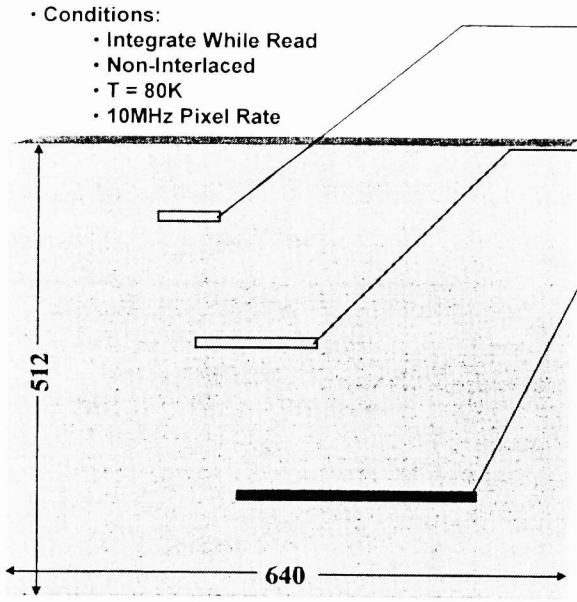
8. WINDOWING

The Standard 640 full window size is 640x512 and is the default window size. To change the window size the chip must be operated in the command mode. The serial control register data bits WAX[7-0] and WAY[6-0] define the column and row start addresses respectively. The data bits WSX[7-0] and WSY[6-0] determine the number of columns in the window and the number of rows in the window respectively. The Figure 10 shows the Standard 640 windowing operation.



Smallest Window in Single Output Mode @ 10MHz @ 80K
32x8 @ 14.16 KFPS

Smallest Window in 2 Output Mode @ 10MHz @ 80K
64x8 @ 14.16 KFPS

Smallest Window in 4 Output Mode @ 10MHz @ 80K
128x8 @ 14.16 KFPS

Output Configuration	Horizontal Resolution of Window Size and Position	Vertical Resolution of Window Size and Position
1 Output	4 Pixels	4 Pixels
2 Outputs	8 Pixels	4 Pixels
4 Outputs	16 Pixels	4 Pixels

Figure 10 – Windowing Mode Summary

9. INTEGRATION MODES

The Standard 640 device features snapshot mode integration, where all pixels integrate simultaneously. The integration process is controlled by the FSYNC clock, and allows both Integrate-While-Read and Integrate-Then-Read modes of operation.

A timing pattern for the Integrated-While-Read operation is shown in Figure 11. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed by a series of LSYNC (LSYNC controls the synchronization of the readout of each individual line) pulses that produce the readout sequence. In this case, the frame time is approximately equal to the readout time for the Standard 640. For this case the integration time occurs during the readout time, allowing for the greatest possible frame rate and integration time duty cycle (where integration time duty cycle = T_{Int} / T_{Frame}) for a given window size.

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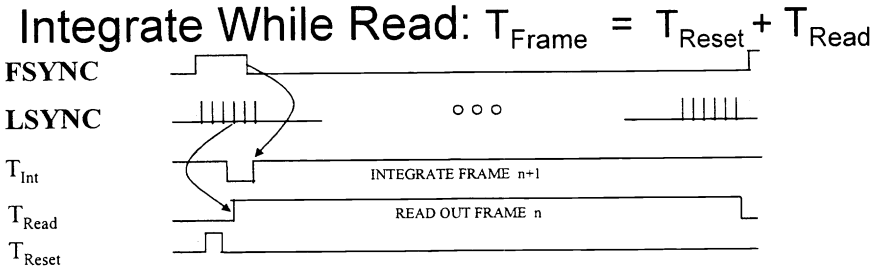

Figure 11 – Integrate-While-Read Timing

Figure 12 shows a timing pattern for operation of the Standard 640 device in the Integrate-Then-Read mode. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed immediately by a sequence of LSYNC pulses that produce a readout sequence. Note that in this case, the FSYNC clock remains high until the readout sequence has been completed. In this case, the integration time occurs after the readout time, resulting in a frame time that is approximately equal to the readout time plus the integration time. This results in a lower maximum frame rate and integration time duty cycle for a given window size.

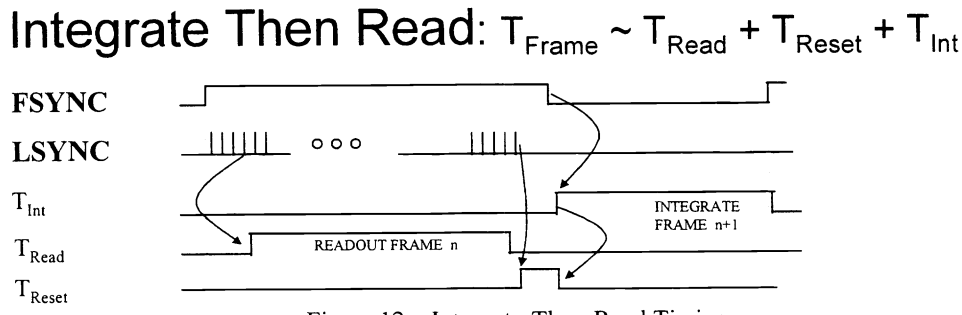

Figure 12 – Integrate-Then-Read Timing

10. OUTPUT RATE AND POWER ADJUSTMENT

Since clock timing and output modes determine the current required to slew and settle internal nodes, power adjustment control is required to allow optimization of operation for the specific application. An adjustment of the on chip master current is also provided to compensate for the temperature of operation.

The ISC9803 powers up in the lowest power, single output, and no output reference mode. Thus, based on the master clock frequency, the power may need to be increased. This setting can be modified by using the serial control register or the Imaster_adj pad for Command Mode and Default Mode respectively.

For applications utilizing the serial control register (Command Mode), programming in a word for the PW(1-0), I(1-0), and PD(0) fields will adjust the internal analog biases. Note that in command mode, the Imstr_adj pad is not connected for 80K operation. The intent of the PW(1-0) field is to provide major current adjustments as required for different clock rate applications. PW(1-0) are inputs to an on chip digital to analog converter (DAC) which adjusts the currents to all analog signal path circuits. When power is applied to the IC, PW(1-0) defaults to (10) which corresponds to the nominal current condition. Programming the PW(1-0) field to (11) will adjust the bias to maximum current condition. The finest bias adjustment resolution with this method of current adjustment is about 1 times minimum current with a maximum adjustment range of approximately 4 times the minimum current. The PD(0) field is provided to adjust the required power based on if a smaller than the 640 default value for the x- direction window is desired. At power up, the PD(0) bit is set to a zero value

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since the default x – direction window is 640. The operator must program PD(0) = 1, if the x-direction window is less than the default value of 640.

Table 1 illustrates the nominal ISC9803 settings for the command mode operation. This table indicates the anticipated settings, target power, and target total Vpos current with respect to the application conditions. The first column indicates the temperature of operation in degrees K. The master clock frequency with units in megahertz is the second column. This is the frequency of the clock applied to the CLK pad. The "# of Outputs" column indicates the number of outputs enabled. The "Reference Output" column indicates if the reference output has been enabled. A "yes" in the "X-Dimension Windowing" column indicates that the x-dimension window value is programmed to less than the default value. The PWR(1-0) column indicates the expected PWR(1-0) field value. Note that for higher frequency operation, the PWR(1-0) field may need to increase to (11). The PD(0) column shows the expected PD(0) field value. Notice that for windowing, PD(0) field must be programmed to a logic one value. The I(1-0) column indicates the expected I(1-0) field value. It should be noted that I(1-0) column values may be revised on a per die basis. The suggested value for the I(1-0) field will be included in the wafer/die test data. The "Imstr_adj Pad" column indicates if the pad needs to be connected (and the bias value) or left open (not connected). For the command mode, Imstr_adj should always be open (not biased) when operating at 80K. The "Min Line Dead Time" column is the minimum required line dead time in master clock cycles. The "Min Output Time" is the minimum output time allowed in master clock cycles for the selected operation mode. The "Power Dissipation" column provides the expected target power dissipation for the selected chip operation mode. The final column indicates the target current for Vpos, for the specific mode of operation.

CONDITIONS					SETTINGS						TARGET VALUES	
Temp (K)	Master Clk (MHz)	# of Outputs	Reference Output	X-Dimension Windowing	PWR(1-0)	PD(0)	I(1-0)	Imstr_Adj Pad (V)	Min Line Dead Time (MC Cycles)	Min. Output Time (MC Cycles)	Power Dissipation (mW)	Total Vpos Current (mA)
300	6.135	1	No	No	(10)	(0)	(11)	NC	45	160	87	15.80
300	6.135	2	No	No	(10)	(0)	(11)	NC	45	160	109	19.80
300	6.135	1	Yes	No	(10)	(0)	(11)	NC	45	160	104	18.90
300	6.135	2	Yes	No	(10)	(0)	(11)	NC	45	160	126	22.90
80	6.135	1	No	No	(10)	(0)	(00)	NC	29	106	87	15.80
80	6.135	2	No	No	(10)	(0)	(00)	NC	29	106	109	19.80
80	6.135	4	No	No	(11)	(0)	(00)	NC	20	80	178	32.30
80	6.135	1	No	Yes	(10)	(1)	(00)	NC	29	26	117	21.30
80	6.135	2	No	Yes	(10)	(1)	(00)	NC	29	26	138	25.00
80	6.135	4	No	Yes	(10)	(1)	(00)	NC	29	26	182	33.00
80	6.135	1	Yes	No	(10)	(0)	(00)	NC	29	106	104	18.90
80	6.135	2	Yes	No	(10)	(0)	(00)	NC	29	106	126	22.90
80	6.135	4	Yes	No	(11)	(0)	(00)	NC	20	80	196	35.70
80	6.135	1	Yes	Yes	(10)	(1)	(00)	NC	29	26	134	24.30
80	6.135	2	Yes	Yes	(10)	(1)	(00)	NC	29	26	155	28.20
80	6.135	4	Yes	Yes	(10)	(1)	(00)	NC	29	26	199	36.10
80	5	1	No	No	(10)	(0)	(00)	NC	23	80	84	15.20
80	5	2	No	No	(10)	(0)	(00)	NC	23	80	105	19.10
80	5	4	No	No	(10)	(0)	(00)	NC	23	80	148	26.90
80	5	1	No	Yes	(11)	(1)	(00)	NC	16	16	140	25.40
80	5	2	No	Yes	(11)	(1)	(00)	NC	16	16	164	29.90
80	5	4	No	Yes	(11)	(1)	(00)	NC	16	16	213	37.20
80	5	1	Yes	No	(10)	(0)	(00)	NC	23	80	100	18.20
80	5	2	Yes	No	(10)	(0)	(00)	NC	23	80	122	22.20
80	5	4	Yes	No	(10)	(0)	(00)	NC	23	80	165	30.00
80	5	1	Yes	Yes	(11)	(1)	(00)	NC	16	16	158	28.80
80	5	2	Yes	Yes	(11)	(1)	(00)	NC	16	16	183	33.20
80	5	4	Yes	Yes	(11)	(1)	(00)	NC	16	16	231	42.00

Table 1 – Nominal Chip Settings for Command Mode Operation.
Note: Power Dissipation and Vpos Current are without Detectors Connected

For applications not utilizing the digital control interface, power adjustment is accomplished by applying a bias to the Imstr_adj pad. The intent of the Imstr_adj bias is to provide power adjustment based on temperature of operation. When power is applied to the IC, the default master current of ~100uA is expected at a temperature of 80K. However, for 300K operation, the Imstr_adj bias is set to 0V. The valid bias adjustment range for Imstr_adj is 0V to 5.5V. An Imstr_adj bias set to 0V corresponds to the maximum current condition. When Imstr_adj bias set to 5.5V, the minimum current condition is realized. The master current adjustment is approximately 20 uA (80K) per volt of adjustment to Imstr_adj bias. The die specific recommended value for Imstr_adj is determined during wafer test and is provided within the wafer test data. Table 2 illustrates the nominal ISC9803 settings for the default mode operation.

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CONDITIONS					SETTINGS						TARGET VALUES	
Temp (K)	Master Clk (MHz)	# of Outputs	Reference Output	X-Dimension Windowing	PWR(1-0)	PD(0)	M(1-0)	Imstr_Adj Pad (V)	Min Line Dead Time (MC Cycles)	Min Output Time (MC Cycles)	Power Dissipation (mW)	Vpos Current (mA)
300	6.135	1	No	No	(10)	(0)	(00)	0	45	320	88	6.80
80	6.135	1	No	No	(10)	(0)	(00)	NC or 2.7	29	212	88	6.80

Table 2 – Nominal Chip Settings for Default Mode Operation.
Note: Power Dissipation and Vpos Current are without Detectors connected.

11.0 WAFER TEST DATA

Each die of the Standard 640 will be rigorously exercised during wafer test. A total of 26 die are contained within each wafer. A color-coded wafer map is produced at the conclusion of testing. All data taken for a wafer map is provided to the customer on a compact disc (CD). Also on the CD is special viewing software, which allows the user to view and print the processed data. For illustrative purposes, the Standard 320 (ISC9705) data is shown in the following discussion. Figure 13 is the test report wafer map for wafer 0018. The green squares are die which have no row or column outages and less than 8 defective pixels. The yield for this wafer is 60% "A" grade die. The red colored squares are die which do not pass the tests. The wafer map is loaded onto the computer screen by the opening the ISC9705.9705 file on the CD. Positioning the screen pointer over a green square (good die) by using the computer mouse and double clicking loads up data menu corresponding to that die as shown in Figure 14. Data such as power, full-scale swing, threshold uniformity, gain, invert/revert, etc, can be accessed. As an example, the MOSFET threshold uniformity test data for die R05C07 is illustrated in Figure 15. This die has a one-sigma threshold distribution on about 4mV.

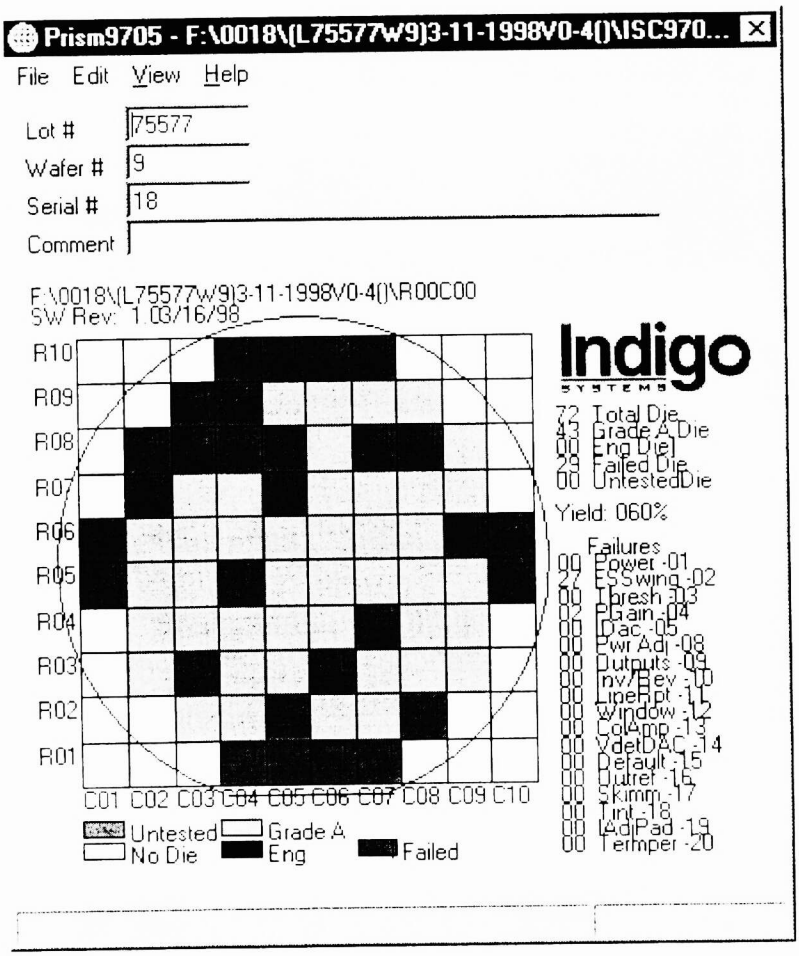

Figure 13 – Test report wafer map for the Standard 320 (ISC9705)

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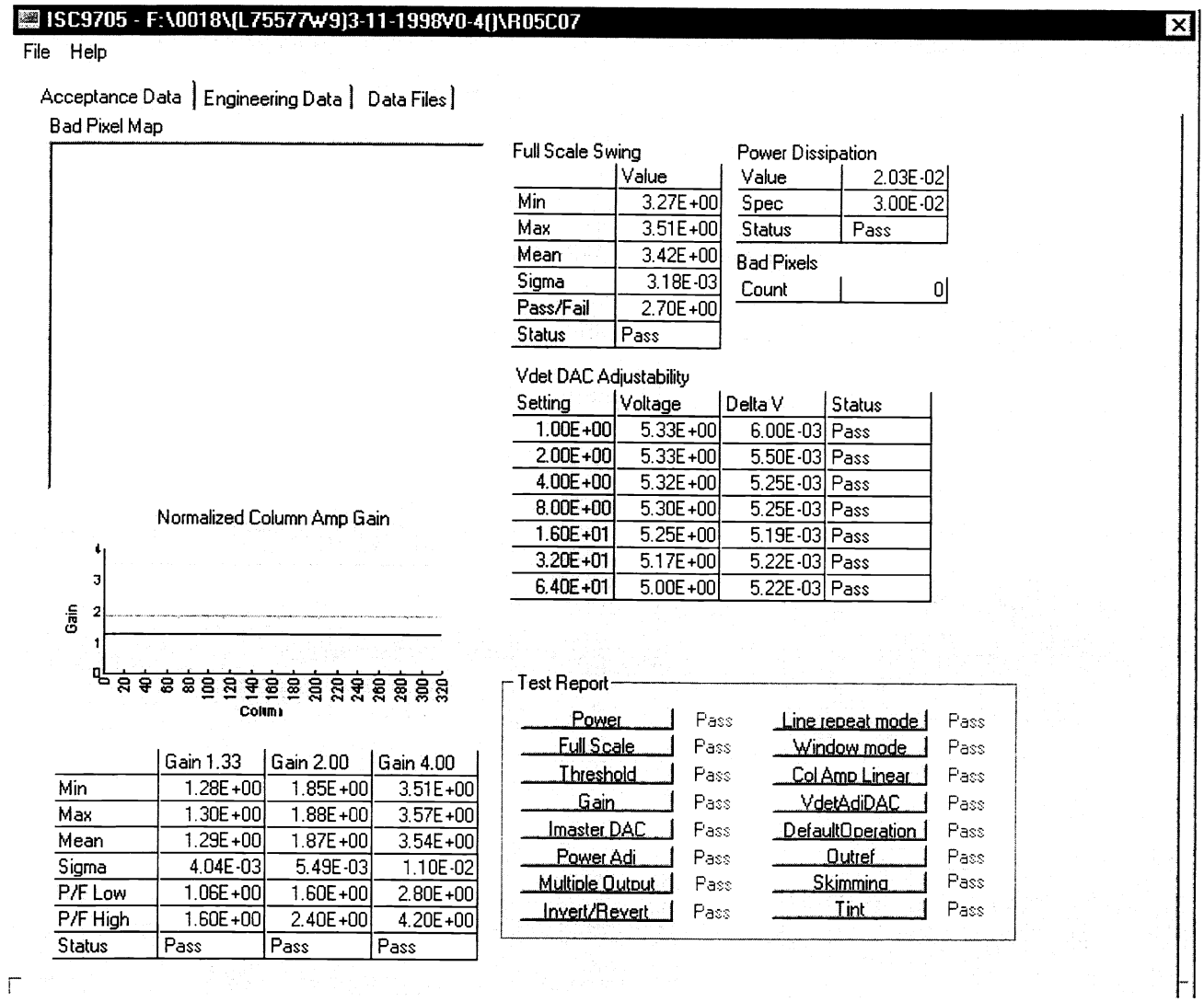

Figure 14 - Data menu for die R05C07 wafer 0018

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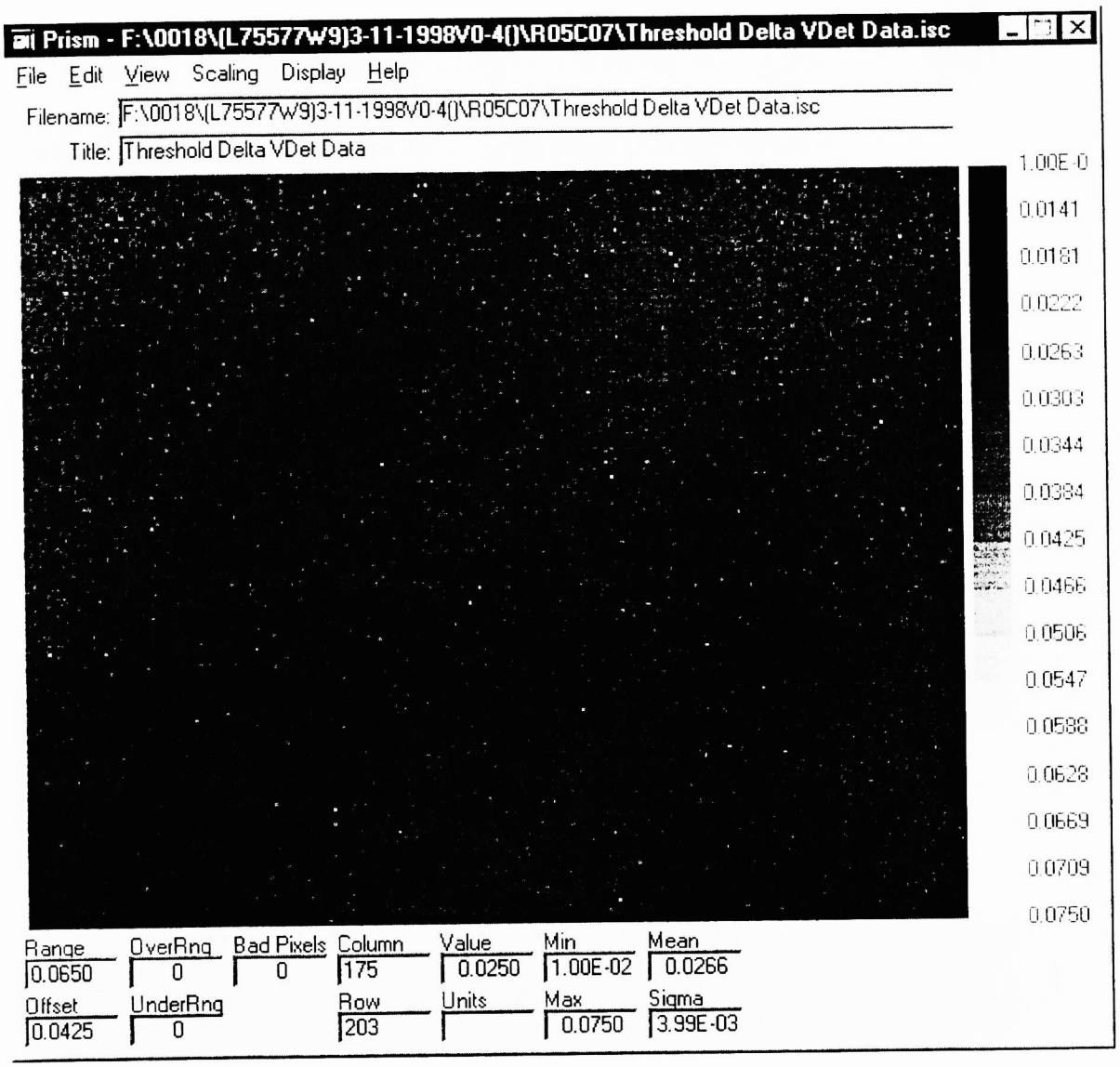

Figure 15 – Threshold uniformity map for die R05C07 wafer 0018

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