



Wafer direct bonding: tailoring adhesion between brittle materials

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Abstract

It is a well-known phenomenon that two solids with sufficiently flat surfaces can stick to each other when brought into intimate contact in ambient air at room temperature. The attraction between the two bodies is primarily mediated through van der Waals forces or hydrogen bonding. Without a subsequent heating step, that type of bonding is reversible. Annealing may increase the energy of adhesion up to the cohesive strength of the materials concerned. The wafer bonding phenomena in brittle materials systems, especially in silicon, is reviewed in the experiment. The focus is on low temperature bonding techniques. The pivotal influence chemical species on the surfaces have on the subsequent type of bonding (van der Waals, hydrogen, covalent bonding, mechanical interlocking) is discussed. Methods of modifying the surface chemistry for tailoring bonding properties are addressed. The paper is aimed at providing an overview of the current understanding of the factors determining the bondability and strength of the bonding obtainable. The authors assess the present state of the experimental methods for determining basic parameters governing the adhesion. A number of examples illustrate the applicability of fusion bonding for as diverse fields as opto-electronics, microsystems technology, and fabrication of advanced substrates like silicon-on-insulator wafers. © 1999 Elsevier Science S.A. All rights reserved.

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1. Introduction

What is wafer direct bonding? If two solids of the same material with clean and flat surfaces are brought into close proximity, attractive forces should pull the two bodies together into intimate contact so that bonds can form across the interface. Two crystals with matching orientation should merge into one crystal with no indication of the former junction, while two misoriented crystals would form a grain boundary at their interface. In the former case the adhesion would be equal to cohesion, in the latter case a similar value would be obtained. Everyday-experience speaks against this scenario and usually it is argued that the bodies can make contact only at some asperities, and even there surface adsorbates would prevent the formation of strong chemical bonds and themselves provide only poor adhesion. Although this interaction suffices to cause friction, it is usually incapable of holding two bodies together. In wafer direct bonding, however, exactly this occurs: two solids with well-polished flat surfaces, when brought into close proximity, spontaneously adhere or ‘bond’ to each other, and once initiated, the bonding will spread by itself across the whole interface. There is no gap at the interface, the two bodies are only an atomic distance apart. The bodies adhere without external force or layer of glue, giving rise to the colloquial reference to wafer direct bonding as ‘gluing without glue’. Wafer direct bonding is also known as ‘wafer bonding’, or ‘direct bonding’. Although in some cases bonding requires external pressure and

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high temperature, ‘fusion bonding’ and ‘bonding by atomic rearrangement’ may be safely subsumed under wafer direct bonding. It is, however, to be distinguished from ‘anodic bonding’ where at elevated temperature and with an electric field applied, metals are joined with sodium-containing glass [1–3].

The adhesion depends on the type of interaction: van der Waals forces, hydrogen bonds or strong chemical bonds of metallic, ionic or covalent nature may mediate the adhesion. A discussion of forces acting at surfaces can be found, for example, in the monograph by Israelachvili and the references to earlier studies at Cambridge therein [4]. Usually in wafer direct bonding, the attraction between the two bodies primarily is seen as a result of van der Waals forces or hydrogen bonds. This type of bonding is reversible provided no subsequent heat treatment has been performed. To show that recent progress in wafer direct bonding permits attaining the full range of attractive interaction through judicious adjustment of the bonding conditions is one of the aims of the current review. Irrespective of composition or internal structure, no matter whether the material is monocrystalline, polycrystalline or amorphous, and no matter whether the material is of a single phase or a composite of several, all materials may be expected to be directly bondable to each other provided the surfaces meet the requirements in smoothness, flatness and cleanliness. In the case of malleable materials mutual conformity can be brought about by plastic deformations; here, however, the focus will be almost exclusively on the brittle materials which allow only elastic distortions.

Although perhaps unexpected from the perspective of common experience, the phenomenon of direct bonding is not new as will be shown in the brief section on its history. The requirements imposed on the surface of materials to make them directly bondable and the procedures generally practised for bonding will be listed in a separate chapter. Methods to judge the quality of bonding or to unravel the intricate interfacial chemistry will be introduced in the section on “Examination of bonding quality”. The system studied best is silicon bonding, and in “Silicon direct bonding” the scope in interfacial adhesion engineering attained in recent years can be shown paradigmatically. “Other materials” treats a variety of other systems of interest, and treating an economically important combination not in a separate chapter is not to deny its importance, it only reflects the dearth of published knowledge on the underlying bonding chemistry. “Electronic properties” deals with silicon and with III–V compound semiconductor bonding. “Examples of applications” mainly aims at giving a flavour of the variety of situations where bonding has established itself as the method of choice or where bonding has been suggested.

In view of the large number of articles published on wafer direct bonding, this review aims not to provide an exhaustive bibliography; instead the reader is referred to a dedicated issue of Philips Journal of Research [5], to topical conference proceedings [6–9], recent reviews [10–21] and to the book by Tong and Gösele on that subject [22]. The adhesion phenomenon is not always wanted. Although closely related, avoidance of bonding is not explicitly covered in the present article, as recent reviews treat stiction in microelectromechanical systems [23–26].

2. History of wafer bonding

Although wafer direct bonding has only recently been added to the toolbox of microelectronics and microsystem technology, the basic phenomenon has been known and used for many centuries. The developments leading to present-day wafer bonding were reviewed, for example by Gösele and Stenzel [27]; Haisma reviewed its history in the patent literature [28]. Additional information on early patents may be found for instance in Ref. [18].

Around 1230–1240 the Franciscan friar Bartholomaeus Anglicus, for instance, one of the medieval encyclopaedists digesting and compiling other sources, stressed the importance of cleanliness when joining silver and gold [29]:

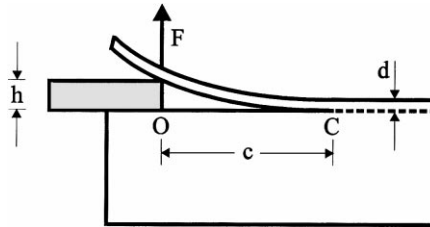


Fig. 2. Schematic set-up of Obreimoff's famous splitting experiment on mica. A wedge of thickness h was inserted to cleave off a lamella of thickness d .

industry learnt to polish glass to optical quality, duly stiction between glass pieces was observed and termed 'ansprengen' by German craftsmen [35], and in analogy, 'wringing on', 'wringing into contact' or simply 'to spring' [28,35]. Similarly, optically polished metallic precision measurement length scales known as 'end pieces' were found to adhere to each other. Often, the adherence then was just a nuisance. The phenomenon had become so commonplace that by 1930 Obreimoff started his report on the surface energy of mica with a reference to glass put in optical contact, stated that the analogue can be observed when two freshly split mica foils are put together, and then posed the question he was going to answer in the paper: whether one needs to apply the same force to split two mica sheets placed in optical contact as to split a fresh one [36]. To measure the fracture surface energy of mica, he used the arrangement schematically shown in Fig. 2. A glass wedge of thickness h was inserted at the bonding interface between a mica lamina of thickness d and the parent block of which it had been cleaved. Obreimoff found that the surface energy decreased dramatically, from 5.0 J m^{-2} (corrected for an error in his formula) for mica split in vacuo to 0.38 J m^{-2} for mica split in ambient atmosphere. For 'bonded' mica the surface energy approached the value of mica in air.

In 1936, Robert John Strutt, fourth Baron Rayleigh (1875–1947), reported probably the first thorough scientific study of room temperature adherence between glass slides [37]. Evaluating the reflective properties of the room temperature bond interface, he arrived at an average separation between the bonded glass plates of ca. $10\text{--}30 \text{ \AA}$ which did not decrease when the samples were pressed together. However, from his comparison with bonded samples annealed short of the softening point, an atomically small separation between the bonding surfaces may be inferred. The adhesion between room temperature bonded silica pieces was quantified by measurements of tensile strength and 'work of stripping' or bond energy. For the latter he developed a chevron-type double cantilever beam test, schematically shown in Fig. 3, which yielded a fracture surface energy of 71 erg cm^{-2} , in the range of modern observations. He noted that upon re-contacting only about half

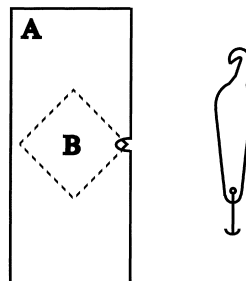


Fig. 3. Lord Raleigh's set-up for measuring the 'work of stripping'. A square piece of glass (B) was bonded under a rectangular glass piece (A) such that a corner of the square was positioned under the notch cut into the rectangle. With the aid of the hook, weights were added to induce debonding [37].

the work of stripping was recovered; the factors causing the irreversibility have not yet been analysed. His comprehensive account could have been a seminal paper on wafer bonding; however, scientifically and technologically it was rather inconsequential and not even his biographer did make much of the work's potential [38].

During the following decades, direct bonding found only occasional entry into the scientific literature, mostly as a specialised joining technique. At Philips Research Laboratories, He–Ne gas lasers were fabricated with the mirrors bonded to the body of fused silica [28], shown in the photograph of Fig. 4 [39]. At least for the thousands of hours of laser operation, room temperature bonding proved to form a vacuum-tight seal [40]. Antypas and Edgecombe probably were the first to utilise direct bonding as a tool for the transfer of epitaxial layers [41]. For the fabrication of a transmission photocathode, they bonded at elevated temperatures a GaAs/AlGaAs bilayer grown epitaxially on a GaAs substrate onto a glass substrate. The AlGaAs layer served as etch-stop during the chemical removal of the GaAs substrate. The epitaxial-layer-transfer concept has only recently found more wide-spread application, for instance in the form of epitaxial lift-off [42]. Together with some later work by Liao and Mull [43], the report by Antypas and Edgecombe [41] sometimes is seen as the inception of wafer bonding in the field of III–V compound semiconductors.

In spite of the long history of the direct bonding phenomenon, the modern development of the science and technology of wafer bonding only was stirred by two reports in the mid-eighties [44,45].

The driving force behind the first report was the quest for a silicon-on-insulator fabrication process yielding device layers of a quality equivalent to bulk wafers. Most electronic devices require only a small fraction of the thickness of a standard wafer. Isolating the thin device layer electrically from the mechanical support of the ‘handle wafer’ offers a number of advantages. Originally, the radiation hardness resulting from the greatly reduced sensitivity to electron-hole pairs generated by radiation was perceived, particularly for military applications, as the main benefit. Meanwhile, the reduction in operating voltage, the integrability of high and low voltage devices and the increased packing densities possible turned out as the advantages of commercial import. To demonstrate a novel route to such a SOI-substrate, Lasky bonded a thermally oxidised wafer to a handle wafer. Before chemically thinning the oxidised wafer to leave a thin monocrystalline layer on top of the oxide, the room temperature bond was strengthened at temperatures between 700°C and 1050°C [45].

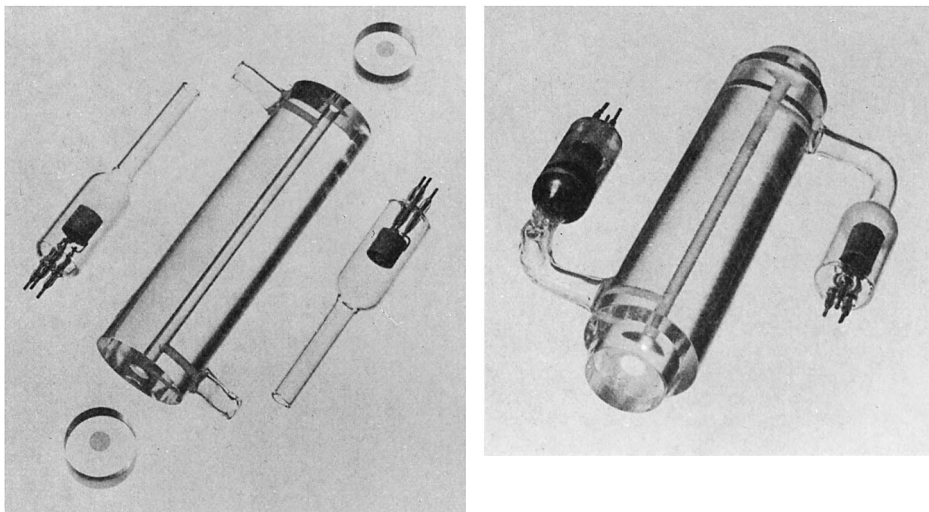


Fig. 4. The short, stable plane-mirror He–Ne gas laser represents probably the first industrial application of direct bonding [28]. The reflecting mirrors and the body of fused silica were ‘wrung together’ [39].

In the second report, Shimbo et al. tried to substitute deep dopant diffusion and the growth of thick epitaxial layers in the processing of devices by a wafer bonding step. Wafers covered with a native oxide were contacted at room temperature; the thus bonded pair was annealed at 1000–1100°C to induce covalent bonding and to dissolve the oxide interlayer [44].

Finally, wafer bonding was seen as a solution to a variety of problems in microelectronics and microsystems technologies, and thus the reports could spark a new field in materials science and revitalise an old joining technique.

3. Bonding requirements and procedure

3.1. Introduction

Wafer bonding puts very high demands on the surfaces to be mated with regard to their flatness, smoothness as well as their cleanliness. In this chapter the requirements which have to be fulfilled to ensure a high bonding yield will be discussed.

Wafer bonding requires surfaces free of contaminants. The contamination which play an important role in wafer bonding can be classified as (a) particle contamination (like dust, hair, fibres), (b) organic contamination (hydrocarbons from the air, plasticisers from wafer boxes) and (c) ionic contamination (metal ions from metal tweezers or glass containers).

Of all these sources of contamination, particles present on the wafer surface before bonding pose the most obvious problem in wafer bonding. Because they act as spacers, particles inhibit the interaction between opposing surface species. As a consequence unbonded areas result which are often many times larger than the particle itself. A particle with a diameter of 1 µm trapped in the interface between two standard 100 mm wafers may lead to an unbonded area with a diameter of 1 cm. Organic contaminants usually do not lead to unbonded areas during room temperature bonding because they are present on the surface as single molecules or as a film and thus do not greatly affect the surface roughness. The contamination film, however, adheres only weakly to the substrate and therefore may limit the adhesion ultimately achievable. In addition organic contaminants are thought to be responsible for the nucleation of interface bubbles during annealing. Like organic contamination metallic ions do not inhibit the bonding at room temperature. Even during annealing such contaminants do not affect the adhesion. Depending on the application trace metal contamination may not present problems at all. However, for electronic applications they may be harmful since they can affect the electronic properties of the semiconductor material.

Fig. 5 schematically illustrates the adsorbate layers commonly found on a hydrophilic substrate surface.

3.2. Cleaning of silicon surfaces

To obtain high quality interfaces it is important to remove all these sources of contamination before bonding. Fortunately, the cleaning procedures commonly used in semiconductor industry are fully compatible with wafer bonding. They are able to remove the surface contamination without degrading the wafer surface. In the following we will limit the discussion of cleaning procedures to silicon surfaces.

When bonding other materials cleaning methods compatible with these materials have to be adopted, always keeping in mind that contaminants have to be removed without degrading the surface.

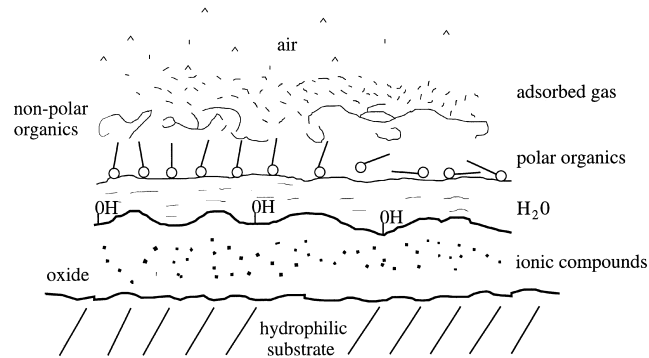


Fig. 5. Schematic illustration of the adsorbate layers commonly expected on hydrophilic surfaces.

Frequently used in semiconductor processing of silicon as well as in wafer bonding is the hydrogen peroxide based RCA wet cleaning procedure. It basically involves two steps: RCA 1 ($\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O} = 1 : 1 : 5$; also referred to as SC 1 or SE 1) and RCA 2 ($\text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O} = 1 : 1 : 6$; also referred to as SC 2 or SE 2) [46]. Other cleaning procedures commonly employed are a mixture of hydrogen peroxide and sulphuric acid ($1 : 4$ or $1 : 2$) or concentrated nitric acid [46]. It has been reported that a mixture of H_2SO_4 and H_2O_2 combined with a small amount of hydrofluoric acid leads to a very thin and smooth native oxide layer useful for wafer bonding [47]. The hydrophilicity of wafer surfaces which underwent different pre-treatments as well as the long-term stability of a clean surface have been investigated by contact angle measurements [48,49]. For the removal of hydrocarbons from the silicon wafer surface a treatment with periodic acid dihydrate ($\text{HIO}_4 \cdot 2\text{H}_2\text{O}$) has been recommended [50].

Since the native oxide can act as a trap for metallic and organic contamination it is frequently removed from the wafer by a dip in diluted hydrofluoric acid or buffered ammonium fluoride solution. Afterwards, the wafer is treated with one of the cleaning solutions mentioned above to form a new, clean native oxide on the wafer surface. Care has to be taken as ammonia (present in RCA 1) attacks bare silicon thereby increasing the microroughness considerably [51]. To prevent this from happening, it has been suggested to decrease the ratio of NH_4OH in the RCA 1 mixture to 0.05–0.25 if bare silicon surfaces are present. Besides the wet cleaning technology which is still the working horse in semiconductor cleaning, there is a growing interest in dry wafer cleaning methods. Dry cleaning procedures commonly employed before the bonding include UV/ozone cleaning [46,52] as well as various plasma treatments [46,48].

Due to the aggressive nature of the agents used in wet cleaning and unsolved problems regarding their disposal it is likely that in the future dry cleaning methods will become increasingly important also in wafer bonding technology.

For the bonding of hydrophobic silicon surfaces the wafers are first cleaned using the wet or dry cleaning methods mentioned above. Afterwards the oxide is etched away in hydrogen fluoride or ammonium fluoride solution. Care has to be taken since hydrophobic silicon surfaces tend to get contaminated by organic compounds even more readily than hydrophilic surfaces [53].

3.3. Flatness and smoothness

The surface flatness is a macroscopic measure which is defined as the deviation of the front wafer surface from a specified reference plane while the back wafer surface is considered being ideally flat. Typically the total thickness variation (TTV) is used to quantify the flatness of a wafer. It

is defined as the difference between the highest and lowest elevation of the top surface of the wafer. During the bonding at room temperature each wafer has to be deformed in order to achieve conformity [54]. X-ray topography (XRT) can be used to image the strain pattern which relate to the flatness nonuniformity of the bonded wafers (see also chapter 4). The strain contrast in XRT-images of room temperature bonded samples do not differ from the contrast found for wafers bonded at elevated temperature. This indicates that most of the deformation occurs already at the room temperature bonding step. Maszara et al. estimated the local stress caused when wafers elastically deform on the mutual surface adaptation [54].

Two sufficiently smooth wafers will spontaneously bond at room temperature despite a flatness variation of a few micrometres. However, if the flatness variations are too large, unbonded areas result. Gösele et al. have theoretically investigated the conditions under which a gap which separates two wafers will prevent bonding [17,55–57]. Recently, a more comprehensive analysis has been undertaken which essentially bears out the previous results [58]. If the gaps are caused by flatness non-uniformities with the lateral extension R much larger than the gap height h the condition for a closing of the gap depends on the ratio of R to the wafer thickness t_w . For $R > 2t_w$ (Fig. 6(a)) the gap will close if:

$$h < \frac{R^2}{\sqrt{\frac{2E't_w^3}{3\gamma}}}, \quad (1)$$

with $E' = E/(1 - \nu^2)$, E being Young's modulus, ν Poisson's ratio, and γ the surface energy. In cases where $R < 2t_w$ (Fig. 6(b)) the condition for gap closing is independent of the wafer thickness and is given by

$$h < 3.6(R\gamma/E')^{1/2}. \quad (2)$$

When bonding wafers of different thickness the equations become more complex [17,56]. In general, the thinner wafer determines the bonding behaviour (for equal E). Fig. 7 shows the region of gap closing for two silicon wafers of equal thickness for $\gamma = 100 \text{ mJ m}^{-2}$. These theoretical considerations indicate that even pieces with infinite thickness can be bonded provided that they possess the required flatness [57,59]. For silicon pieces thicker than about 3 mm the conventional semiconductor polishing method does not produce the necessary flatness anymore. For such materials optical polishing has to be applied [57,59]. Two 20 mm thick silicon pieces bond to each other after being optically polished down to a surface flatness variation of a 10th of a wavelength (about 63 nm) [57].

Commercially available prime grade 4 in. silicon wafers of the usual thickness (0.5 mm) exhibit a flatness variation of 1–3 μm . Variations of this order can be easily accommodated through mutual deformation of the wafers. Bow and warpage up to 25 μm pose no obstacle to bonding.

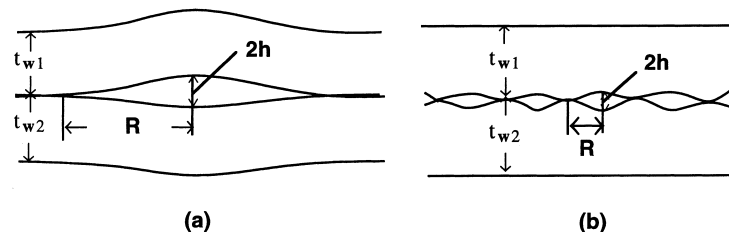


Fig. 6. Schematic drawing of a gap caused by flatness non-uniformities [17,56]: (a) $R > 2t_w$; (b) $R < 2t_w$.

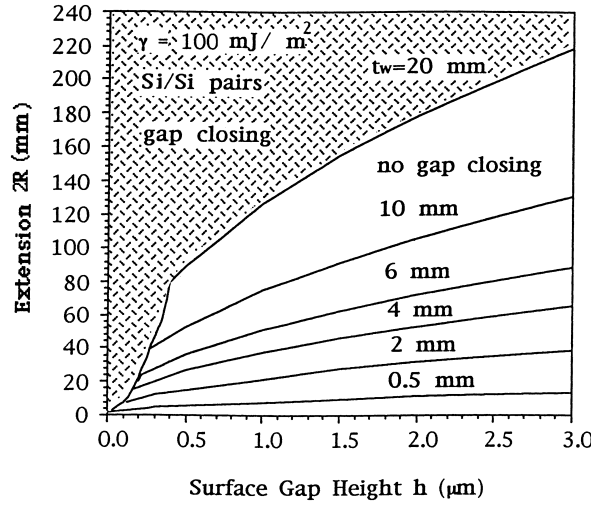


Fig. 7. Parameter combinations of gap height h and lateral extension R of gaps which can be closed for silicon wafers with a thickness of $525 \mu\text{m}$ and a surface energy of 100 mJ m^{-2} . The area in which a closing of the gap can occur is shaded [17,56].

Besides the flatness of a surface, its smoothness usually quantified as microroughness, is crucial for wafer bonding. The microroughness is a local microscopic parameter relating to the wafer surface roughness in very small wavelengths. If the microroughness exceeds a critical value the wafers are not bondable anymore. A model which describes the relation between bondability and surface morphology has been derived by Gui et al. [60]. They consider the elastic contact between a nominally flat, but rough surface and a nominally flat smooth surface. The roughness of the former is caused by a random series of asperities with spherical caps with a constant radius β and a Gaussian height distribution. The adhesion parameter $1/\Delta_c$ which is defined as the ratio of the standard deviation of the distribution of asperity heights σ to the extension which an asperity can sustain before the adhesion is lost has been derived by Fuller and Tabor [61]:

$$\frac{1}{\Delta_c} = 0.513 \frac{\sigma}{\beta^{1/3}} \left\{ \frac{K_E}{\Delta\gamma} \right\}^{\frac{2}{3}}. \quad (3)$$

K_E is the elastic constant which is defined by the following formula:

$$K_E = \frac{4}{3} \left\{ \frac{1 - \nu_1^2}{E_1} + \frac{1 - \nu_2^2}{E_2} \right\}^{-1}, \quad (4)$$

where ν_1 and ν_2 are the Poisson's ratios and E_1 and E_2 Young's moduli of the two materials. Fuller and Tabor have derived the relation between the relative pull-off force of the contacted interface and adhesion parameters [61]. If $1/\Delta_c > 3$ no force is needed to separate the materials. For known material properties and surface adhesion force the surface roughness at which bonding will become impossible can be calculated. For hydrophilic silicon wafers with $\gamma = 100 \text{ mJ m}^{-2}$ and a mean radius of the surface asperities of $100 \mu\text{m}$ bonding would occur if the standard deviation of the asperity heights is less than 2 nm .

In practice hydrophilic silicon wafers will bond spontaneously to each other via hydrogen bonds if the microroughness characterised by a value such as root mean square (rms) roughness is less than 0.5 nm . Commercially available prime grade polished silicon wafers exhibit a rms roughness in the

Ångstrom range. Unstructured silicon wafers with standard thickness thus are bondable without any problems. The low rms roughness of silicon wafers are without any doubt related to the ever improved polishing techniques developed in the last decades. The last and most important step in the polishing of wafers in terms of surface smoothness is the chemo-mechanical polishing (CMP). It is this final polishing step which produces extremely smooth surfaces crucial for void-free wafer bonding [62]. Besides being used as final step in the production of prime grade silicon wafers, CMP can be employed for preconditioning of surfaces. It is applied just prior to using the wafers and activates the wafer surface by removing the uppermost few nanometres of the material. CMP preconditioning yields an activated surface free of contamination [62]. Finally CMP is used to planarise patterned or structured wafers before a wafer bonding step. Particularly when fabricating micromechanical devices a final CMP step may be necessary before bonding the patterned and structured wafers. The deposition of a thin CVD oxide followed by CMP has been used to form a flat layer on the surface of a processed VLSI bulk silicon wafer. The patterned substrates which were not bondable due to a lack in surface quality were first planarised by depositing an oxide via plasma enhanced chemical vapour deposition utilising tetraethoxy silane (TEOS) as precursor. The surfaces produced subsequently underwent CMP yielding rms roughness of less than 0.5 nm [63]. Spontaneous bonding was observed upon contact with bare silicon wafers.

High quality surfaces suitable for direct bonding also have been achieved via CMP of polycrystalline silicon [60,64], silicon dioxide [60,62] and silicon nitride [60,65,66].

3.4. The bonding procedure

To minimise re-contamination of the wafer surfaces bonding should be conducted directly after cleaning. A clean environment is absolutely necessary to ensure a high bonding yield. Thus, bonding is usually carried out in a high quality cleanroom. Typically a class 10, or better class 1, cleanroom is chosen for bonding. However, even in this clean environment bubbles caused by particulates may be detected. Furthermore, as cleanroom atmospheres are usually places of high hydrocarbon concentrations organic compounds may readily adsorb onto the clean surfaces.

The bonding is carried out either manually or by making use of a commercial bonder. The latter is particularly useful if the wafers have to be aligned before bonding. The room temperature bonding step may be carried out in air or in a different atmosphere such as oxygen, nitrogen or argon. Besides bonding under normal pressure, the bonding under reduced pressure has attracted interest. It offers certain advantages which will be discussed in chapter 5. The bonding at room temperature usually is reversible (with the exception of UHV-bonding, chapter 5).

For research purposes and low budget production a bonding apparatus which can be used outside a cleanroom facility has been developed [67,68]. This so-called micro-cleanroom is based on the spin-coater concept with some additional features (Fig. 8). After wet or dry cleaning, two wafers are placed in the micro-cleanroom so that the mirror-polished sides face each other. They are separated from each other by removable spacers. The space between the two wafers is then thoroughly flushed with particle-free, deionised water. After the rinsing a lid is put over the wafers and they are spin-dried. The drying can be enhanced by heating the wafers using an IR lamp. Finally, the spacers are removed without opening the lid. The upper wafer drops onto the lower one. If the bonding is carried out in air the wafers usually float on each other due to a thin air cushion between them. By locally pressing them gently together so as to squeeze out the air bonding is initiated. The bonding then propagates by itself. In general, the bonding should be started at only one location since an initiation of the bonding simultaneously on different locations may cause the trapping of air bubbles.

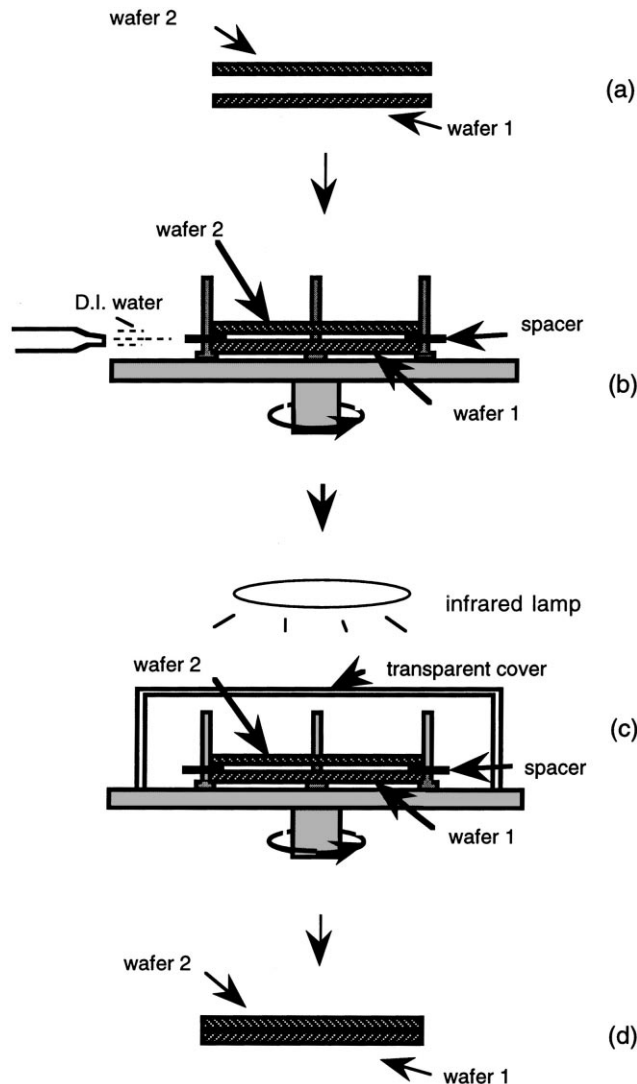


Fig. 8. Schematic drawing of the micro-cleanroom [67,68].

Within a few seconds the bonded area spreads over the entire wafer surface, particularly when bonding hydrophilic silicon surfaces. The bonding between two hydrophilic 4 in. Si wafers as observed with an IR camera is shown in a sequence of photographs in Fig. 9. The velocity of the contact wave has been studied. Stengl et al. [69] have investigated the bonding velocity of hydrophilic silicon surfaces as a function of temperature. They report a decrease in bonding speed with increasing temperature reaching zero at about 200°C. This behaviour is attributed to the enhanced desorption of water molecules at elevated temperature which are involved in the formation of hydrogen bonds across the interface. Haisma et al. reported an increase in bonding velocity with an increasing pH of the solutions used for surface treatments prior to bonding. They related the increase in bonding speed to a higher fracture surface energy [16]. However, Cha showed that wafers covered with a thin film of protein molecules exhibit an exceedingly low bonding speed while at the same time the fracture surface energy is in the range expected for van der Waals interaction [70]. This indicates that a low bonding velocity does not necessarily relate to a low fracture surface

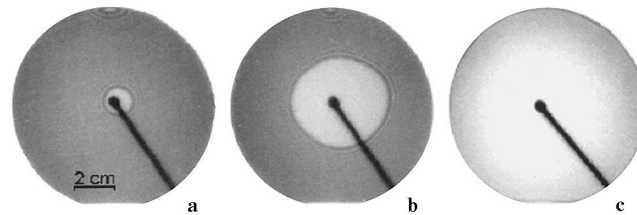


Fig. 9. Sequence of photographs taken with an infrared-sensitive camera, showing the propagation of the bonded area.

energy. Bengston et al. investigated the dependence of the bonding velocity on the wafer thickness [71]. Thicker wafers are less deformable and thus the bonded area spreads slower when thicker wafers are involved [71]. However, when using wafers of identical surface quality, no dependence on thickness could be observed. Instead the contact wave velocity was found to depend on the gas pressure in the interface [72]. The authors carry out bonding experiments at ambient pressure and under reduced pressure. The bonding velocity increases with decreasing pressure. The authors conclude that the bonding speed is determined by pressing the gas out of a localised area just in front of the propagating bonding front [72].

Bonding has also been carried out by contacting the wafers under ultra-pure water leaving a water film which is much thicker than the commonly observed few monolayers of water in the interface [73–75]. If the wafer pair is stored at slightly elevated temperatures under vacuum the water slowly diffuses laterally out of the interface.

3.5. Interface bubbles

One problem frequently associated with wafer bonding is the formation of interface bubbles, sometimes referred to as voids. In principle there are two different kind of interface bubbles: (a) bubbles which occur in the as-bonded interface at room temperature and (b) bubbles which are generated at elevated temperatures (typically at 200–800°C).

The first type is usually caused by surface irregularities, particulates or trapped air. Trapped air can be avoided by initiating the bonding in the centre of the wafer pair or bonding in vacuo. Particles cause unbonded areas as they prevent the wafers from making close contact. The wafers are deformed around the particle upon bonding. The resulting bubbles or circular unbonded interface areas are quite large compared to the actual size of the particle. Tong et al. have investigated the bubble diameter as a function of the size of a particle trapped between two wafers [17,56].

In Fig. 10 the deformation caused by a particle trapped in the interface is shown schematically. In Fig. 10(a) the radius h (or height $H = 2h$) of the particle is much smaller than the radius R of the unbonded area resulting and much smaller than the wafer thickness t_w . Using the simple theory of

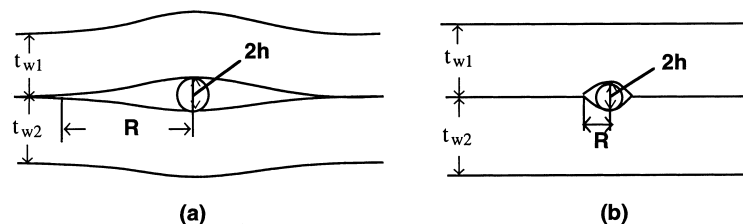


Fig. 10. Schematic drawing of a particle leading to an unbonded area [17,56]. (a) Unbonded area with a radius R larger than the wafer thickness t_w ; (b) with a radius, R , smaller than the wafer thickness, t_w .

small elastic deflection of a thin plate, R can be calculated from Eq. (5) by assuming that the particle is incompressible [17,56]:

$$R = [2/3E't_w^3/\gamma]^{1/4}h^{1/2} \quad (5)$$

(γ = surface energy of each wafer when partially debonded, $E' = E/(1 - \nu^2)$ with E denoting Young's modulus and ν Poisson's ratio).

For two wafers of different thickness more complex equations result [17,56].

It can be easily derived from Eq. (5) that even a relatively small particle will result into a large unbonded area. For example a particle of diameter 0.5 μm trapped between two 4 in. silicon wafers each with a thickness of 525 μm will yield an unbonded area of approximately 0.5 cm radius. Since compared to thick wafers thinner wafers are more easily deformable a reduction in wafer thickness leads to a considerable decrease of unbonded area. Moreover, for very small particles with a radius below a critical radius h_{crit} given by

$$h_{\text{crit}} = 5(t_w\gamma/E')^{1/2}, \quad (6)$$

the resulting unbonded area is very small (Fig. 10(b)). This behaviour is thought to be due to an elasto-mechanical instability occurring under these conditions [17,56]. For a 4 in. silicon wafer pair a critical height, h_{crit} , in the order of 100 nm was anticipated, i.e. a particle of this size trapped in the interface would cause an unbonded area only with a radius in the same order (100 nm). For a study of the crack length as a function of asperity height, a wafer with photolithographically defined steps of down to 9 nm height was bonded against a plane wafer and subsequently examined using high-voltage electron microscopy [76,77]. Fig. 11(a) shows the long crack in the wake of a 18 nm step. The presently available results of step-structures (Fig. 11(b)) cannot validate the elasto-mechanical instability which had been hypothesised in Refs. [17,56] for the case of spherical particles.

In conclusion, bubbles or unbonded areas in the interface of as-bonded wafers at room temperature can be avoided by:

- bonding sufficiently flat wafers,
- joining clean surfaces in a particle-free environment,
- avoiding the trapping of air.

In addition to the bubbles which are observed at room temperature, unbonded areas may be generated during storage or annealing. In the interface of hydrophilic silicon pairs the bubbles are formed at temperatures as low as room temperature upon storage for an extended period of time [78]. In contrast hydrophobic silicon pairs reportedly did not show any interface bubbles upon storage for up to 113 h at 220°C [78]. However, the formation of bubbles is observed during annealing at 300°C. In general, the interface bubbles vanish when the bonded wafer pairs are heated to temperatures above 1000°C. The formation of interface bubbles upon annealing was first reported by Shimbo [44] and Ohashi [79]. The bubbles were thought to be related to interfacial water [44,69,80]. However, no correlation was found between the amount of water in the interface and the tendency for bubble formation [81]. Even in the interface of hydrophobic silicon wafers, in which there is no water present, a large number of interface bubbles may be detected upon annealing. Mitani et al. suggested that the presence of hydrocarbons in the interface contributes to the formation of interface bubbles [81,82]. A thermodynamic model for the formation of interface bubbles has been presented [82]. The authors suggest that small hydrocarbon molecules are desorbed which are mobile at the interface of the bonded wafer pair. If the vapour pressure which they generate exceeds the energy of adhesion

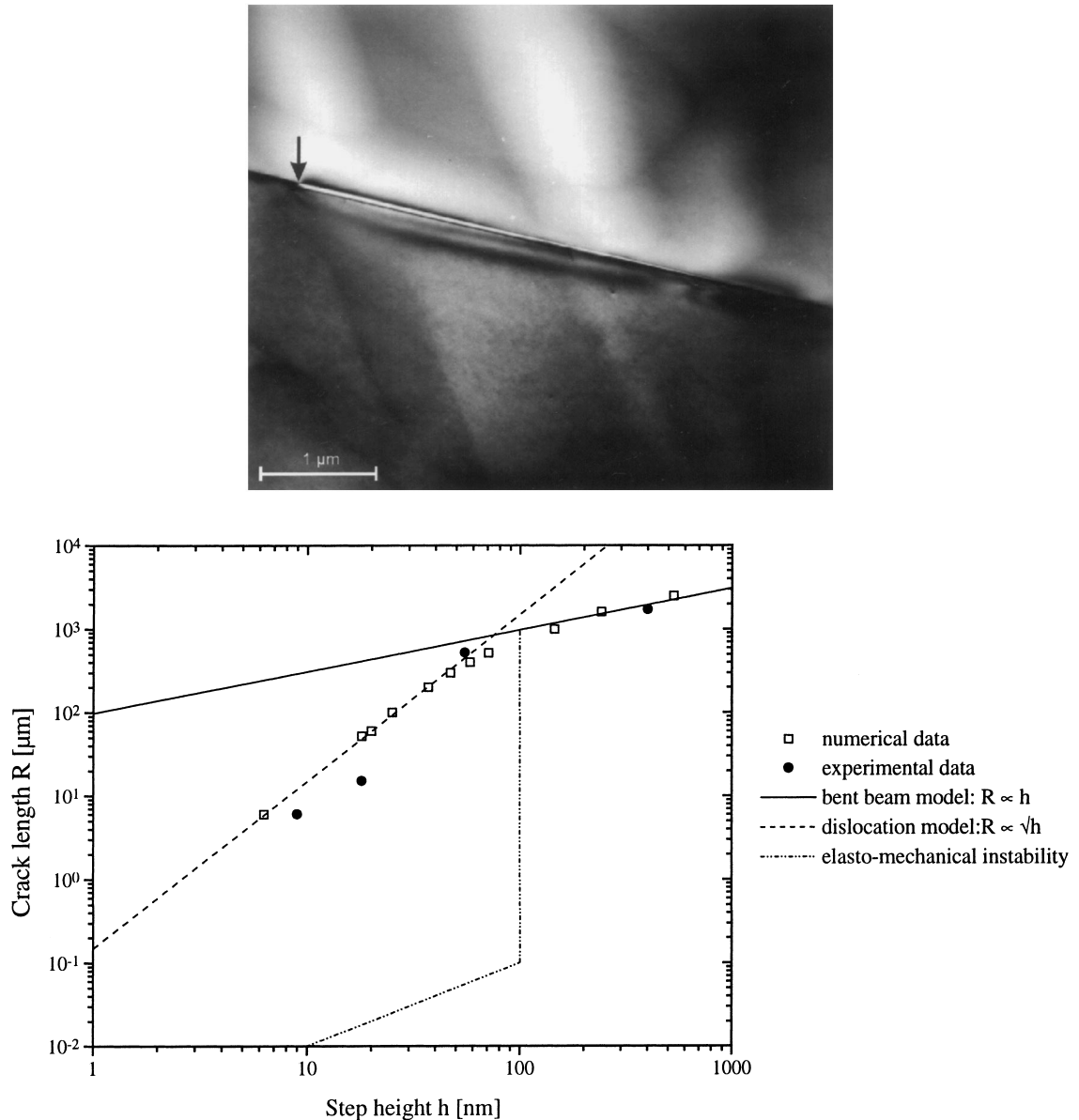


Fig. 11. Investigation of crack length as a function of step height [77]. (a) The high-voltage transmission electron micrograph shows the long crack in the wake of the 18 nm step (marked with an arrow). (Figure reproduced with kind permission of the authors) (b) Comparison of theoretically predicted and experimentally observed crack lengths as a function of step height. The numerical data were calculated employing the boundary element method. The expected elasto-mechanical instability [17,56] is indicated (data taken from [76]).

interface bubbles are nucleated. The bubbles grow by incorporating hydrogen molecules which diffuse along the interface [82].

To study the formation of temperature-dependent interface bubbles and the chemical composition of the trapped gases arrays of cavities of the same size but with different areal densities were produced on a silicon wafer by anisotropic etching [83]. The test structure with the arrays of cavities is depicted in Fig. 12. At the bottom of each cavity only a thin membrane

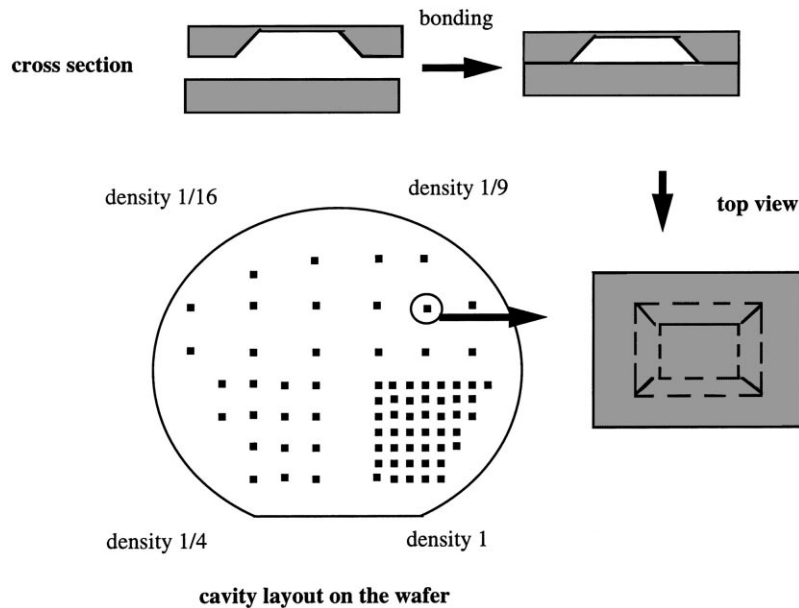


Fig. 12. Cavity structure: Test-wafer layout using various densities of cavities [83].

remained. The expansion of the membrane is related to the pressure formed in the cavity. The structured wafer was bonded to a bare silicon wafer, with either hydrophilic or hydrophobic surfaces under high vacuum. Upon heating the pressure inside the cavities increases. The increase in pressure was measured as a function of cavity density, time and temperature applied. The results of this experiment are shown in Fig. 13. A higher pressure is observed in the cavities with a lower areal density. This can be explained by the larger bonding area around these cavities compared to the bonding area around the cavities with a higher areal density. The gasses trapped in the cavities have

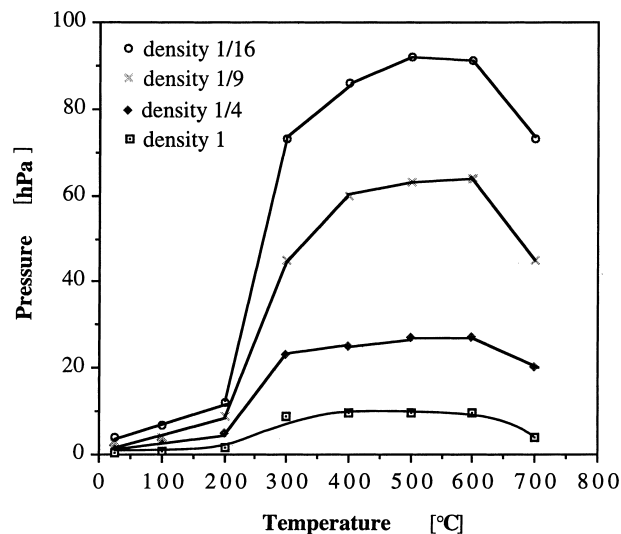


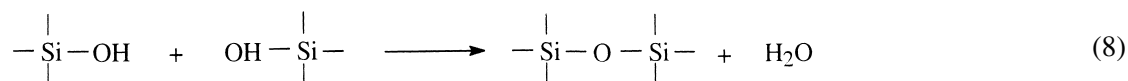
Fig. 13. Pressure increase measured in cavities of bonded hydrophilic silicon wafers as a function of annealing temperature and areal density of the cavities (annealing time: 70h) [433].

been characterised by mass spectrometry [84]. The main content of the gas mixture trapped in both hydrophilic as well as hydrophobic silicon wafer pairs at a temperature range from room temperature to 700°C was identified as hydrogen. Minor amounts of water, hydrocarbons and nitrogen have also been found [84]. These results indicate that at temperatures below 500°C hydrogen molecules diffuse along the interface until they find a cavity or form an interface bubble around a nucleus. Only above about 500°C an appreciable amount of hydrogen diffuses into bulk silicon.

In hydrophilic silicon wafer bonding hydrogen is formed by the reaction between bulk silicon and water (Eq. (7)):

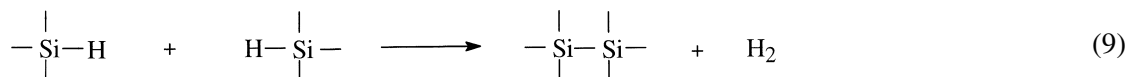


The water for this reaction originates from the few monolayers of water which are present on a hydrophilic silicon surface. Additional water is formed during the condensation reaction between silanol groups (Eq. (8)):



The water diffuses to the bulk silicon where it reacts according to Eq. (7).

The hydrogen in the interface of hydrophobic silicon wafers is formed by the desorption of hydrogen atoms which terminate the surface of hydrophobic silicon wafers (Eq. (9)):



The results of the experiment described above clearly indicate that interface bubbles formed upon annealing are caused by hydrogen. However, for interface bubbles to form the presence of hydrogen alone was found insufficient; hydrocarbons as nucleation centres are also necessary [81]. Taking this in account methods can be devised to prevent the formation of interface bubbles. One step towards the prevention of interface bubbles would be the removal of any thermally unstable organic contamination prior to bonding. Mitani et al. could show that hydrophilic silicon wafers which have been exposed to oxygen or argon at elevated temperature prior to bonding do not form any interface bubbles after bonding and subsequent annealing [81]. A simpler approach to bonding without the occurrence of temperature-dependent interface bubbles is the treatment of hydrophilic silicon surfaces with the dihydrate of periodic acid ($\text{HIO}_4 \cdot 2\text{H}_2\text{O}$), a strong oxidising agent [50]. Both procedures remove organic contamination effectively. As a consequence no interface bubbles are generated upon annealing, even though plenty of water and, after annealing, subsequently hydrogen (Eq. (7)) is present in the interface. Interface bubbles can also be avoided by bonding wafers which are covered with a thermal oxide. The open structure of the thermal oxide is said to allow the hydrogen as well as the volatile organic contaminants to diffuse into the oxide, thereby greatly reducing the gas pressure at the interface [80].

4. Examination of bonding quality

4.1. Introduction

There is a variety of parameters which characterise a bond interface. The relevance of specific properties of the interface depends on the application in mind. For each property, a particular

experiment may be regarded as particularly suitable. It cannot be the intention to list here all the methods applicable to wafer-bonding-related questions. Here only those methods will be summarised which have been most prominent in wafer bonding research.

Frequently, in wafer bonding one is concerned with the question of how well two wafers actually are bonded. The quality of the bonding is determined by the fraction of the interfacial area being in intimate contact and the strength of the bond interaction.

First some methods are to be presented with which areas of bonding can be distinguished from unbonded areas.

4.2. Detection of unbonded areas

After having bonded two wafers one usually would like to know whether intimate contact was established across the whole boundary area or, to put it differently, whether there are any ‘voids’, ‘interface bubbles’ or ‘delaminations’, ‘debonds’ or ‘disbonds’ as the unbonded areas generally are referred to. In the evaluation of adhesive bonds, ‘void’ often means a space in the joint which is free of the adhesive material, whereas ‘delamination’ refers to a separation between a bonding partner on the one side and the adhesive material attached to the other bonding partner on the other side. As in wafer direct bonding the very surface of the bonding partners must be regarded as the adhesive material, this distinction is impractical and the terms often are used synonymously. Depending on their origin, voids may be present immediately after contacting the wafers or only after some storage or annealing time. Uneven surfaces, particles on the surfaces, or pockets of gases trapped by the advancing bonding front can cause voids from the beginning [85]. The mechanisms for the generation of voids with time has not been unravelled in detail. However, it is generally agreed upon that the voids are caused by local accumulation of gases. The gas in the voids can stem from (1) outgassing from the materials to be bonded, (2) from gas entrapped during bonding, (3) thermal decomposition of surface contaminants like hydrocarbons or (4) chemical reactions at the bond interface. In the case of hydrophilic silicon bonding, the formation of water during the silanol condensation or the formation of hydrogen during the oxidation of silicon in the reaction with interfacial water would be examples for the latter cause.

Whether voids of a given size are permissible or not depends on the particular application in mind. If one of the bonded wafers needs to be thinned down to a small thickness, even small delaminations can endanger the integrity of the film. Debonded areas in a loaded bond may accelerate failure.

There are destructive and non-destructive techniques for the detection of interfacial voids. The suitability of a given method depends among other considerations on the size of the bubbles to be detected, the properties of the bonding materials, the stability of the bond interface, the speed and ease of use. The more common techniques only will be listed here. In general, the non-destructive detection of voids is not a difficult analysis problem, unlike the quantitative evaluation of the strength of adhesion.

4.2.1. Optical transmission

The most popular technique to detect areas where intimate contact is lacking is based on the interference of light reflected at internal surfaces [12]. Those Newton’s rings delineate the shape of the delamination. Simultaneously, the bright and dark rings of equal optical thickness permit determining how far the surfaces are separated from each other [86].

In the case of at least one optically transparent bonding partner, like glass, quartz, sapphire or gallium phosphide, voids can be observed with the unaided eye. For materials with lower band gaps

infrared light for illumination and an infrared sensitive camera for viewing are required. Often, the bonded pair is examined in transmission but a reflexion set-up can be of advantage when one of the bonding partners is opaque, for example, like heavily doped silicon. For routine inspection of silicon bonding, a tungsten halogen lamp as light source and a silicon CCD camera whose IR blocking filter has been removed are sufficient.

The method's appeal for global surveying rests mainly with its real-time and non-destructive nature. To detect voids, the surfaces must be separated by at least a quarter of the probing wavelength. The lateral resolution typically is quoted to be 1 mm [12].

Infrared microscopy can be used to enhance the lateral resolution. Khánh et al. reported on a scanning infrared microscopy method utilising light scattered at inhomogeneities [87]. They demonstrated a resolution of about 1–2 μm . Light scattering topography has also been used to detect voids in a fast and non-destructive manner [88].

4.2.2. *Scanning acoustic microscopy*

Next to the interference of light at internal surfaces, scanning acoustic microscopy is the most widespread non-destructive technique to detect delaminations. In acoustic microscopy, mechanical waves are used for probing a sample. A variety of configurations have been demonstrated; for a review, see for example [89].

In wafer bonding, a reflexion mode scanning acoustic microscope is commonly employed. In this so-called C-scan mode, an acoustic transducer generates an acoustic pulse which a lens focuses to a diffraction-limited spot. Typically, the transducers operate at a frequency in the range between 10 and 100 MHz. After the emission of the probing signal, the transducer is switched into detection mode and receives the incoming echoes. The amplitude or the phase of the incoming echo are detected. Through gating, an echo coming from a particular depth can be selected, and by scanning the transducer relative to the sample an acoustic image of that plane in the sample is gathered. Fig. 14 schematically shows an oscilloscope trace of an incoming echo, a so-called A-scan. At the interface between the solid and the void the mechanical waves are reflected almost completely, giving the technique a very high sensitivity even for minor gaps of some 10 nm separation. On the other hand, the large impedance mismatch between solids and air makes it a necessity to use a coupling fluid to effectively transmit the ultrasound pulses from the transducer to the sample and back. Often water is being used. The need for a couplant can limit the non-destructiveness of the method. In the case of weakly bonded specimens, for instance silicon wafers bonded at room temperature in air, the coupling agent may diffuse into the bonding seam, thus causing delamination.

The lateral resolution of acoustic microscopy depends on the frequency used and the materials under investigation. For a 400 MHz transducer, the lateral resolution reportedly lies around 4 μm , and around 8 μm for a 200 MHz transducer; the vertical resolution was found to be better than 50 nm [90].

The useful depth range of the technique is limited on the top surface by a dead zone where the large echoes from the couplant/sample interface mask the echoes from the near surface region and in the depth of a sample by the attenuation of the acoustic pulses.

Other variants of acoustic microscopy can be used. In particular, there is some interest in extending acoustic techniques to a quantification of the strength of the adhesion in bonded areas, as mentioned below.

4.2.3. *X-ray diffraction topography*

When smaller voids are to be detected, X-ray diffraction topography [91] can be used, provided the sample is monocrystalline. In X-ray topography, local changes in spacing or orientation of lattice

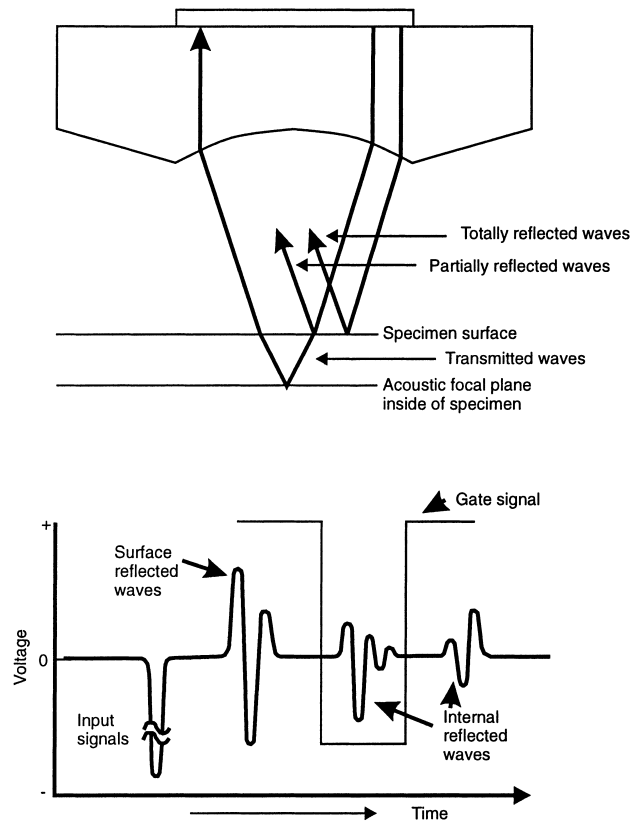


Fig. 14. Principle of C-scan acoustic microscopy.

planes in the investigated sample cause local variations in diffracted X-ray intensities which then are represented in a two-dimensional image. Therefore, at least one of the bonding partners needs to be a single crystal.

The bonded pair is aligned to meet the Bragg's condition $n\lambda = 2d \sin\theta$ (where λ is the X-ray wavelength, d the spacing of the diffracting planes, θ the angle between the incident beam and diffracting planes and n the order of the diffraction), and while the sample is illuminated with a collimated beam of monochromatic X-rays, the ensemble of sample and X-ray recording film is scanned in front of the beam (Fig. 15). The elastic distortions in the wake of a void cause topographic contrast and thus reveal the presence of a bubble.

In the absence of suitable X-ray lenses, there is no magnification involved in X-ray topography. The spatial resolution essentially is limited by the resolution of the detector, for X-ray film this amounts to ca. 1 μm . Because of the need for scanning and the low X-ray intensities, long exposure times are necessary, making the technique time-consuming and expensive. As an example, an X-ray topogram of a 100 mm wafer usually takes several hours.

For the investigation of bonded wafers, X-ray topography may be used in transmission or in reflexion [10,92,93].

Of the common non-destructive void detection techniques discussed in this article, X-ray topography probably is the most sensitive technique; however, the equipment is not routinely available and the method is time-consuming and expensive.

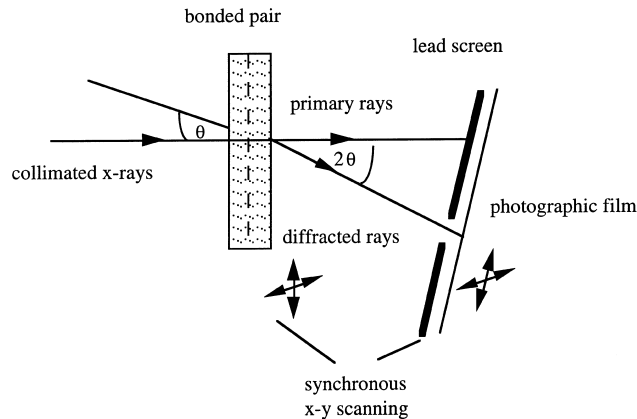


Fig. 15. Principle of X-ray topography.

4.2.4. Magic mirror topography

The magic mirror, or Makyoh, topography is a simple technique for characterising the morphology of mirror-like surfaces [94,95]. The basic principle of the method is shown in Fig. 16. At a small inclination from normal incidence, a collimated beam of light illuminates the whole surface of the sample under investigation. The reflected light is projected into a camera or onto a screen or photographic film to record the topographic image. Any deviations from an ideal mirror plane can cause contrast in the reflected image. The method is very simple, fast and non-destructive.

Particles enclosed in the bonding interface or a gas-filled delamination cause the wafer to locally bulge. In the case of a wafer with a mirror-polished backside, the convex surface deformation due to a bubble can be seen in the reflected image as a dark centre surrounded by a bright ring. As the radius of curvature concomitant with an interface bubble depends on the thickness of the wafers bonded, the ability of the method to detect voids is higher when a thinner wafer has been chosen as reflecting surface. To gain higher sensitivity, the wafer can even be thinned and polished after bonding [96].

Okabayashi et al. compared X-ray topography, ultrasonic microscopy and magic mirror topography; they found that for a 350 μm thick silicon wafer, the magic mirror topography had a slightly lower resolution than X-ray topography [94]. In addition to contrast from the delaminations,

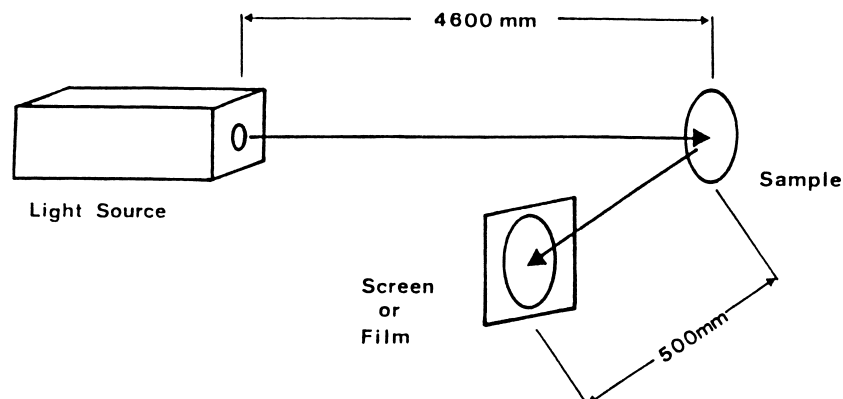


Fig. 16. Principle of Magic Mirror [94].

warping caused during the initial contacting and other defects leaving surface features may complicate the interpretation of the images.

4.2.5. Void detection by etching

Unlike light transmission, C-mode scanning acoustic microscopy, X-ray diffraction topography or the Makyoh method, void detection by etching is a destructive technique. Either the bonded wafer pair is simply etched to thin it or a cross-section is being etched.

The first variant of the method relies on the fact, mentioned above, that thinning one of the wafers of a bonded pair under test enhances the visibility of voids simply through the decrease in the radius of curvature for thinner ‘membranes’ [96,97].

In the second variant, the sample is sawed or cleaved to expose a cross-section of the bonded interface to attack by etchant. Therefore, the samples must adhere strongly enough to withstand the cross-sectioning and immersion in the etching solution. The method permits the detection of voids too small for detection through light transmission, but it only can reveal those bubbles present in the plane of cross-sectioning.

Mitani et al. [98] decorated defects in silicon/silicon bond interfaces with a hot aqueous solution of potassium hydroxide (KOH) on samples sawed in suitable crystallographic directions. They utilised the well-known crystallographic anisotropy of silicon for etching in KOH and the preferential attack of defective silicon. During 15–30 min in the KOH solution, the stronger etching at voids enhances their visibility in optical or scanning electron microscopy.

Horning et al. [99] simply cleaved their silicon/silicon samples and, instead of KOH, they used 4–5 min room temperature Wright etching to decorate the interfacial defects. The main advantage of their procedure seems to lie with the simpler sample preparation and with the better visibility of the etch defects. Samples which were well-bonded apparently displayed only little etching in the interface, thus small defects are not obscured. By implication, the Wright etching technique was reported to require samples of higher adhesion than the KOH approach. Another drawback of the Wright etchant (aqueous solution of CrO_3 , $\text{Cu}(\text{NO}_3)_2$, HF, HNO_3 , CH_3COOH) may be seen in its toxicity and cancerogenicity.

For III–V compound semiconductor interfaces, Babic et al. immersed their samples in a 1 : 1 : 50 H_2SO_4 : H_2O_2 : H_2O solution for 90 s or substituted sulphuric acid by phosphoric acid [19].

4.3. Quantification of adhesion

An important parameter in the characterisation of a bonding process is, loosely speaking, the ‘amount’ of adhesion. Practical adhesion can be quantified in a variety of ways, among others as Dupré work of adhesion or fracture surface energy, or as bond strength.

4.3.1. Measurement of surface energy

In the case of brittle materials which we are concerned here, the Dupré work of adhesion can be measured with fracture mechanical techniques. The work of adhesion and surface energies, γ_1 , γ_2 , are related via

$$W_{\text{adhesion}} = \gamma_1 + \gamma_2 - \gamma_{12}, \quad (10)$$

with the interface energy γ_{12} . The thermodynamic aspects of adhesion and interfacial energies are discussed, for example in Refs. [100–102].

The most common approach for the measurement of fracture surface energies on bonded wafers uses an elaboration of Obreimoff’s arrangement for controlled cleavage [36] described above: the

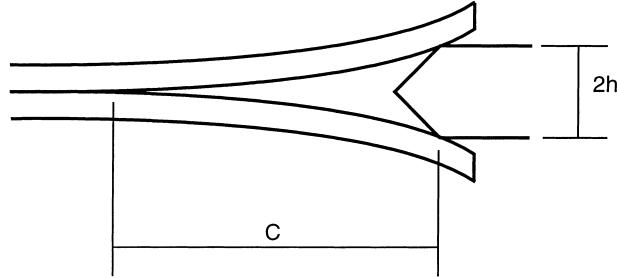


Fig. 17. Double cantilever beam test geometry under constant wedging conditions. The razor blade of thickness $2h$ causes a crack of length c .

double cantilever beam test geometry under constant wedging conditions, shown in Fig. 17. The elastic strain energy in the bent thin plate balances the work of adhesion W_{AB} required to form two new surfaces through the extension of the crack. A wedge of a thickness of $2h$ is inserted at the rim of the beams into the bond interface so as to debond an area of crack length c . At equilibrium, the critical strain energy release rate G_{Ic} equals the work of adhesion

$$W_{AB} = 2\gamma = G_{Ic} = \frac{3Eh^2d^3}{4c^4}, \quad (11)$$

with d being the thickness of the beams and E denoting Young's modulus in the direction of crack propagation [102].

The work of adhesion can also be related to the critical stress intensity factor, K_{Ic} ; in the case of pure mode I loading, this can be expressed as [102–104],

$$W_{AB} = 2\gamma = G_{Ic} = \frac{K_{Ic}^2(1 - \nu^2)}{E}, \quad (12)$$

with ν denoting Poisson's ratio. One of the advantages of the stress-intensity factors in the case of a known crack geometry is their relation to uniformly applied stress [102], σ_A :

$$K_{Ic} = \psi \sigma_A^I \sqrt{c}, \quad (13)$$

with ψ a geometry term, tabulated for many crack geometries [105].

Maszara et al. probably were the first to apply the crack-opening characterisation method in the study of wafer direct bonding [106]. Following their example, the test customarily is applied to complete bonded wafer pairs, and, instead of the work of adhesion, most of the wafer bonding literature quotes the fracture surface energy γ as a measure for the bonding strength. The crack length usually is measured optically, allowing for the additional crack length shadowed by the tip of the wedge and for that part of the crack narrower than ca. $\lambda/4$ of the probing wavelength. The double cantilever beam test applied to complete wafers is sometimes referred to as 'razor blade', 'Maszara' or 'crack opening' test. When executed with the due circumspection, the values should be reproducible to approximately 10%. However, because of the deviation from the proper double cantilever beam geometry, the measurement on complete wafers systematically overestimates the fracture surface energy [107]; as shown by Bagdahn et al. through a finite element analysis, the error increases for increasing adhesion, in their example from about 20% to 80% (Fig. 18).

With some caution, the test can also be applied to patterned wafers, where only a certain area, A_c , of the total wafer area A_t is available for bonding [108]. In the case of stripes of bonding running

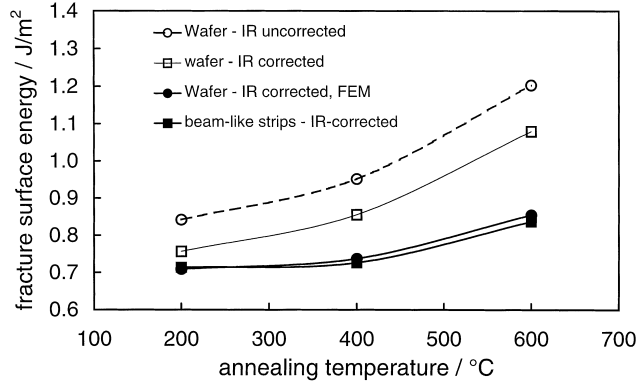


Fig. 18. Fracture surface energy derived from various measurements on wafer and beam-like specimens, after Ref. [107].

parallel to the direction of crack propagation, the apparent fracture surface energy is reduced; this was compensated by a multiplicative factor A_t/A_c :

$$\gamma = \frac{3Eh^2d^3}{8c^4} \cdot \frac{A_t}{A_c}. \quad (14)$$

For stripes normal to the direction of crack propagation, the unmodified formula is applicable.

When bonding wafers of different thickness or elastic properties, the work of adhesion could be calculated according to

$$W_{AB} = G_{Ic} = \frac{3h^2E_1d_1^3E_2d_2^3}{2c^4(E_1d_1^3 + E_2d_2^3)}. \quad (15)$$

The case of a thin wafer bonded to a thick one, or the testing arrangement of Fleming et al. [109], essentially is the system studied by Obreimoff with

$$W_{AB} = 2\gamma = G_{Ic} = \frac{3Eh^2d^3}{8c^4}, \quad (16)$$

where only one beam is being bent.

Without proper precautions, the fracture surface energy derived from the blade test cannot be identified with the intrinsic surface free energy of a solid. Frequently, the test is not completely reversible (cf. also Ref. [37]) and above all, environmental conditions like humidity are known to affect the observed fracture surface energy considerably, often causing a decrease with time [110]. The sensitivity of the fracture surface energy of silicon dioxide, for instance, towards humidity has long been recognised [111]; cracks in pure silicon, however, appear to be rather immune to chemical processes [102]. The main appeal of this blade test applied to complete bonded wafer pairs is its ease of use, requiring no special sample preparation. When comparing data from different experimentators, or when comparing the values with other techniques, the short-cuts taken in the customary blade test should be borne in mind. In addition, there is sometimes some ambiguity in terminology. The fracture surface energy measured occasionally is referred to as interface energy which is not to be confused with the interfacial energy mentioned above. Bond or bonding energy are other terms not unknown in the direct bonding literature. Those terms often make it difficult to know precisely whether the fracture surface energy or the work of adhesion, twice the fracture surface energy, is meant.

In principle, creating a new surface by advancing a crack through the contact interface or advancing the bonding front should be equivalent. Suitably structured wafers may serve as tools for an ‘in situ’ determination of the work of adhesion. Horning et al. patterned silicon wafers with a sequence of parallel lines of known height which serve as wedges [112]. If the line height, line spacing and wafer-thickness were chosen appropriately for the work of adhesion, the wafers bonded between a given pair of lines. A variation of line spacings across the wafer included a range of bond energies. The bond energy was then measured by a simple IR inspection. The technique was used to investigate the influence of surface treatments on the strength of adhesion. With a method similar in spirit, the adhesion was estimated with which two 10 nm thick platinum films, bonded immediately after sputter-deposition onto silicon, adhere to each other [113].

The double cantilever beam test under constant loading was used by Lord Raleigh in his investigation of the bonding of glass [37]. For a rectangular crack geometry, the strain energy release rate is an increasing function of the crack length, making the system unstable. Preparation of a chevron-type specimen geometry stabilises the system again, and such a geometry was used in that investigation. The laborious preparation necessary understandably has never become popular. However, when bonding structured wafers, proper chevron test geometries have been successfully applied [114].

Fracture surface energies as a measure for adhesion can also be extracted from hydrostatic blister tests [115]. Shimbo et al. bonded a silicon wafer with shallow wells against an equivalently polished silicon disk with through-holes, as illustrated in Fig. 19 [44]. Through the hole of a test chip, hydrostatic pressure was applied and the fracture strength was taken as a measure for the strength of adhesion.

4.3.2. Tensile testing

Perhaps the most popular characterisation technique is the tensile test [92,116]. The specimen under test is pulled normal to the bonding interface until the system ruptures (Fig. 20(a)). Almost generally, the stresses observed are much smaller than those which correspond to the forces acting in the bonding interface. This is usually attributed to small flaws in the bond (deliberately introduced structures would act similarly [117]), to elastic stresses stored during formation of the joint, or for

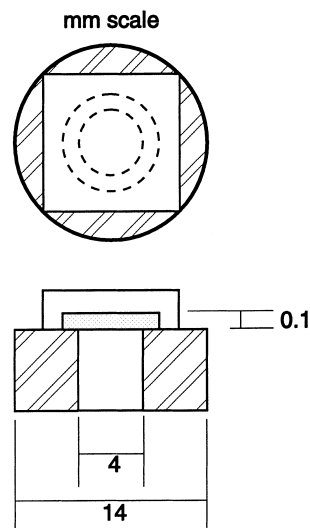


Fig. 19. Sample geometry for adhesion test using hydrostatic pressure [44].

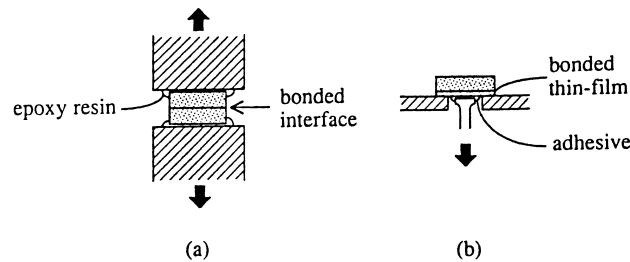


Fig. 20. Tensile test geometrie. (a) Principle, (b) modification for thin films.

instance to defects at the edges of the sample. The applied stress is being concentrated at certain defects and this leads to early failure [118].

Most experimentators mention that the sample under test should be slightly larger than the test stubs, in order to prevent glue creeping around the edges and covering the sides of the test chip (Fig. 20(a)) [116]. The alignment of the test stubs is of critical importance, as small deviations from the surface normal already induce bending moments which can cause premature failure of the sample under test [119]. When applying the adhesives properly, tensile strength values up to 80 MPa may be measured for a standard geometry; for more strongly bonded samples the glue between sample and test stubs gives only a lower limit for the adhesion. Care needs to be taken in dicing the bonded wafers for tensile testing to minimise residual damage at the periphery of the test specimens.

In the case of thin films transferred via direct bonding to a wafer, Abe et al. recommended a modified geometry, shown in Fig. 20(b) [92].

4.3.3. Other tests

Occasionally torsion or shear tests are being used [119].

With all these tests, it is of importance to assess a suitable number of equivalent specimens. Any comparison, be it quantitative or qualitative, must allow for the strong dependence of critical tensile stress values on flaws. When strengthening the bonds of hydrophilic silicon wafers, the tensile strength often does not increase monotonically with the annealing temperature in spite of the monotonic increase in bonding energy. The reason for this is generally ascribed to formation and later disappearance of bubbles in the bonding interface [116].

Often adhesion is assessed simply by noting that a bond withstood certain treatments like grinding of one of the wafers, dicing up the bonded pair through sawing or cleaving, or other loads associated with the application in mind.

An interesting question particularly for microsystems applications, yet hitherto not pursued in much detail, is the problem of long-term stability of subcritically loaded samples [114,120]. The lifetime of joints can be calculated using fracture mechanical models incorporating stress corrosion [114].

All tests presented so far determine some parameter characterising the adhesion destructively. A non-destructive evaluation method with a reasonable lateral resolution would be advantageous. There are several approaches being pursued, all based on acoustic techniques, to realise a non-destructive test for adhesion characterisation.

One method is based on the non-linear dependence of the backdriving force at the bond interface on the deflection, Fig. 21 [121,122]. By increasing the amplitude of the ultrasonic probe pulses, the back-driving force of the bond interface was being brought into the non-linear regime. As schematically shown in Fig. 21, a sinusoidal signal is transmitted into the sample under test. A broad-band ultrasonic transducer is used as receiver for the signal modulated by the elastic response

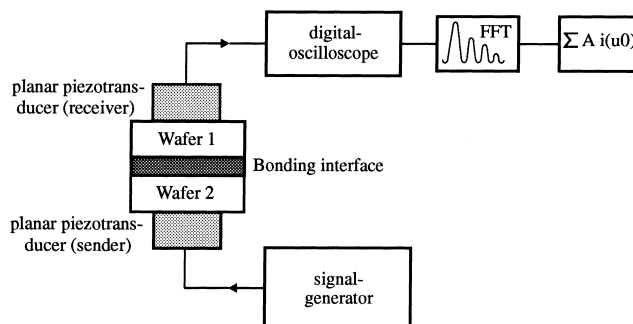


Fig. 21. Schematic set-up of for the non-destructive quantification of adhesion using acoustic microscopy measurements [122].

of the interface. The received signal is Fourier transformed and a summation of the Fourier components served the authors as measure for the back-driving force. Its maximum was taken as a measure of the strength of bonding. Local variations in adhesion and an increase as a function of annealing temperature could be measured. Further developments in ultrasonic transducers could allow a realisation of the technique's potential [122].

Hao et al. used picosecond ultrasonics to generate and detect acoustic pulses in bonded silicon-on-insulator structures [123,124]. A laser pulse hit the aluminium-coated wafer surface and launched a strain pulse into the structure. At interfaces the pulse is partially reflected and those echoes are being detected via the modifications in reflectivity which they impart on the aluminium layer. The authors asserted that numerical fitting allowed them to detect improvements on bond quality; however, no direct comparison with results obtained with another technique have been provided.

4.4. Methods to unravel bonding chemistry

Due to its steric constraints, wafer direct bonding represents a novel environment for the study of chemical reactions. During the annealing of bonded wafer pairs, various chemical reactions must occur to facilitate an increased adhesion. Often the reactions can involve by-products whose evolution can determine the overall reaction behaviour. The chemical reactions upon which much of wafer direct bonding is based may also have a bearing on the long-term stability of the bonding joint or on the pressure attainable in encapsulated cavities. With the exception of silicon bonding, the study of the interfacial chemistry has not yet received much attention. The analysis of the interfacial reactions is being complicated by the initially weak adhesion of many of the systems of interest. Only in exceptional circumstances can destructive techniques like analytical electron microscopy or secondary ion mass spectroscopy be used. Additionally, the area of interest is buried typically in wafer thickness, ca. 1/2 mm, below the surface, ruling out surface analytical probes like X-ray photoelectron spectroscopy.

Two approaches have been demonstrated as particularly well suited to the problem of wafer bonding chemistry, one being a destructive mass spectroscopic technique, the other being a variant of infrared spectroscopy, leaving the bonding interface intact but requiring the preparation of a suitable specimen out of a bonded wafer pair.

4.4.1. Mass spectroscopy

The mass spectroscopic analysis of gases evolving during the annealing of bonded samples is mainly the work of Mack [83,84,120,125]. For his experiments, he etched holes into the wafers so

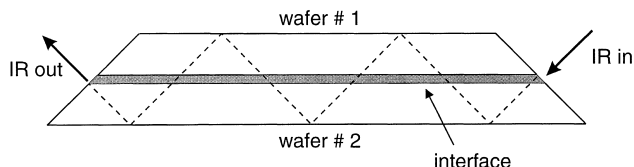


Fig. 22. Specimen geometry for IR spectroscopy in multiple internal reflection on bonded samples [129].

that only a thin membrane had been left; Fig. 12 gives an example of the patterns used. Bonding then created cavities in which the gases could be collected. The deflection of the membrane permitted measuring the internal gas pressure as a function of annealing time or temperature. Hermeticity and interfacial diffusion were thus determined. After in vacuo fracturing of those membranes, the gas content could be analysed mass spectrometrically.

4.4.2. IR spectroscopy

For the infrared spectroscopic analysis of bonded silicon wafers, multiple internal transmission has been established as a most useful geometry with which even for buried layers the sensitivity can be achieved necessary for the detection of monolayers [126–130]. The schematic drawing of Fig. 22 illustrates the shape of a typical sample: the light entrance and exit edges are bevelled, either as shown or to form a parallelogram. In the case of weakly adhering specimens, there is a certain risk that the bonded wafers separate upon dicing, bevelling or chemical cleaning [127]. With the void detection methods described above, like optical transmission or scanning acoustic microscopy, the integrity of the samples can be ascertained. Because of the protective nature of bonding [131], the interface chemistry can be investigated over prolonged periods of time and for various annealing conditions.

Multiple internal transmission infrared spectroscopy is very sensitive to absorption perpendicular to the interface, and interface absorption is strongly enhanced compared to absorption at the outer surfaces of the specimen. However, in-plane absorption would be difficult to detect [127]. The technique provides chemical information via the infrared active molecular species present in the interface. In addition, from shifts of spectral features, the interaction which mediates the adhesion, for example van der Waals forces or hydrogen bonding, can be inferred. As an example, infrared spectroscopy had been used to corroborate that in hydrophobic silicon bonding the hydrogen-terminated (111) oriented wafers adhere essentially through van der Waals interactions [129].

5. Silicon direct-bonding

5.1. Introduction

The phenomenon that mirror-polished oxidised or non-oxidised silicon surfaces bond to each other when they are contacted at room temperature was first reported in 1985/1986 independently by two research groups [44,45]. In the meantime many other materials have been joined by wafer bonding; however, silicon remains the best studied system in wafer bonding technology and is used frequently as a model for a better understanding of the bonding behaviour displayed by other materials. It is widely accepted that intermolecular interactions including van der Waals forces are responsible for the bonding phenomenon at room temperature. Depending on the surface species

involved hydrogen bonding may also play an important role in wafer bonding. However, neither van der Waals forces nor hydrogen bonds are strong enough to join two solids irreversibly. Thus, it is highly desirable to form strong chemical bonds (covalent bonds) across the interface. As we will see in this chapter, the silicon surface may be modified in many ways so that the actual bonding may be caused by weak van der Waals interaction, by hydrogen bonding or even by strong covalent bonds. If the bonding is carried out under ultra-high vacuum covalent bonds even may be formed at room temperature. However, in general, the adhesion is relatively weak at room temperature and is typically increased by annealing the joint. At elevated temperatures, chemical reactions take place between the surface species of opposing wafer sides which usually yield covalent bonds. Typically temperatures of more than 1100°C have been regarded as necessary for this step [14,44,45]. In recent years, however, a variety of procedures have been developed which yield strong adhesion at moderate temperatures. By-products which are formed during interface reactions may cause problems as they may lead to a build-up of pressure in the interface and subsequently to local debonding. Acceptable by-products in silicon wafer bonding are water and hydrogen for water may be consumed through a reaction with silicon and the small hydrogen molecules readily diffuse in the silicon lattice or into a silicon dioxide layer.

Materials which are difficult to bond due to an unfavourable surface chemistry may be bonded via silicon interlayers. Silicon layers can be deposited on many substrates and chemo-mechanical polishing ensures bond-quality surfaces. Since the bonding is governed by the surface species of the two joined materials, the basic bonding behaviour of materials with silicon layers is analogous to the bonding of pure silicon wafers.

In this chapter the actual bonding of different silicon surfaces is described.

It has been stressed already that particulates which are present on the wafer surface before bonding lead to unbonded areas. As a consequence bonding has to be carried out in a particle-free atmosphere. The bonding is either done manually, or a commercially available bonder is used. The latter is particularly useful if the wafers have to be aligned before bonding. For research purposes and small budget production a so-called micro-cleanroom for utilisation in a normal laboratory has been developed. The set-up is described in chapter 3.

The characterisation of the interface formed after the bonding remains a challenge. Several destructive and non-destructive methods for interface characterisation are described in chapter 4. Lately, it has become possible to monitor the processes taking place at the interface of bonded wafers at various temperature using infrared spectroscopy. Silicon is essentially transparent in the spectral range in which vibrations of the species which play an important role in wafer bonding including OH, SiOH, SiH and CH are observed.

Thus, IR vibrational spectroscopy carried out with a special optical configuration to make it more sensitive for interface species (referred to as multiple internal transmission) is a powerful method to monitor the interface chemistry during annealing. Multiple internal transmission IR spectroscopy is described briefly in chapter 4. Using IR vibrational spectroscopy, Chabal and co-workers have monitored the evolution of the molecular interface of bonded silicon wafers [127,132–134] and could essentially corroborate the models developed in recent years [69,135] to explain the wafer bonding phenomenon.

5.2. *The surface of silicon*

It is well-known that silicon easily oxidises when exposed to the ambient atmosphere. Thus, silicon wafers are covered by a 1–2 nm thick native oxide layer, particularly after the usual cleaning steps in highly oxidising solutions [136]. The native oxide layer is terminated by Si–OH groups, so-

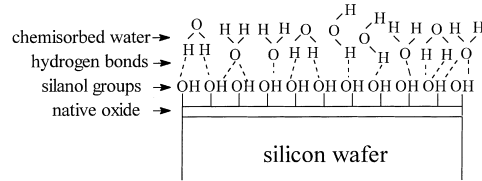


Fig. 23. Schematic drawing of the surface of a hydrophilic silicon wafer covered with a native oxide and chemisorbed water molecules.

called silanol groups (Fig. 23). These silanol groups render the silicon surface hydrophilic and govern the surface chemistry of silicon wafers. The hydrophilicity of a silicon wafer can be easily determined by measuring the contact angle a drop of water forms on the wafer surface (Fig. 24). On a hydrophilic surface a drop of water will spread over a large area. As a consequence the contact angle will be small ($<5^\circ$). Hydrophilic silicon surfaces have much in common with the surface of silica (SiO_2), a material which has been studied in great detail [137]. Many of the findings made for silica, particularly its surface chemistry, can be transferred directly to silicon wafers covered with a native oxide layer. Like silica, hydrophilic silicon surfaces are usually covered with water molecules which interact with the surface silanol groups through the formation of hydrogen bonds (Fig. 23). Their number depends on the humidity and temperature to which the wafers are exposed. The number of surface silanol groups is reported to be 4–5 per nm^2 for a fully hydrolysed silica surface [138]. These groups remain on the surface if the sample is dried at $120\text{--}150^\circ\text{C}$ [138]. The number of surface silanol groups on a hydrophilic silicon wafer surface may be slightly different but is in the same range. The two surface species, namely the silanol groups and chemisorbed water molecules, play an important role in the processes which occur during wafer bonding. Up to now we have only considered the surface of silicon wafers with a native oxide layer. In practice one does, however, often deal with silicon wafers which either are covered with a thick oxide layer or do not possess an oxide layer at all. Such surfaces will be discussed in the following paragraphs.

Many applications require an insulating oxide of considerable thickness on the surface of a silicon wafer. Such thermal oxides are grown in a diffusion quartz tube either in the presence of dry oxygen (Eq. (17)) (dry oxidation) or water through wet oxidation (Eq. (7)), as mentioned above; repeated for clarity) at high temperatures (1000°C). The water is either supplied by a water bubbler or it is formed through an in situ reaction between oxygen and hydrogen in the diffusion tube [139]:



Due to the high temperatures it is exposed to during oxidation, the surface of a silicon wafer possessing a thermal oxide, particularly that of a dry oxide, is relatively dehydrated, i.e. it lacks silanol groups and is therefore hydrophobic. Oxides grown in dry oxygen are dense, whereas wet

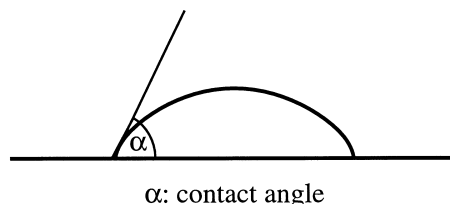


Fig. 24. Contact angle of a droplet on a surface.

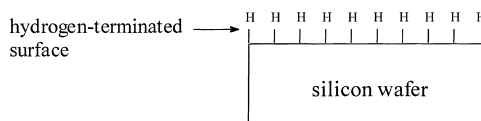
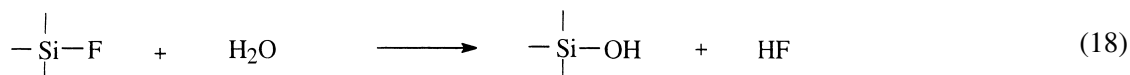


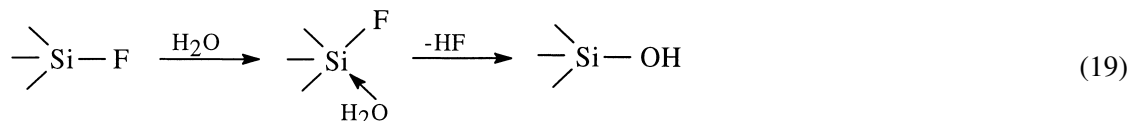
Fig. 25. Schematic illustration of a hydrogen-terminated hydrophobic silicon surface.

oxides tend to be more porous [140]. As the Si/SiO₂ interface tends to become rough with increasing oxide thickness it is believed that the oxide surface itself will also become rough during growth which influences the bondability and energy of adhesion after bonding [141]. Before bonding silicon wafers with thermal oxides the surfaces should be hydrophilised either by treating them in boiling water for an extended period of time or more effectively by a surface activation like oxygen plasma treatment.

Some applications require the absence of any oxide layer. Silicon dioxide layers can be removed by a dip in hydrofluoric acid. For the etching of (111) Si surfaces, buffered ammonium fluoride solution has been recommended [142]. The oxide dissolves during the dip in the etching solution and the remaining bare silicon surface is mainly terminated by hydrogen (Fig. 25) [142]. Additionally, some Si–F bonds can be detected [143,144]. Although the Si–F bond has a high bond energy (see Table 1) [145], it is highly reactive and is cleaved readily in the presence of water. The reaction with water yields Si–OH groups according to (Eq. (18)):



One may ask why despite of its high bond energy the Si–F bond readily is attacked by water, whereas the much weaker C–F bond (see Table 1) possesses a pronounced stability toward water. This difference can be explained by the presence of unoccupied d-orbitals in case of silicon. These unoccupied orbitals facilitate the attachment of a water molecule to the silicon centre and the subsequent formation of a Si–OH bond as shown in (Eq. (19)):



If no empty d-orbitals are available, as it is the case for carbon, the attachment of water cannot proceed and as a consequence the C–F bond cannot be cleaved by water [146]. The reactivity of Si–X bonds toward water (hydrolysis) also is strongly influenced by the polarity of the bond. The polarity of a bond is best described by the difference in electronegativities of the two elements involved. Table 2 displays the electronegativity difference, Δx , for several Si–X bonds [146]. The tendency of the Si–X bond to hydrolyse decreases with decreasing Δx .

5.3. Room temperature bonding of hydrophilic silicon surfaces

Bonding between two wafers can only occur if the surfaces are sufficiently smooth so that when two wafers approach each other the opposing surface species come close enough to interact. If this

Table 1

Mean bond energies, E_b , of some Si–X and C–X bonds in kJ mol^{−1} [145]

E_b (kJ mol ^{−1})	222	452	318	381	565	486
	Si–Si	Si–O	Si–H	Si–Cl	Si–F	C–F

Table 2

Electronegativity difference, Δx , for several Si–X bonds [146]

Δx	Si–F	Si–Cl	Si–C	Si–H
	2.36	1.09	0.76	0.46

requirement is fulfilled the wafers ‘snap’ together as soon as they come in intimate contact. If the wafers are covered with water molecules, which is the case for hydrophilic silicon wafers, the bonding at room temperature is caused by hydrogen bonds between chemisorbed water molecules located on opposing wafer surfaces (Fig. 26). The ‘bonding energy’ between the two wafers which is also referred to as surface energy or, more correctly, as fracture surface energy can be roughly estimated. The energy of hydrogen bonds between OH-species is approximately $20\text{--}40\text{ kJ mol}^{-1}$ [147,148]. This relatively large range is caused by the fact that the energy of hydrogen bonds between silanol groups and water differs from that between two water molecules. Moreover, the energy of hydrogen bonds depends on the distance and orientation of the species involved. An exact calculation of the bonding energy is therefore difficult. For a simple estimate we assume that one monolayer of water is adsorbed to each silicon wafer. The OH-surface density is approximately 5 nm^{-2} . If each OH-group is covered by one water molecule and each water molecule forms one hydrogen bond to an opposing water molecule a bonding energy or more exactly fracture surface energy, γ , of $80\text{--}160\text{ mJ m}^{-2}$ should result. Please note that the fracture surface energy is calculated for the area of the two silicon surfaces which is created if the wafer pair is separated. There is quite some confusion in the literature concerning surface energy values. Depending if the author applies the energy to only one of the two surfaces involved or both surfaces formed during separation the values may differ by a factor of 2.

Experimentally, the fracture surface energy of bonded wafers can be determined by the double cantilever method, as described in chapter 4. The experimental values for bonded silicon containing a native oxide layer are in the range of $100\text{--}150\text{ mJ m}^{-2}$ and are thus in good agreement with the calculated values. If the bonded wafers are stored at room temperature for an extended period of time (100 days) the interface energy increases to more than 200 mJ m^{-2} [78]. The increase is attributed to the slow diffusion of water molecules out of the interface. Some opposing silanol groups may then be close enough to form a covalent bond across the interface leading to an overall increase of the fracture surface energy.

Silicon wafers with thermal oxide layers show an analogous interface chemistry at room temperature. The experimentally determined values energy for fracture surface are approximately 100 mJ m^{-2} and thus lower than in the case of silicon wafers which are covered by a native oxide. This can be explained by a slightly rougher surface of thermal oxides [141].

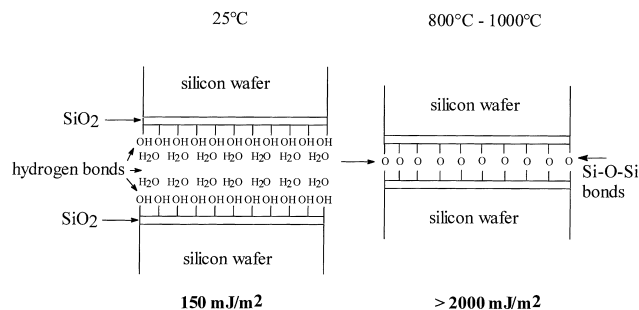
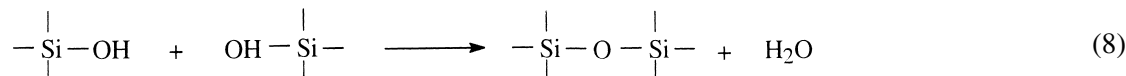


Fig. 26. Schematic drawing of the bonding of a two hydrophilic silicon surfaces at room temperature and at 800°C.

From a chemist's point of view, it is rather surprising that at room temperature the bonding phenomenon seems to be entirely based on weak van der Waals forces and hydrogen bonds. It is widely accepted that Si–OH groups can condensate with each other at room temperature or slightly above forming Si–O–Si and water (Eq. (8), as mentioned above; repeated for clarity) [137,149]:



In fact, the sol–gel processing of SiO₂ is based on the condensation of silanol groups, and temperatures well below 100°C are found perfectly sufficient. A large number of Si–OH groups is present on a hydrophilic silicon surface. Nevertheless, if two silicon wafers are contacted the condensation between silanol groups of opposing silicon wafers which would subsequently lead to a strong adhesion does not occur anywhere close to room temperature. This different behaviour is the result of very different reaction conditions of silanol-containing species in a sol–gel process on the one hand and silanol surface groups in wafer bonding on the other hand. Whereas, in the sol–gel process the reaction occurs in solution with molecules being free to move around, the silanol groups on a silicon wafer are immobilised on a solid substrate. Moreover, the immobilised silanol groups are covered by water molecules which make them inaccessible for a reaction with silanol groups of the opposing wafer side. Therefore, at room temperature the reacting species at the interface are the chemisorbed water molecules; the silanol groups are not directly involved in the bonding under these conditions.

5.4. Room temperature bonding of hydrophobic silicon wafers

Hydrophobic silicon surfaces are generated if the native oxide layer is removed by applying etching solutions like hydrogen fluoride or ammonium fluoride. This treatment leads to hydrogen terminated surfaces with some Si–F bonds present. The surface is not wetted by water anymore, the contact angle with water is 60–70° [49,150]. The treatment with HF-containing solutions can lead to a roughening of the wafer surface which may effect the bonding [151].

When bonding H-terminated silicon wafers, the rinsing as well as the spin-drying step should be omitted to avoid re-hydrophilisation of the wafers due to the reaction of Si–F with water which leads to Si–OH. Moreover, hydrophobic surfaces tend to get contaminated by hydrocarbons much faster than hydrophilic surfaces [53]. Thus, it is important to bond hydrophobic silicon wafers immediately after the removal of the silicon dioxide layer.

The bonding between hydrogen terminated silicon surfaces is caused by the formation of van der Waals bonds between surface H-atoms located on opposing wafer sides (Fig. 27) [151,152]. Additionally, the few F-atoms or OH-groups formed by the reaction of water with Si–F present on the surface may form hydrogen bonds to opposing species. Some authors attribute the interaction between hydrophobic silicon surfaces entirely to hydrogen bonds formed by minority impurities like Si–F or Si–OH groups present on the opposing surfaces [143,144,153]. To determine whether van der Waals forces between opposing Si–H groups cause the bonding, IR spectroscopy was performed on NH₄F/HF etched (111) silicon surfaces and interfaces. The IR spectrum of an atomically flat hydrophobic (111) silicon surface significantly differs from the spectrum observed of the interface of a room temperature bonded hydrophobic (111) silicon wafer pair. Whereas the hydrophobic (111) Si-surface exhibits a sharp Si–H monohydride stretching vibration, the Si–H vibration is strongly perturbed upon bonding [129,134]. This indicates that the wafers are in intimate contact after the bonding and that there are van der Waals forces present between opposing Si–H groups in the interface between two hydrophobic silicon surfaces. If the silicon surface is rather rough (rms

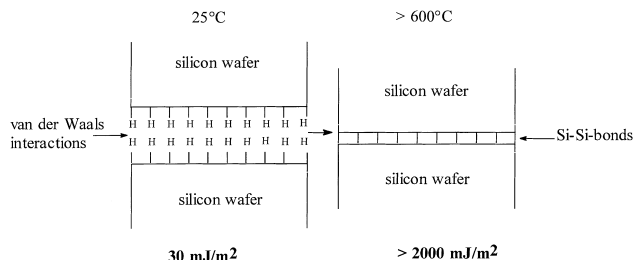


Fig. 27. Schematic drawing of the bonding of two hydrophobic silicon surfaces at room temperature and at 600°C.

roughness >0.3 nm), as it is frequently observed for HF-etched (100) or (111) silicon surfaces, no shift of the signal for the Si–H vibration is observed when comparing the unbonded silicon surface to the interface of a bonded wafer pair. This is due to a lack of intimate contact between opposing Si–H groups. In this case the bonding involves only a small number of sites [134].

Since van der Waals forces are weaker than hydrogen bonds the energy required to separate two bonded silicon wafers with hydrophobic surfaces is lower than in the case of hydrophilic silicon surfaces. Values between 20 and 30 mJ m^{-2} are reported for the surface energy of hydrophobic silicon wafers [152].

Another type of hydrophobic silicon surfaces, namely wafers which have been treated with monolayers of organic molecules will be discussed later.

5.5. Thermal treatment of bonded silicon wafers

After bonding at room temperature the wafers are usually treated at elevated temperatures to increase the energy of adhesion. Extensive studies of the reactions which occur during the annealing process in the interface of a bonded silicon wafer pair have been carried out in recent years. The knowledge gained has been utilised to develop low temperature bonding methods which are described later in this chapter.

5.5.1. Thermal treatment of hydrophilic silicon wafers

Fig. 28 shows the gain in bonding energy with temperature for silicon wafers containing a native oxide layer. As described earlier the bonding at room temperature is caused by the formation of hydrogen bonds between chemisorbed water molecules located on opposing wafer surfaces. Below 110°C the interface energy remains low. Above this temperature the desorption of water molecules sets in. The water molecules diffuse out of the interface either through the native oxide to the bulk silicon where they react to form SiO_2 and hydrogen (Eq. (7), as mentioned above, repeated for clarity) or they diffuse along the interface to the outside.



To verify that some of the water molecules react with silicon after diffusion through the oxide the following experiment was carried out: silicon wafers containing cavities were bonded under vacuum and annealed at elevated temperature. The gaseous products formed during the interface reaction were trapped in the cavities and analysed by mass spectrometry. The main component was found to be hydrogen [84].

As soon as water molecules have left the interface, opposing silanol groups which come close enough can react with each other to form covalent Si–O–Si bonds (siloxane bonds) and water

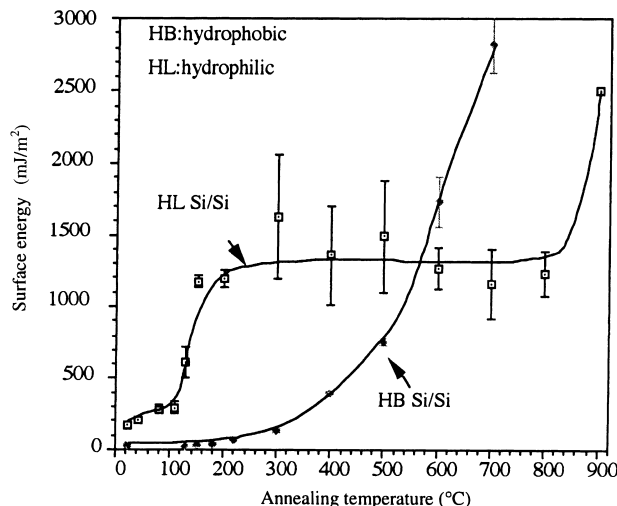
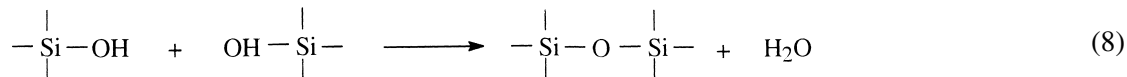


Fig. 28. Fracture surface energy of hydrophilic and hydrophobic bonded silicon wafers as a function of annealing temperature (with permission of the authors reprinted from Ref. [22]).

(Eq. (8), repeated for convenience):



As a consequence the interface energy increases rapidly between 110°C and 200°C. Several authors report an almost constant fracture surface energy of about 1.2 J m^{-2} between 200°C and 700°C [69,135]. At 700–800°C there is another increase in fracture surface energy to a value of more than 2 J m^{-2} up to the cohesive strength of silicon [69,135].

One explanation for this behaviour suggests that up to 700°C the fracture surface energy is limited by the actual contact area. According to this theory the wafers are not perfectly smooth and thus there are areas which do not come close enough to react. As a consequence, microgaps may form at the interface. At 800°C the native oxide is viscous enough to fill out these microgaps. As a consequence the remaining silanol groups can condensate and thus the fracture surface energy increases [135]. There is, however, some evidence that also other factors influence the interface energy, particularly the ability of the system to remove water molecules which are formed during the condensation of silanol groups. The condensation reaction described in Eq. (8) is in principle reversible. Thus, water molecules formed during the condensation of silanol groups may cleave siloxane units as described in Eq. (20), thereby weakening the adhesion [154].

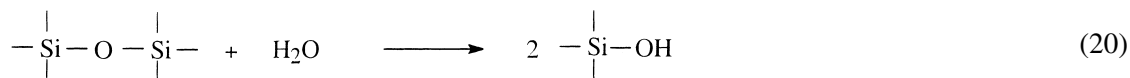


Fig. 29 shows a cross-sectional transmission electron micrograph of the interface of a bonded silicon wafer pair. The amorphous layer is caused by the native oxides present on the two silicon surfaces prior to bonding. Additional oxide is formed through the reaction between interfacial water and silicon. Usually an oxide layer thickness of 3–4 nm is observed at room temperature or moderate temperature. After annealing the sample at temperatures above 1000°C the layer thickness decreases to 2–2.5 nm [155,156]. From an applications point of view, the thermal stability of the oxide interphase is an important issue. On the one hand it may be desirable to join wafers using hydrophilic

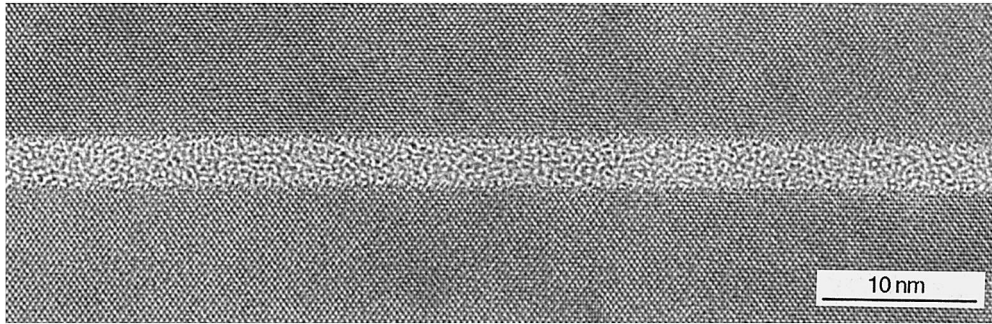


Fig. 29. Cross-sectional high resolution transmission electron micrograph of the interface of a bonded hydrophilic silicon wafer pair. The amorphous interlayer represents the combined native silicon dioxide layers of both wafers (micrograph courtesy Dr. R. Scholz, MPI Halle).

direct bonding but being able to dissolve this insulating layer in a subsequent annealing step, on the other hand a homogeneous insulating oxide interphase may need to sustain high-temperature processing steps without degradation in uniformity. Therefore a number of studies addressed the question of the silicon oxide interphase stability [155,157–161]. The possibility that the silicon oxide interphase between well-oriented wafers (twist less than 1°) may dissolve upon annealing at temperatures above 1000°C has been known from the beginning of silicon direct bonding [44].

In the absence of misorientation, the thermal stability of the interfacial oxide is governed by solubility considerations, with the oxygen dissolving into the bulk of the bonded wafers, and the interface energy at the Si/SiO₂ boundary as driving force [157]. In the case of misoriented crystals, additionally the energy required for dislocation formation needs to be taken into account [157]. Based upon their analysis, Ahn et al. derived a critical angle of some $1\text{--}3^\circ$, above which the energy which needed to be expended in forming the dislocation network in the interface stabilises the oxide interphase against disintegration, and this was also borne out by their experiments [157]. In float-zone grown silicon, long-term high-temperature annealing can succeed in dissolving the oxide interphase irrespective of the misorientation between the bonded wafers, reflecting the larger solubility of oxygen there [157]. A supercritical misorientation angle, however, reportedly stabilised the silicon oxide layer against disintegration during a 2 h 1100°C annealing; while a further 10 days 1150°C annealing step completely eliminated the oxide interphase [157]. Although the higher oxygen content in Cz-grown silicon makes a dissolution of the silicon oxide layer difficult, the reduction in Si/SiO₂ interfacial energy drives the non-uniform dissolution via holes in the oxide layer, oxide disks and finally oxide spheroids [157]. Provided the oxide interphase is thinner than 3 nm, the disintegration of the oxide layer for subcritical misorientations may start by the formation of holes and concomitant growth or thickening of the remaining oxide through local diffusion of oxygen [157]. There are, however, indications that the oxide interlayer is prone to disintegration even for larger angles. For instance, Ju et al. observed for samples annealed at 1100°C for 3 h in nitrogen the onset of disintegration [161]. In addition, after 1100°C annealing for 5 days, plan-view transmission electron micrographs of a wafer pair bonded with a twist of 7° exhibited a disintegrated oxide layer, as shown in Fig. 30(a) and (b) [162]. Also the growth of an oxide interphase during thermal oxidation has been studied [163,164].

When bonding wafers containing a thermal oxide layer ($1\text{ }\mu\text{m}$, grown in the presence of water at 1000°C), annealing at 1000°C is required to reach a fracture surface energy of 2 J m^{-2} [165]. The fracture surface energy at $150\text{--}600^\circ\text{C}$ does not exceed $700\text{--}800\text{ mJ m}^{-2}$. However, when two silicon wafers, one of which contains a native oxide layer the other one a thermal oxide, are bonded the gain

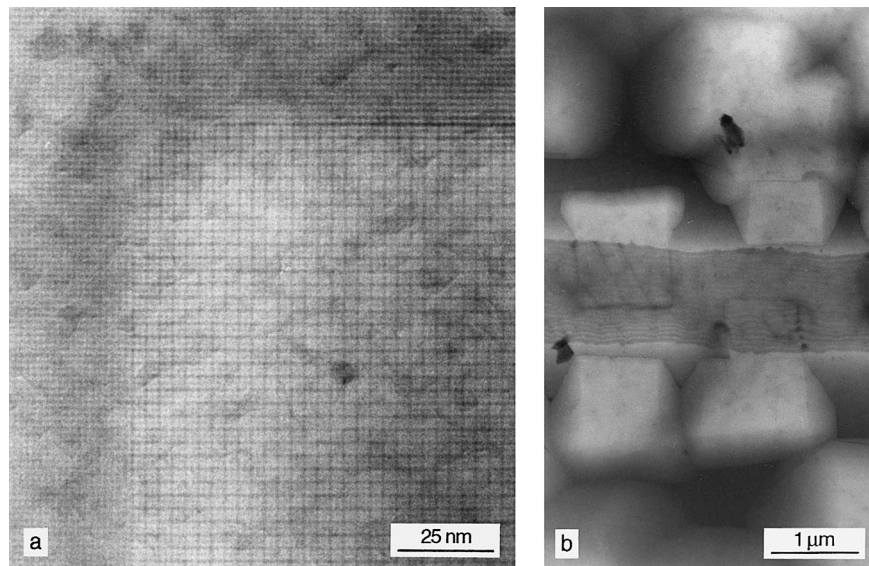


Fig. 30. Disintegration of the oxide interphase, in an advanced stadium of hole formation. Cz-grown silicon wafers with a hydrophilic surface were bonded with a supercritical twist angle of 7° and subsequently annealed at 1100°C . (a) Dislocation network in oxide hole indicates Si/Si interface whereas area with oxide interphase shows only Moiré pattern (mesh with smaller spacing), (b) Low magnification overview shows the holey oxide interlayer, where the bright areas are holes [162] (micrographs courtesy Dr. R. Scholz, MPI Halle).

in fracture surface energy with time is similar to that obtained when bonding two wafers with native oxides only. In an interphase consisting of two thermal oxides the diffusion of water through the interphase into the silicon lattice, where it can react according to Eq. (7), is hampered. However, if one of the interface oxides is a thin native oxide the diffusion of water can readily proceed through the thin layer. Moreover, silicon dioxide layers are known to absorb hydrogen readily [80]. Thus, a wafer combination consisting of one silicon wafer with native oxide and one with a thermal oxide is beneficial for wafer bonding. While the native oxide allows the diffusion of water out of the interface, the thermal oxide may absorb hydrogen which is formed in a reaction between silicon and water (Eq. (7)) [80]. From this, a simple design rule can be derived: if a buried oxide layer is to be produced by wafer bonding, one wafer should contribute the whole oxide, while the other wafer should be covered by a native oxide only, to yield strong adhesion at relatively moderate conditions [165].

5.5.2. Thermal treatment of hydrophobic silicon wafers

The increase in fracture surface energy with temperature as observed for a bonded silicon wafer pair with hydrogen terminated silicon surfaces is depicted in Fig. 28. Up to about 400°C the energy of adhesion remains low. At 400°C the desorption of hydrogen from the wafer surface sets in. First hydrogen from the less stable dihydride arrangements desorbs, followed by hydrogen from the monohydride structures [166,167]. The small hydrogen molecules readily diffuse along the interface or into the relatively open silicon lattice, while Si–Si bonds are formed across the interface. At about 700°C the bonding energy reaches the cohesive strength of bulk silicon [143]. Fig. 31 shows the interface formed upon annealing (600°C) of two bonded hydrophobic silicon wafers. In contrast to the interface of hydrophilic silicon wafers no amorphous interlayer is visible. However, in the example chosen there is a high density of nanometre-size voids at the interface. It can be

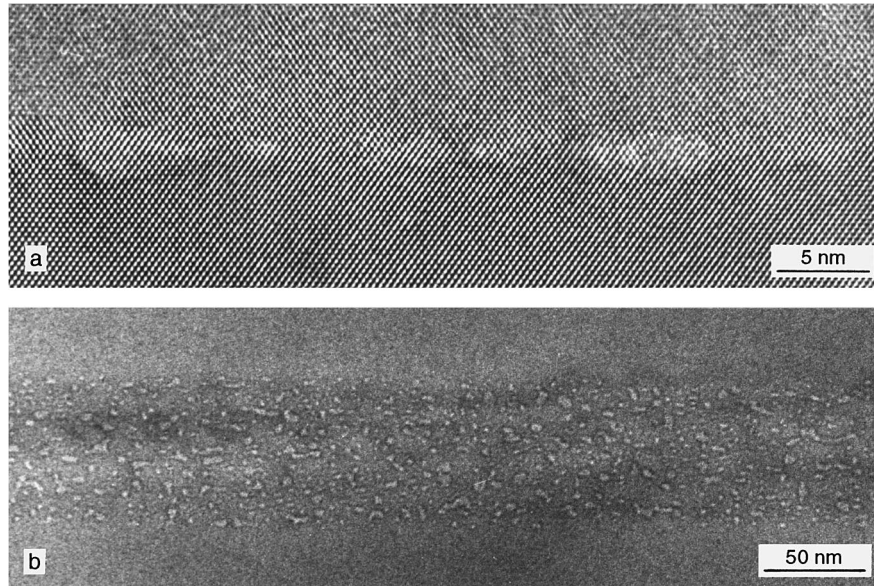


Fig. 31. Interface of a hydrophobic FZ-grown (100) Si wafer pair bonded at room temperature and subsequently annealed at 600°C. (a) Cross-sectional high resolution transmission electron micrograph of the interface. In addition to the quasi-coherent continuation of the lattice across the interface, a few nanometre-size voids are discernible, (b) The cross-sectional specimen of (a) tilted by 40°, to image the interface in quasi-plane view. Kinematic electron-optical conditions in underfocus are employed to delineate the minute cavities through Fresnel contrast (areal density ca. 10^{12} cm^{-2}) (micrographs courtesy Dr. R. Scholz, MPI Halle).

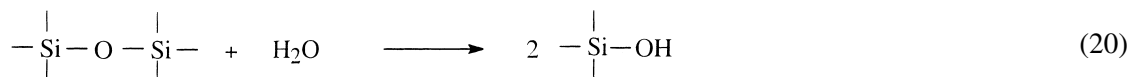
assumed that the voids are filled with hydrogen desorbed from the bond surface during annealing (Eq. (9)).

5.6. Low temperature bonding

For many applications the high temperatures required in conventional wafer bonding to reach sufficient adhesion present a problem. Particularly pre-structured wafers which already contain temperature-sensitive structures cannot be exposed to the high annealing temperatures. Thus, shortly after the discovery of silicon wafer bonding, studies aimed at the development of methods which yield strong adhesion at low temperatures were initiated. Today, a variety of different methods for low temperature bonding are available.

Many studies in the field of low temperature bonding have focused on the bonding of hydrophilic silicon surfaces. From the sol–gel glass literature it is known that the conversion of Si–OH groups into Si–O–Si units can proceed at low temperatures [119,137,149]. Since the increase in bonding energy in hydrophilic silicon wafer bonding is based on the conversion of silanol groups into siloxane groups it should in principle be possible to obtain high bonding energies at low temperature. There is quite some evidence that the diffusion of water out of the interface is the limiting factor in hydrophilic silicon wafer bonding at low temperature. As discussed above, water molecules are adsorbed at the hydrophilic silicon surface at room temperature and thus are present in the interface after bonding. Additional water is produced through the condensation reaction of silanol groups (Eq. (8)). It is obvious that the water molecules have to be removed from the interface before a close contact of all surface species can be established. On their way out of the interface water molecules may react with already formed siloxane groups. As a consequence the siloxane unit

is cleaved yielding silanol groups (Eq. (20)), as mentioned above; repeated for clarity) which weakens the overall energy of adhesion:



One approach to low temperature bonding of hydrophilic silicon surfaces is therefore to facilitate the diffusion of water through the interface. As can be seen in the following section, several low temperature methods are aimed at the acceleration of water diffusion and the subsequent enhancement of silanol condensation.

5.6.1. Long-term storage of bonded wafers

A considerable increase in fracture surface energy is observed when storing bonded wafers at temperatures between room temperature and 150°C [78]. For hydrophilic wafers the bonding energy increases gradually at a storage above room temperature to reach saturation. Hydrophobic wafer pairs have to be stored at temperatures >150°C to observe an analogous effect. Interface bubbles form upon storage of hydrophilic wafer pairs at temperatures as low as room temperature [78].

5.6.2. Surface treatment with hydrolysed tetraalkoxysilanes $\text{Si}(\text{OR})_4$ (with $R = \text{alkyl}$)

If silicon wafers are soaked in a highly diluted solution of hydrolysed mixtures of tetramethoxysilane (TMOS) or tetraethoxysilane (TEOS) and subsequently bonded, fracture surface energies of about $1.7\text{--}2 \text{ J m}^{-2}$ are obtained after annealing the wafer pair at 200–400°C [168,169]. The thickness of the native silicon dioxide layer does not increase during this treatment as determined by spectroscopic ellipsometry. One explanation for this observation could be found in the hydrolysis of tetramethoxysilane which yields monosilicic acid ($\text{Si}(\text{OH})_4$) [170]. If present in low concentration monosilicic acid condensates very slowly. The condensation products which possess numerous silanol groups may replace some of the native oxide. This reactive layer may facilitate the diffusion of water out of the interface thereby accelerating the overall reaction rate. The best bonding results are obtained when TMOS is hydrolysed in the presence of NH_4OH [171]. This reaction yields dissolved ammonium silicate ($(\text{NH}_4)_2\text{SiO}_3$). As discussed later in this chapter, silicates are known to enhance the bonding process considerably. This assumption, however, needs to be investigated in further studies. Nevertheless, the treatment with hydrolysed TMOS or TEOS is quite effective without introducing any undesirable ions in the interface.

5.6.3. Surface treatment with nitric acid

A simple method to obtain strong adhesion at low temperature is to first remove the native oxide layer by a dip in hydrofluoric acid and subsequently treat the wafers with concentrated or diluted (65%) nitric acid prior to bonding. Concentrated nitric acid offers the advantage that it is compatible with aluminium. After this simple surface treatment the tensile strength of the bonded wafer pair yields 15–20 MPa upon annealing at temperatures as low as 120°C [172–174]. The only drawback of this surface treatment is the toxic and irritant nature of hydrofluoric and nitric acid.

The authors did not give a convincing explanation for the dramatic increase in fracture surface energy after the treatment with nitric acid. It seems, however, likely that the oxide formed during the treatment in nitric acid is more porous than the conventional native oxide. Nitric acid reacts with silicon among other products under the formation of gaseous nitrogen monoxide (Eq. (21)):



Generally, if in a chemical reaction a solid product (here SiO_2) is formed under simultaneous evolution of a gaseous product, the solid becomes porous. This effect is frequently used when preparing foams, for example polyurethane foam. In this case the formation of polyurethane proceeds under simultaneous evolution of carbon dioxide gas.

When treating silicon wafers with nitric acid, some of the nitrogen monoxide gas may be trapped in the native oxide layer and is removed upon extensive rinsing or by treating the wafers in boiling water. An observation which supports this theory is that a large number of bubbles is formed in the interface upon annealing if wafers are not thoroughly rinsed after the treatment with nitric acid. The authors suggested a 1 h rinse with deionised water after nitric acid treatment [174]. This long period of rinsing is obviously necessary to remove any traces of gaseous nitrogen oxide trapped in the porous native oxide. When the gas has been removed pores remain in the native oxide layer. The interface water can readily diffuse through these pores. Further investigations are needed to clarify the effect of nitric acid treatment.

5.6.4. Low vacuum bonding

If the bonding of hydrophilic silicon surfaces is carried out under a vacuum of a few mbar, upon annealing of the bonded wafer pair at temperatures as low as 150°C fracture surface energies of about 3 J m^{-2} are reported [175]. Fig. 32(a) shows the increase of the fracture surface energy as a function of annealing temperature. The increase in fracture surface energy as a function of annealing time at a constant temperature of 150°C is depicted in Fig. 32(b). The authors suggested that at ambient pressure trapped nitrogen prevents the silanol groups from reacting with each other at low temperatures. If the nitrogen is removed by applying vacuum prior to bonding the silanol groups can get close enough to react at much lower temperatures than in conventional bonding. A similar effect was observed for wafers bonded at ambient pressure, either when they subsequently were stored under vacuum at room temperature and finally annealed in air at 150°C , or when they were annealed at 150°C under vacuum [175]. The trapping of nitrogen in the interface of bonded silicon wafers has also been suggested by other authors who, upon annealing of hydrophobic bonded silicon wafers to 1150°C , observed the formation of silicon nitride in the interface [87].

Besides trapped nitrogen there may, however, be another reason for the observed strong adhesion at low temperature in low vacuum bonding. At a vacuum of a few mbar, water is removed readily from the wafer surface and even from the native oxide particularly if the wafers are slightly heated during the vacuum treatment. A decrease in the number of water molecules in the interface could accelerate the condensation of surface silanol groups and additionally lead to a faster diffusion of water molecules formed during the condensation reaction. Multiple internal transmission IR spectroscopy would be the method of choice to monitor the interface reactions in low-vacuum bonding. A comparison of the spectra with the spectra obtained for samples which were bonded without applying a vacuum could elucidate the observed phenomena.

5.6.5. Surface activation via plasma treatment

There are several reports stating that a plasma treatment prior to bonding leads to an increased chemical reactivity of the silicon surface and consequently to high fracture surface energies at moderate temperature. Most commonly an oxygen plasma is used [48,165,176–180]; however, other gases including argon [181] gave similar results. At room temperature the bonding energy is similar to the values obtained without plasma cleaning. However, annealing of the plasma-treated bonded wafer pair at $300\text{--}400^\circ\text{C}$ results in a bonding energy which exceeds 2 J m^{-2} . The effect the plasma treatment has on the surface is not really understood. Some authors suggest that the density of bonding sites is increased [179]. The surfaces are highly charged after the plasma treatment which is

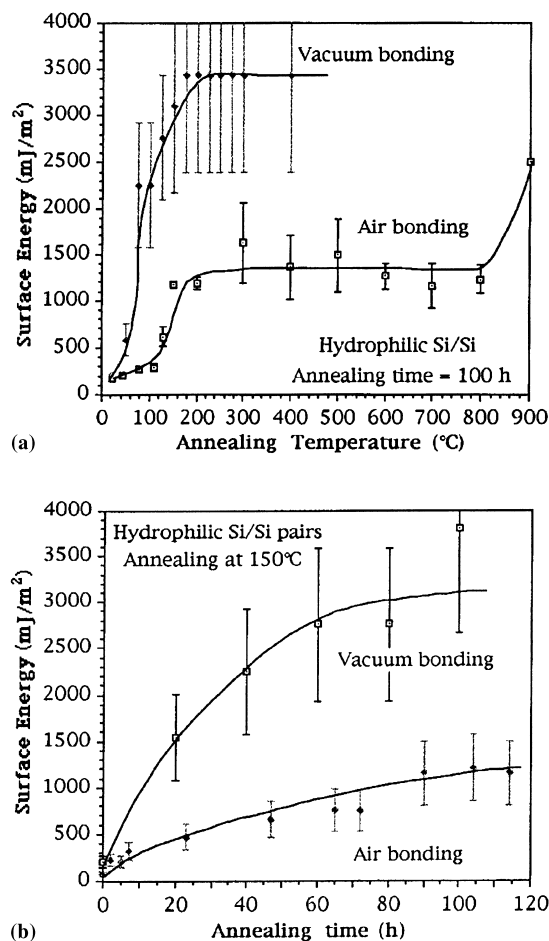


Fig. 32. Fracture surface energy as observed in low vacuum bonding (a) as function of annealing temperature; (b) as function of annealing time at a constant annealing temperature of 150°C (after Ref. [175]).

thought to lead to an significant increase in the atomic mobility of the reacting species [180]. Although the surface of plasma treated silicon is highly reactive the activated surface possesses a long-term stability. Even after several days of storage the contact angle remains low [48]. This is in contrast to observations made for silicon surfaces cleaned using the common wet cleaning procedures where a significant increase in contact angle after several hours of storage had been noted [48].

Alternatively, oxygen ion bombardment [182] or the deposition of a reactive sputtered oxide [183] has been reported for surface activation.

5.7. Bonding via designed monolayers

Recently, attempts have been undertaken to modify the silicon surface via designed monolayers of organic compounds prior to bonding. The compounds are deposited either using the Langmuir–Blodgett technique [184] or by adsorption from solution [185]. Both techniques allow the deposition of uniform monolayers. In a first set of experiments macromolecules with a rigid backbone and additional flexible side chains, so called hairy-rod molecules (Fig. 33), have been deposited onto

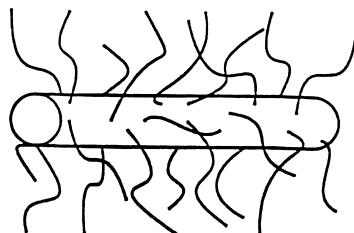


Fig. 33. Schematic drawing of a hairy-rod molecule.

silicon wafers employing the Langmuir–Blodgett technique. This technique offers the advantage that any number of monolayers can be transferred. It is carried out by spreading the desired compound on a water surface. A movable barrier is used to push the layer together until a dense monomolecular film is formed on the water surface. Then a hydrophobic silicon wafer is slowly dipped into the water while the barrier keeps pushing (Fig. 34). One monolayer is transferred during each dipping and undipping step. Two wafers treated with hairy-rod molecules were contacted to induce bonding. The interaction between the two wafers is based on the formation of mechanical entanglements between the flexible sidegroups of opposing molecules. The bonding energy at room temperature increases from 30 mJ m^{-2} for a hydrophobic silicon wafer pair without hairy-rod molecules to $100\text{--}450 \text{ mJ m}^{-2}$ for wafer pairs containing a few monolayers of hairy-rod molecules [184].

An alternative and very simple method to deposit monolayers of organic compounds onto silicon wafers is the adsorption from solution. A suitable compound possessing a functional group which is able to form a covalent bond with the surface silanol groups of a silicon wafer is dissolved in an inert organic solvent. Subsequently, a silicon wafer is exposed for a few hours to this solution. Certain compounds including long-chain alkylsilanes like octadecyltrichlorosilane (OTS) or dimethyloctadecylmonochlorosilane assemble themselves as monolayers on the wafer surface (Fig. 35). Silicon surfaces with monolayers of alkylsilanes are very smooth and highly hydrophobic, exhibiting contact angles of more than 100° . If two silicon wafers treated with such compounds are contacted they bond spontaneously through van der Waals interactions between opposing methyl groups. The bonding energy is in the range of 20 mJ m^{-2} . A considerable increase in the energy of adhesion is obtained if entanglements between opposing alkyl chains are formed (Fig. 36). This is achieved by heating the wafer pair above the melting point of the alkyl chain. Entanglements between opposing chains are, however, formed only if there is enough space between two neighbouring alkyl chains, i.e. if the packing of the monolayer is not too dense [185]. Thus, in case of the densely packed OTS monolayers no increase in energy of adhesion is observed, whereas wafer pairs treated with the less densely packed dimethyloctadecylmonochlorosilane experience a dramatic increase in fracture surface energy after a heat treatment at 180°C .

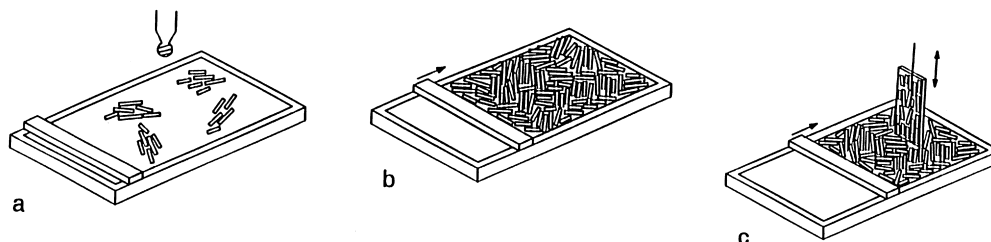


Fig. 34. Schematic drawing describing the Langmuir–Blodgett technique: (a) spreading; (b) compression; (c) transfer.

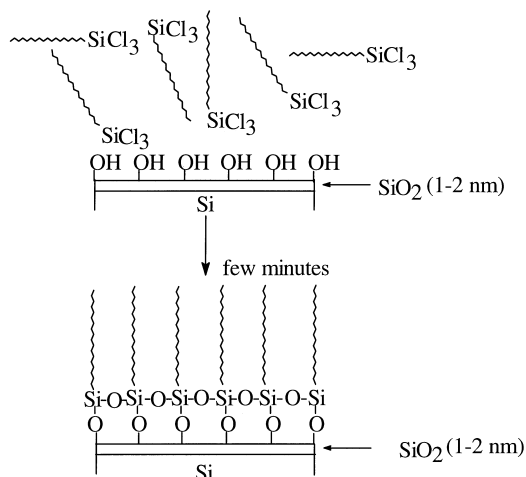


Fig. 35. Self-assembly of octadecyltrichlorosilane (OTS) molecules; the long alkyl chains are drawn as zigzag lines.

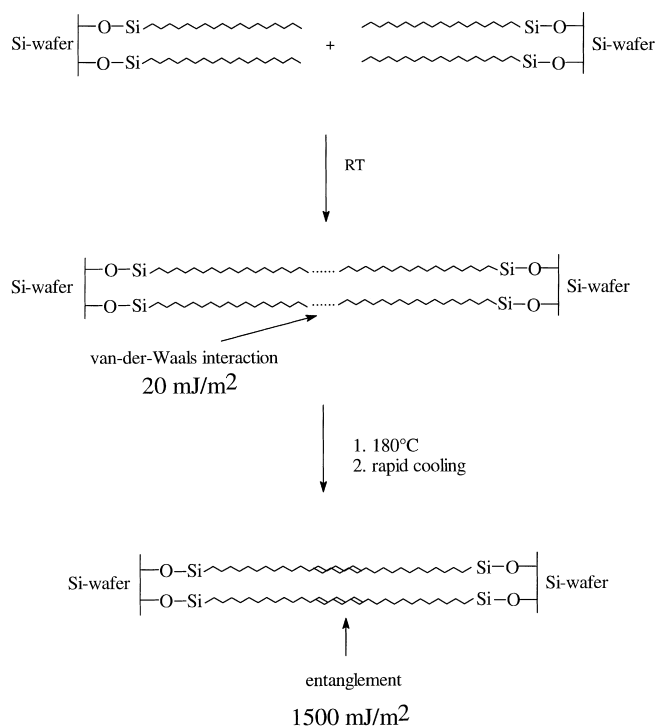


Fig. 36. Formation of entanglements of surface-immobilised dimethyloctadecylmonochlorosilane molecules located on opposing silicon wafers. Upon heating to 180°C and subsequent cooling, entanglements are formed.

The next logical step in bonding via monolayers would be the design of monolayers which are not only able to covalently bond to the wafer surface but possess a second functionality which would allow them to form a covalent bond across the interface to the opposing monolayer. To avoid debonding, the interface reaction would have to proceed without the formation of by-products. This, combined with the steric restriction imposed in the interface, make such studies particularly challenging. Research aimed in this direction has been undertaken recently [186,187].

5.8. Room temperature covalent bonding

With the bonding methods discussed so far, the wafers adhere to each other upon room temperature contact through van der Waals forces or hydrogen bonds. Si–Si or Si–O–Si bonds were formed across the interface only when the wafers were annealed. In many instances a stronger initial interaction is required. The bonding of atomically clean surfaces is such a low temperature joining technique as it can attain adhesion comparable to the cohesion of the solids involved. The basic concept of this approach is very simple: bonding is regarded as the reversion of the cleaving of a crystal. In the absence of surface reconstruction, the atoms at the surface would lack part of their nearest neighbours and the resulting dangling bonds would constitute very reactive species. Formation of covalent bonds with an adjoining surface would permit annihilating the dangling bonds. In a more formalistic rationalisation, the regain of the fracture surface energy expended during splitting drives the bonding reaction. Erosion and indentation measurements gave 1.82 J m^{-2} for Si (111), 2.25 J m^{-2} for Si (100) and 2.4 J m^{-2} for Si (110) surfaces [188], so that between 3.6 and 4.8 J m^{-2} might be expected as driving force. Contaminants adsorbing on the surface diminish the surface energy dramatically [102] and hence the ability for room temperature covalent bonding. In this simplistic description, difficulties arising from surface reconstructions have been neglected [189,190]. However, the possibility of reconstructions so stable that an additional thermal activation [191] would be required should be borne in mind. Through a judicious choice of the bonding conditions guaranteeing atomically clean silicon surfaces, covalent bonds can be formed at room temperature as soon as the wafers come into intimate contact.

From a theoretical point of view, Nelson et al. studied with self-consistent pseudopotential methods the interaction between ideal Si(111) 1×1 surfaces [192]. Driven by the overlap of electronic surface states, the solids exhibit a structural instability as the surfaces approach each other: for separations smaller than 2.5 \AA , through the formation of covalent bonds, an adhesive avalanche occurs [192].

Scheerschmidt et al. simulated the bonding of (100) oriented silicon surfaces with semi-classical molecular dynamics routines [193–196]. They used the Si(100) 2×1 surface which one expects when the hydrogen of hydrogen-terminated silicon is thermally desorbed just above 500°C [197]. As soon as the two solids approached each other within the interaction distance of their potentials, the dimers broke up and covalent bonds were formed joining the two crystals. The energy set free can be used in the re-arrangement of surface atoms so as to form a smooth interface (Fig. 37). In these molecular dynamics investigations, there was no evidence for an activation barrier that could prevent covalent bonding to proceed at room temperature. The molecular dynamics studies also were extended to model the atomic structure defects in the interface caused by steps or rotations. Simulated transmission electron micrographs taken on those structural models then were compared with experimentally obtained micrographs. The splitting up of the screw dislocations into partial dislocations was predicted. A detailed discussion of molecular dynamics studies of wafer bonding will be the topic of a forthcoming review by Scheerschmidt et al. [198]

The feasibility of this novel approach has been demonstrated by Gösele et al. experimentally. At room temperature, covalent bonding between two clean 4 in. (100) silicon wafers was achieved without the application of external pressure. To meet the stringent requirements on the surface cleanliness, the bonding experiments were conducted in ultra-high vacuum, and therefore this type of bonding sometimes is referred to as ‘UHV-bonding’. Since that seminal report, not only silicon has been joined by this method but in an analogous fashion a variety of other homo- or hetero-junctions have been produced [199–205], even involving metal interlayers [206]. Experimentally two approaches have been adopted for preparing the clean surfaces. One method relies first and foremost

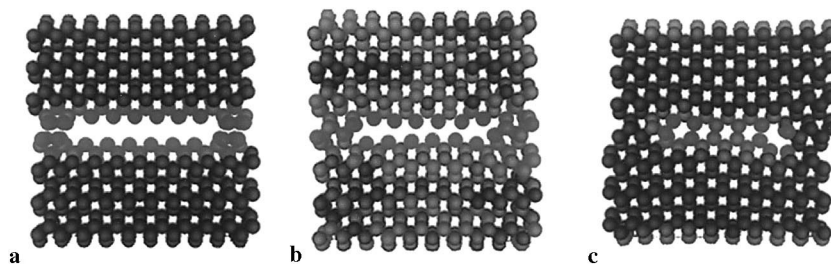


Fig. 37. Molecular dynamics sequence showing the bonding across a double step. The grey scale depicts the energy dissipation during bonding, with the lighter shades of grey indicating a higher potential with reference to the ground state. (a) initial configuration with one layer missing in both wafers, (b) after 12.5 fs (300 K), (c) after cooling (0 K) (after Ref. [196], reproduced with kind permission of the authors).

on an argon fast-atom-beam (FAB) to remove the surface contamination layer through erosion [199,203]. This method frequently is referred to as surface activated bonding. Alternatively, a two step cleaning procedure has been adopted. After standard wet chemical cleaning the native silicon oxide layer has been dissolved in an aqueous solution containing hydrofluoric acid which simultaneously passivates the surface through hydrogen termination of dangling bonds. Following this ex situ cleaning step, the hydrogen passivation has been thermally desorbed in vacuo (Fig. 38) [201,202,207,208]. The latter method does avoid crystal damage which may result from the bombardment with energetic particles employed in the first method. Moreover, preferential sputtering during atom or ion beam cleaning can change the stoichiometry of compound materials to be joined, as for instance observed in the case of steel [209].

Frequently it has been inferred from tensile testing that the bonding is of covalent nature. Such pull tests, however, inherently yield data with a large scatter as local flaws and imperfections lead to localised stress increase and hence to premature failure of the sample under test. Therefore the assertion of adhesion comparable to cohesion based on pull tests may not be above criticism. More conclusive evidence has been provided through fracture mechanical approaches like four-point bending or double cantilever beam tests [202]. Silicon wafers cut in (100) [199,201,207,210], (110) or (111) [202] orientation have been bonded to like or unlike surfaces. They all bonded covalently at room temperature. The reactivity of the surfaces reportedly did not depend sensitively on the relative orientation of the bonding partners [202]. The results published so far do not provide evidence for an activation barrier towards bonding. In some earlier adhesion studies on diamond with atomically clean surfaces only negligible interaction was found between two crystals in intimate contact [211]. It is unclear whether this is solely due to the insufficient smoothness and planeness of the crystals used or whether it was caused by an activation barrier. The fact that in many of the earlier adhesion

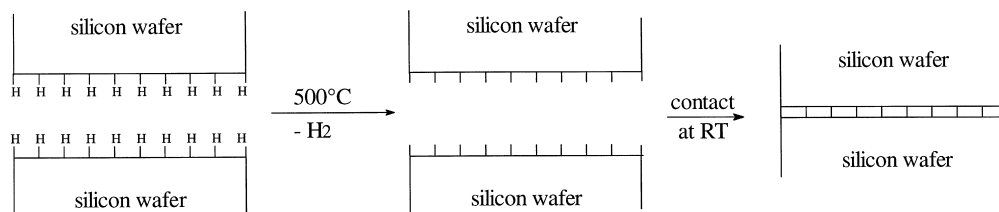


Fig. 38. Schematic illustration of UHV-bonding: preparation of clean surface through chemical cleaning and in vacuo thermal desorption of hydrogen passivation.

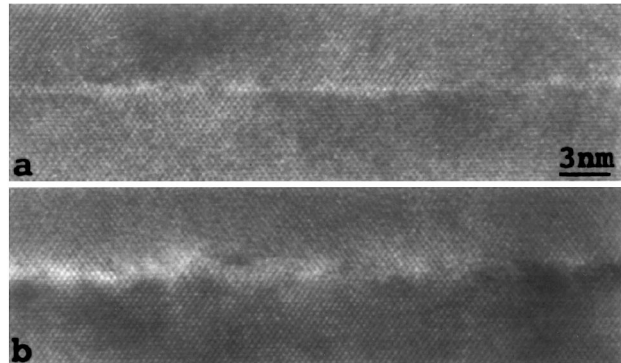


Fig. 39. High-resolution transmission electron micrographs of UHV-bonded 3 in. (100) Si wafers [201]. (a) Interface of wafers with clean surfaces; (b) interface of wafers with ca. 5% monolayer of carbon contamination.

studies the surfaces were rough by normal wafer bonding standards makes many of those findings inconclusive.

Adsorbates are known to reduce the reactivity of the surfaces, eventually preventing the formation of covalent bonds at room temperature contact. There are no quantitative investigations detailing what amount of residual contaminants would be permissible. Circumstantial evidence emphasises the detrimental influence which carbon-containing species could exert on the reactivity of the silicon surfaces. Carbon contamination equivalent to 5% of a monolayer apparently did not prevent room temperature covalent bonding [201]. However, it caused roughness at the interface. Fig. 39 compares cross-sectional transmission electron micrographs of such a contaminated sample to one of a clean sample [201,212]. Silicon carbide precipitates had been detected in a sample which had been annealed after the usual procedure for room temperature covalent bonding resulted only in adhesion via van der Waals forces [202]. A reduction in fracture surface energy was observed when the silicon surfaces were stored in UHV after the desorption of the hydrogen passivation (Fig. 40) [202].

Contaminants preferentially react with surface radicals (dangling bonds) or attack the strained bonds between silicon dimers. Oxidation of the surface might be a likely deactivation process. For instance, water vapour adsorbs dissociatively onto silicon at room temperature and the oxygen then

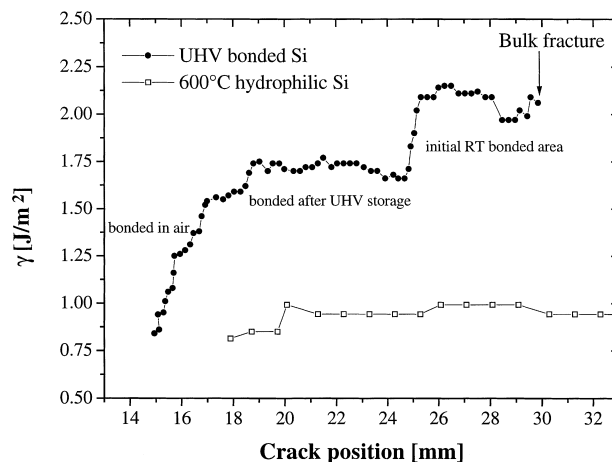


Fig. 40. Dependence of fracture surface energy on in vacuo surface contamination (after Ref. [202]).

inserts into the dimer bond, forming a suboxide surface structure [213]. The oxidised surface structure is believed to be less reactive than the pure silicon surface as all dangling bonds have been saturated in relatively stable bonding configurations. It is an intriguing question whether an oxidised silicon surface or a silicon dioxide surface is amenable to room temperature covalent bonding or not. Experiments some 30 years ago on the adhesion of polished quartz crystals in ultra-high vacuum did not find any reactivity between the surfaces, only adhesion mediated through van der Waals forces [214]. Similarly, an investigation of the adhesion between clean surfaces using crossed glass cylinders did not find any evidence for the strong bonding expected [211]. In a more recent experiment in which $9 \times 9 \text{ mm}^2$ pieces of oxidised silicon were pressed together with an applied load of 1 MPa after they had been cleaned with an Ar FAB, again only weak adhesion could be attained [215]. The question as to whether room temperature contact is sufficient to form covalent bonds between silicon oxide surfaces remains an unresolved issue. It is tempting to speculate that the configurational freedom of the silicon-oxide system known from its glass-forming capability [216] is sufficient to ensure that surfaces can be terminated with chemically stable bonds. Under this assumption, silicon dioxide bonding may serve as an example of a system with an appreciable activation barrier. However, further studies are required to determine the limits of the room temperature covalent bonding concept.

The structural quality of the samples depends on the cleanliness of the surfaces as well as on the method of cleaning. Argon beam cleaning is known to amorphise a surface layer of silicon and consequently all samples bonded employing this cleaning technique contained an amorphous interlayer, of approximately 5 nm thickness [215]. In the case of a chemical removal of the silicon oxide and the subsequent in vacuo desorption of the hydrogen passivation, no amorphous interlayer has been apparent in high resolution transmission electron micrographs. The interface could be described as smooth with the lattice planes quasi-coherently continuing across the interface (Fig. 39) [201,210]. The absence of interfacial voids is in agreement with the notion that the voids reported in conventional bonding arise from gaseous by-products of the bonding reaction or from the cracking of residual surface contaminants.

The square network of $a/2$ [100] screw dislocations which the plan-view transmission electron micrograph of Fig. 41 shows, formed upon room temperature contact of two (100) silicon wafers rotated by 1.4° around their surface normal [210]. Although not a necessary precondition, the formation of an interface structure predicted from general grain boundary theory [217,218] and known from silicon grain boundaries formed by high temperature fusion [219–223] represents further evidence for covalent bonding at room temperature. Indeed, in a number of cases no dislocation network had been observed in spite of adhesion comparable to the cohesion of silicon, as determined through measurements of fracture surface energies [202]. The reasons which lead to those structural differences have not yet been clarified.

5.9. Bonding via silicon and silicon dioxide interlayers

5.9.1. Bonding via polycrystalline silicon (polysilicon) interlayers

Polycrystalline silicon is readily deposited onto a variety of substrates by the pyrolytic decomposition of silane at normal or low pressure. Films grown below a temperature of 575°C are amorphous, whereas films grown above this temperature are polycrystalline. Reasonable growth rates are obtained at $650\text{--}700^\circ\text{C}$ [224]. Because of their identical chemical composition polysilicon and single crystalline silicon exhibit basically the same surface chemistry, and thus the same chemical reactions reported for single-crystalline silicon should occur in the interface of bonded polysilicon.

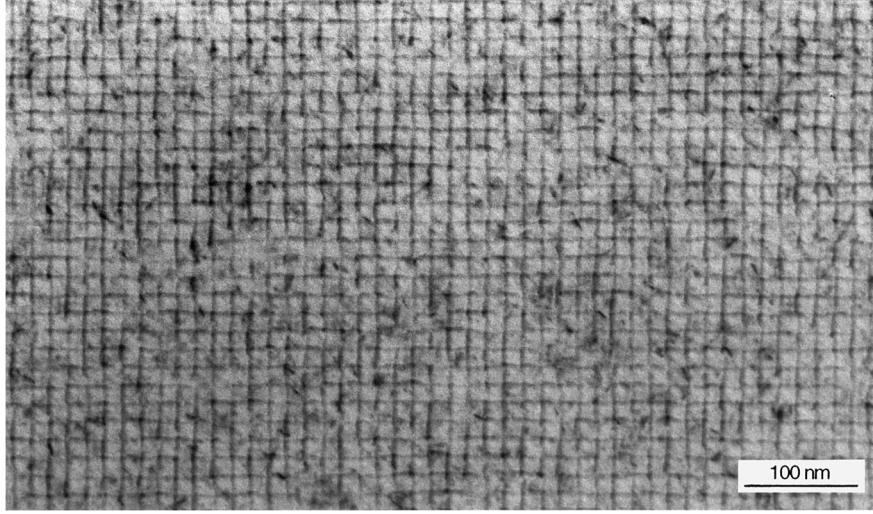


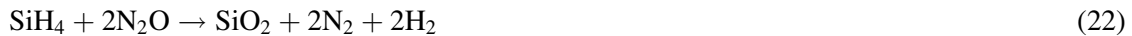
Fig. 41. 1.4° twist boundary formed through room temperature UHV-bonding of two (100) silicon wafers. The multibeam plane-view transmission electron micrograph shows the square network of $a/2\langle 110 \rangle$ screw dislocations (after Ref. [202]).

Since polysilicon consists of many small crystallites (grains) the surface of the material received upon deposition is not sufficiently smooth ($\text{rms} > 100 \text{ nm}$) for wafer bonding. Thus, the surface smoothness has to be improved by chemo-mechanical polishing (CMP) down to a rms roughness of a few Ångström. Highly doped polysilicon layers are conductive and additionally exhibit a reasonable thermal conductivity. Therefore, smooth polysilicon layers have the potential to serve as intermediate bonding layers in cases where an uneven topography has to be planarised and additionally good electrical and thermal conductivity is required at the interface. There are several reports about the direct bonding of polysilicon coated substrates [225–229]. The authors stress the importance of mechanical and chemical polishing to obtain smooth surfaces suitable for bonding.

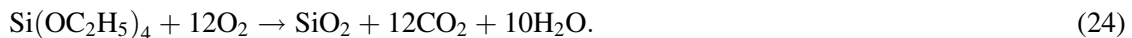
Polysilicon bonding has been reported for the preparation of laminated dielectrically isolated (LDI) wafers [227,228]. The critical step in these procedures remains the polishing of the polysilicon layer in order to attain a surface smooth enough for bonding. In a different study, polysilicon-to-polysilicon bonding has been used to produce a 3C-SiC layer on SiO_2 [229–231]. The polishing of polysilicon surfaces has been in the focus of recent research efforts [64] and it can be anticipated that the direct bonding of polysilicon intermediate layers will be stimulated further by these studies.

5.9.2. Bonding via silicon dioxide layers

Silicon dioxide layers deposited by CVD are promising interlayers in cases where an unfavourable topography prohibits bonding. Silicon dioxide films are formed by the oxidation of silane with both N_2O or O_2 in a LPCVD system at about 450°C (Eqs. (22) and (23)) [232]:



Silicon dioxide films are also frequently grown by the pyrolytic oxidation of alkoxysilanes like tetraethoxysilane (TEOS) (Eq. (24)):



The reaction is carried out by LPCVD at 650–750°C or by PECVD at low temperatures (typically 350°C) [232]. Both methods yield uniform films with an excellent step coverage.

As the interface chemistry of CVD-oxides is very similar to the chemistry of thermal silicon dioxide the bonding proceeds analogous to the well-studied bonding of thermal silicon oxides. The surface of a CVD-oxide is generally rougher than that of a thermal oxide. Before bonding, consequently, a polishing step using CMP is usually required. Moreover, deposited films have a higher contamination level when compared to thermal oxides. Therefore, before bonding an outgassing heat treatment is frequently applied to avoid the formation of gas bubbles in the bonding interface upon annealing of the bonded wafer pair. CVD-oxide bonding has also been used to prepare small area SOI islands by selective polishing [233].

A CVD-silicon oxide has been deposited onto the surface of a processed VLSI bulk silicon wafer where, after chemo-mechanical polishing, it formed a bondable layer [63]. The bonding behaviour of CVD-SiO₂ with other CVD-layers including polysilicon and silicon nitride has been studied [225]. There was also a report of low temperature bonding via CVD silicon nitride layers [434].

5.10. The bonding of quartz, fused silica and glass

The chemical composition of the surface of glass, fused silica and quartz is almost identical with that of the hydrophilic silicon surface. Thus, the chemical reactions which take place during bonding and annealing are very similar to those in silicon bonding. Unlike silicon, the materials quartz, fused silica and glass are hardly able to consume water at elevated temperature. If no silicon is present most of the water has to diffuse laterally out of the interface.

Several studies deal with the bonding of quartz to silicon. Quartz is a crystalline modification of silicon dioxide. The trigonal α -quartz, which is the stable modification at room temperature, undergoes a phase transition at 575°C to form hexagonal β -quartz [234]. This phase transition limits the annealing temperature the material can be exposed to after bonding. Due to its piezoelectric properties the material is used extensively in crystal resonators, oscillators and in filters for frequency control and modulation. The material is transparent, insulating and inert against most chemicals. Structures can be introduced by anisotropic etching with HF-based solutions [235,236]. Clean quartz wafers of sufficient surface quality bond spontaneously when brought into intimate contact at room temperature. The fracture surface energy can be increased by an annealing step at 200–500°C [237].

For the development of miniaturised electro-acoustic devices it has become essential to bond quartz crystals with controlled crystallographic orientation onto a silicon substrate [238,239]. Quartz and silicon exhibit an identical surface chemistry. Both have terminal silanol groups which are covered by chemisorbed water molecules. Thus, room temperature bonding between an optically polished quartz crystal and a prime grade polished silicon wafer proceeds readily via the formation of hydrogen bonds between chemisorbed water molecules. However, due to the different thermal expansion coefficients of both materials (4.6×10^{-6} (silicon, 300°C); 14.5×10^{-6} – 16.6×10^{-6} (single crystalline quartz, 300°C)) the heat treatment which is necessary to convert the weak hydrogen bonds into strong covalent Si–O bonds may lead to cracking. These problems can be circumvented by selecting a very thin quartz crystal for the bonding experiments. If the quartz crystal is only 50 μm thick and bonded to silicon wafer of a thickness of 500 μm the assembly may be heated to 450°C without any crack formation. If the quartz crystal has a thickness of 170 μm the annealing temperature of the assembly should not exceed 200°C [238] to avoid cracking.

There have been several reports about the bonding of ‘quartz wafers’ to silicon [240–243]. The material the authors refer to as “quartz” is in fact transparent fused silica, an amorphous material which is formed at high pressure and temperature from silicon dioxide powder [244], also known as quartz glass. The bonding of fused silica to silicon with subsequent thinning of the silicon leads to a single crystalline silicon film on a transparent insulating layer (silicon-on-insulator). Silicon on fused silica is attractive for microwave devices, image sensors and electroluminescence displays. As in the case of bonding single crystalline quartz to silicon, the difference in the thermal expansion coefficient of fused silica and silicon causes the build-up of stress which may lead to cracking during the annealing step. It has been suggested to bond the wafers by a two-step thermal treatment process [240]. The initial bonding of the plasma activated silicon and fused silica wafer is carried out at 150–450°C, applying a slight pressure. Then the pre-bonded wafers are heated in a vacuum furnace to 850–1250°C to achieve strong bonding. Other authors recommend bonding at room temperature [241] or 80–90°C [242], 100 h storage at room temperature and an annealing at different temperatures which do not exceed 150°C. Recently, a thin layer of silicon has been transferred to a fused silica wafer at moderate temperatures utilising wafer bonding [243]. A silicon wafer was implanted with boron and subsequently with H_2^+ , pre-annealed at 250°C and bonded to a fused silica wafer at room temperature. On heating the bonded pair to 200°C microcracks are formed in the implanted region of the silicon wafer. Finally a thin silicon layer splits from the silicon wafer yielding a fused silica wafer with a thin silicon layer on top [243]. This method is an extension of the ‘smart cut’ approach to SOI and will be described in more detail in chapter 8.

For the microfabrication of chemical-analysis-devices the direct bonding of glass is an interesting alternative to the commonly employed anodic bonding. Polished borosilicate glass wafers bond at room temperature when brought in intimate contact. The bonding energy is increased during a thermal annealing at 350°C [245]. Glass direct bonding has been employed to create a hermetically sealed package [246]. Glass wafers can also be bonded to silicon wafers. If the surfaces are activated in an oxygen plasma strong bonding can be achieved below 350°C [247]. Structured glass substrates have been bonded to a glass cover plate via a thin layer of sodium silicate [248].

6. The bonding of non-silicon materials

6.1. Introduction

Shortly after the discovery that bare as well as oxidised silicon wafers bond to each other when brought into intimate contact, Haisma and co-workers showed that direct bonding is by no means limited to silicon. They presented a detailed investigation on the bonding behaviour of a range of different materials including refractory metals, semimetals, metals, carbides, fluorides, nitrides, oxides and chalcogenides [16] as well as polymers, boron and various magnetic materials [249]. The study underlined that direct bonding is a versatile joining method which can be applied to a large number of materials. Bonding does, however, require a high surface quality in terms of flatness, smoothness and cleanliness. Therefore, the bonding is usually not limited by the materials chosen for bonding but by the attainable surface quality. For every new material to be bonded, a polishing technique has to be developed which yields a peak-to-valley roughness of less than 1 nm [16]. If this can be accomplished room temperature bonding via van der Waals forces or hydrogen bonding should take place. In many cases the bonded pair requires a heat treatment to increase the energy of adhesion. The reactions which take place at elevated temperatures depend on the

species present at the bonding surfaces (and are at the interface after the bonding). Interface reactions occur if reactive groups approach each other within a distance of about 2 Å. Such a reaction may yield volatile products. Depending on the volatile compounds formed and the surrounding material this may or may not cause problems. Hydrogen molecules, for example, usually do not present a problem since they are small enough to diffuse through most materials to the outside. As described in chapter 5, water molecules are not of much concern in silicon direct bonding as long as they are able to diffuse to the bulk silicon where they react to form SiO_2 and H_2 . However, volatile reaction products which do not readily diffuse to the outside and are not consumed by a reaction with the surrounding bulk material, lead to a pressure build-up in the interface which may subsequently push the wafers apart. Evacuated cavities in which volatile products can gather [83,84] or grooves along the interface which extend to the edge of the sample and thus provide an outlet for volatile products [19] are measures to avoid the build-up of pressure in the interface.

One of the great potentials wafer bonding offers is the joining of two are more dissimilar materials to form hetero-structures. The integration of dissimilar materials has attracted increasing attention recently. Particularly the combination of III–V compound semiconductors with the highly developed silicon circuits has been pursued in recent years with the goal to incorporate photonic and high-speed electronic devices with advanced silicon technology. Much of the research in this field has focused on the hetero-epitaxial growth of thin films onto dissimilar substrates. Although major progress has been made in the field of hetero-epitaxial growth, problems persist for many systems including a high density of defects which originate from the lattice mismatch of the combined materials. Additionally, thermally induced strain is frequently observed which is the result of the different thermal expansion coefficients of the joined materials. This strain often deteriorates the device performance. Recently, alternatives to hetero-epitaxy have been developed including epitaxial lift-off (ELO) [42], a technique in which a hetero-epitaxially or lattice-matched grown thin III–V film is transferred to a new substrate by taking advantage of a highly selective chemical etch of a sacrificial buried layer. After its detachment the thin film is transferred to a new substrate on which it sticks reportedly via van der Waals forces. Strictly speaking hydrogen bonding is probably responsible for the sticking of the thin film on the new substrate, as water is present in the interface. The attachment of the film to the new substrate relies on the same physical and chemical phenomena as wafer bonding.

With wafer bonding a new technique has emerged for the integration of dissimilar materials. In recent years numerous non-silicon materials have been joined utilising wafer bonding.

The interfaces of single crystalline dissimilar materials joined by wafer bonding have been in focus of recent studies. Liao, for instance, investigated the strain caused through the lattice mismatch between covalently bonded wafers [250]. Transmission electron microscopy studies were used to optimise the bonding process [251].

Whereas the bonding at room temperature usually proceeds readily if the surfaces are in principle suitable for wafer bonding, one major concern when bonding dissimilar materials is the stress induced during any subsequent heat treatment. The thermal stress is caused by the different thermal expansion coefficients of the materials bonded and may be released by undesired phenomena like debonding, sliding, cracking or the formation of misfit dislocations. Wafer bonding is used frequently to produce thin films of a material on a dissimilar substrate. To achieve this, one of the two materials bonded to each other is thinned to the desired thickness after bonding. If one component of the bonded pair is sufficiently thin, the thicker partner is able to bounce back leaving the entire stress in the thin film. If the thickness of the thin film is below a critical thickness the formation of misfit dislocations is prevented. Below a critical temperature plastic deformation of the

thin film will not take place. From this, simple rules for the fabrication of a thin film on a dissimilar substrate through wafer bonding can be derived:

- The lowest possible annealing temperature should be chosen to prevent any of the undesired phenomena mentioned above.
- The annealing temperature should be high enough to yield strong adhesion which is sufficient for the wafer pair to withstand the subsequent thinning step.
- The thinning should proceed down below a critical value which is characterised as the thickness required to avoid the formation of dislocations at the maximum device processing temperature.

6.2. Wafer bonding of III–V compound semiconductors

Bonding of a III–V compound semiconductor to another material was described as early 1974 [41] and thus long before the first papers on silicon direct bonding were published. At this time Antypas et al. reported the fabrication of a glass-sealed GaAs–AlGaAs transmission cathode. They prepared a GaAs/GaAlAs/GaAs/GaAlAs hetero-structure by liquid-phase epitaxy. The last-grown GaAlAs layer then was fusion-bonded to a glass substrate which possesses a similar thermal expansion coefficient as GaAs. Removal of the top GaAs layer, followed by stripping off the uncovered GaAlAs layer using wet chemical etching yields a hetero-structure consisting of GaAs/AlGaAs/glass with an excellent layer morphology, uniform thickness, and good photocathode performance. Meanwhile, numerous examples of bonding III–V semiconductors to themselves or to other materials have been reported and will be briefly discussed.

A procedure for the bonding of III–V materials which has been adopted with little changes by many groups working in this field, was reported by Liao et al. in 1990 [43]. The surfaces to be joined are thoroughly cleaned and contacted at room temperature. Liao carries out the annealing step in a graphite assembly which fits closely into a cylindrical quartz container (Fig. 42) [43]. Upon heating the wafers are pressed together due to the different thermal expansion coefficient of quartz and graphite. The disadvantage of this assembly is that the actual pressure applied during bonding is difficult to ascertain, and thus it is almost impossible to reproduce the bonding conditions. Since

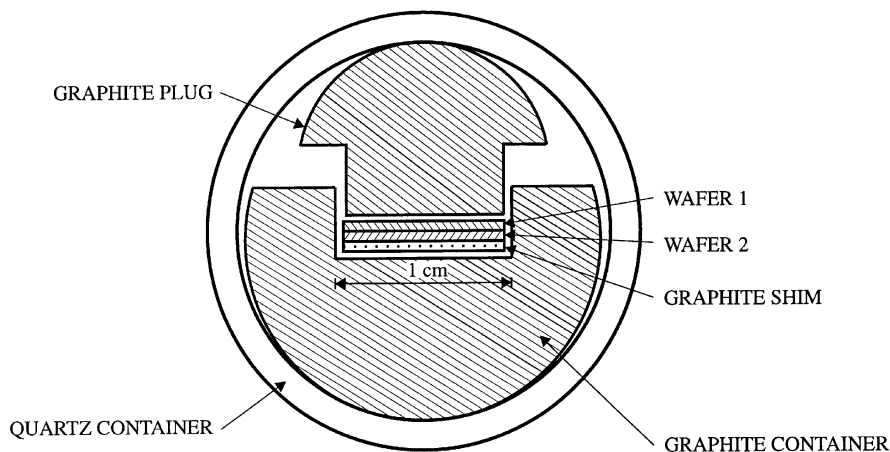


Fig. 42. Schematic drawing of a wafer fusion reactor for the bonding of III–V semiconductor compounds. Due to the different thermal expansion of graphite and quartz the wafers are pressed together (after Ref. [43]).

detailed studies on the necessary bonding conditions have not been reported so far, it is unclear whether pressure is really a necessity for bonding III–V compound semiconductors.

Typically, the annealing step is carried out in a hydrogen atmosphere to prevent the formation of volatile group III or group V oxides. Patriarche et al. report that the use of nitrogen as process gas yields similar results [251].

6.2.1. GaAs/GaAs

Gallium arsenide direct bonding is expected to increase the flexibility of many device fabrication processes and thus research in this field has been pursued in recent years. Gallium arsenide crystals have been bonded via an intermediate Ge alloying layer as early as 1973 [252]. However, a direct adhesion between two GaAs wafers was first described in 1988. The wafers were treated in hydrochloric acid, contacted at room temperature in air and annealed at 850°C for 1 h in a hydrogen atmosphere [253].

Strong adhesion can be achieved by annealing two room temperature bonded gallium arsenide wafers at 400–420°C in hydrogen atmosphere [254]. Other authors describe the side-by-side lateral direct bonding of a pair of cleaved GaAs facets [255]. After annealing at 700°C in a H_2/AsH_3 ambient strong bonding is observed. The bonded interface does not form an electrical barrier. Non-linear optical material has been prepared by the formation of stacked GaAs-plates through direct bonding at 850°C in a hydrogen/nitrogen gas mixture [256–258]. Although the 850°C 2 h annealing had been found to yield good bonds, the overall device performance can be degraded, for instance due to a loss of arsenic [259]. Graphite holders for pressing the GaAs samples during bonding were preferred over sapphire or quartz holders as those reportedly tended to bond to the sample [259].

Fig. 43 shows a cross-sectional transmission electron micrograph of the bonding interface of two GaAs wafers. A thin amorphous layer, presumably consisting of group III or group V oxides, is visible [260].

6.2.2. Si/GaAs

The direct bonding of silicon to gallium arsenide has attracted much interest as it may produce structures in which photonic and high speed electronics can be combined with the advanced silicon technology. The epitaxial growth of gallium arsenide onto a silicon substrate is hampered by the 4.1% difference in the lattice constants of both materials. This large lattice mismatch frequently leads to the formation of threading dislocations which severely degrade the device performance. As the difference in lattice constants is of no concern in wafer bonding, direct bonding of silicon and

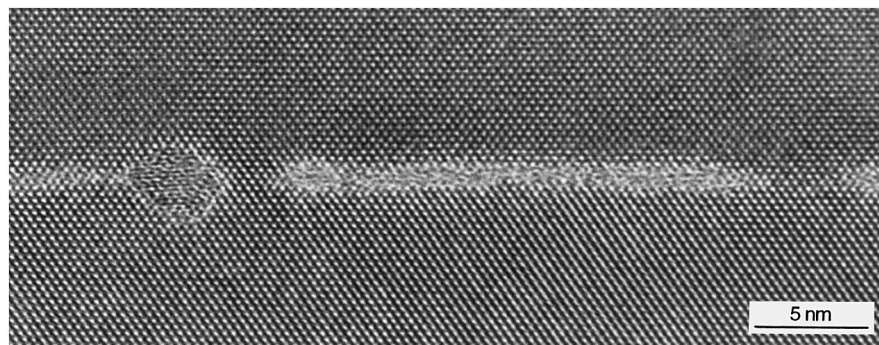


Fig. 43. Cross-sectional TEM micrograph of the bonding interface of two gallium arsenide wafers bonded in a hydrogen atmosphere at 400°C. The thin amorphous layer presumably consists of oxides [260] (micrograph courtesy Dr. R. Scholz, MPI Halle).

gallium arsenide is an attractive method to produce gallium arsenide layers integrated on a silicon substrate. Unfortunately, the considerable mismatch in thermal expansion coefficient limits the temperature to which a bonded Si/GaAs pair can be exposed. Bonding gallium arsenide to a silicon-on-sapphire substrate obviates the problem because of the similar thermal expansion of gallium arsenide and sapphire [435]. Bonding of gallium arsenide to silicon and oxidised silicon has been reported by several research groups [16,68,261]. The bonding can be carried out using the micro-cleanroom set-up described in chapter 3 [68]. The authors report that the wafers debond if the pair is heated above 160°C and explained this behaviour with the formation of thermal stress upon heating due to the large mismatch in thermal expansion [68]. Thinning of the GaAs layer can reduce the magnitude of the maximal stress [262]. The epitaxial lift-off method has been used to bond a thin GaAs film, which has been removed from its original substrate, to a glass or oxidised silicon substrate [261]. The film with a thickness of 1 µm remained attached to the oxide if the temperature changes are kept below 50°C. If the temperature is further increased the thermal stress exceeds the bonding shear strength and the film slips at the bonding interface which is indicative of a relatively low energy of adhesion [261].

If a gallium arsenide film is lifted off its original substrate and transferred to a processed silicon IC chip the direct bonding is hampered due to a lack in planarity of the processed chip [263].

A bonding method which yields strong adhesion between Si and GaAs at room temperature has been reported recently [203,264]. Silicon and gallium arsenide pieces are introduced in a UHV-chamber, the surface is cleaned and activated in situ with an argon fast atom beam and the pieces are pressed together applying an uni-axial force. Strong bonding at room temperature is achieved. Unlike in the case of Si/Si bonding in UHV, here pressure reportedly is a necessity.

Gallium arsenide films can be transferred to silicon by making use of the smart-cut process [265]. Hydrogen is implanted in a certain depth into a gallium arsenide wafer which is subsequently bonded to a silicon wafer. No details were given how GaAs was bonded to silicon and how the problem of differing thermal expansion was overcome. Low temperature bonding or low viscosity glass layers may be a possibility. On annealing at moderate temperature blisters are formed in the implanted region and finally the gallium arsenide wafer splits apart, yielding a silicon wafer with a thin layer of gallium arsenide.

6.2.3. *AlGaInP/GaP*

Recently, wafer bonding has been successfully employed in the fabrication of LEDs. Visible light emitting diodes (LED) consisting of AlGaInP on gallium phosphide exhibit outstanding luminous efficiencies that exceed that of all other current LED technologies in the yellow–green to red spectral range [266]. The AlGaInP layer is grown onto a gallium arsenide substrate by MOCVD. Using conventional chemical etching the substrate is removed and the exposed layer is subsequently joined with a gallium phosphide substrate by utilising wafer bonding at elevated temperature and uni-axial pressure [266–270]. Reportedly, N₂ or H₂ ambient had been used. No details were given how the surface had been prepared for bonding and how bonding was performed.

6.2.4. *GaAs/InP*

Various studies have been devoted to the fabrication of optical devices, which operate at long wavelengths, through wafer direct bonding [19].

The materials gallium arsenide and indium phosphide have a lattice-mismatch of 3.8%. When hetero-epitaxy is used to produce structures with such strongly lattice-mismatched materials, frequently a high density of threading dislocations is formed throughout the sample. Threading dislocations may degrade the device performance severely.

To join GaAs and InP through wafer bonding, Liao et al. introduced a quartz/graphite reactor in an H_2 -ambient [43]. In the meantime numerous groups have reported the fusion of GaAs and InP, most of them adopting the procedure reported by Liao et al. Typically, the surfaces are cleaned, etched to remove the native oxide by a dip in acid, joined at room temperature and finally heated to 600–700°C in hydrogen. Usually, the wafers are pressed together during the annealing step to ensure close contact [19,271–277]. Babic et al. emphasised the importance of an array of channels (widths: 2–10 μm ; pitch: 150 μm) which are etched in one or both substrates before bonding [19]. These channels which extend to the end of the sample serve as an outlet for gaseous interface reaction products. When the sample is cleaved after the annealing step, a dense liquid is recovered [19], whose chemical composition is unknown. If the bonded samples are annealed without creating channels prior to bonding, macroscopic voids and oxide islands are formed in the interface. Meanwhile other groups have adopted this method [277]. Patriarche et al. have studied the interface of bonded GaAs/InP hetero-structures by transmission electron microscopy [251,278]. They found three dislocation networks in the interface. Threading dislocations throughout the sample, as they are frequently observed when employing hetero-epitaxy, reportedly were totally eliminated when using wafer bonding as joining technique for GaAs and InP. One dislocation network in the interface accommodated both the lattice mismatch and the inevitable twist between the two crystals. The second network results from the slight tilt angle of the two surfaces. The third dislocation network is comprised of proper 60° dislocations, irregularly distributed and with an average spacing of about 1 μm . Unlike the other two networks the third one did not lie in the interface, and hence it could not react with the other two. It has been intimated that the third network results from the plastic partial relaxation of the thermal mismatch developed during cooling down to room temperature [251].

6.3. Sapphire wafer bonding

Most reports on the bonding of sapphire deal with the formation of hetero-structures between silicon and sapphire on the one hand and gallium arsenide/sapphire on the other hand. However, other material combinations have also been obtained through bonding, including sapphire/sapphire, sapphire/ SrTiO_3 and sapphire/ LaAlO_3 [279,280]. However, we will limit our discussion to the former material combinations.

6.3.1. Sapphire/Si

Sapphire is an electrical insulator with a high thermal conductivity. Thin monocrystalline layers of silicon on sapphire (silicon-on-sapphire (SOS)) are used as substrates in high power microwave monolithic integrated circuits and radiation-hard devices [281,282].

Because of difficulties inherent in the hetero-epitaxial growth of silicon on sapphire, wafer bonding recommends itself for the preparation of Si/sapphire hetero-structures. Sapphire wafers exhibiting a sufficient surface quality can be readily joined with clean silicon substrates through wafer bonding at room temperature. However, due to the different thermal expansion coefficients the bonded wafer pair reportedly cannot be heated to temperatures above 200°C [281] or 270°C [282] without the cracking of one of the wafers. Nevertheless, after annealing the pair at these moderate temperatures, the bonding is strong enough to withstand thinning of the Si-layer down to 10 μm [281,282]. Wang et al. report the fabrication of N-channel metal oxide semiconductor films that were bonded onto sapphire substrates [283]. The thermomechanical strain which is formed upon annealing of a bonded sapphire/silicon wafer pair has been investigated [284].

6.3.2. Sapphire/GaAs

As gallium and sapphire have quite similar thermal expansion coefficients, bonded sapphire/GaAs wafer pairs can be annealed at elevated temperature without the build-up of excessive thermal strain [285]. At elevated temperatures the formation of macroscopic bubbles in the interface has been observed [285,286]. Fig. 44(a) shows a cross-sectional transmission electron micrograph of an interface region with a bubble which is filled with an amorphous material. The chemical composition of the phases formed in the interface upon annealing has been determined by X-ray diffraction. The bubbles are reportedly filled with γ -Ga₂O₃ and elemental arsenic [286]. In Fig. 44(b) a plane-view transmission electron micrograph of an area with larger voids is shown. The grey contrasts represent bonded areas along the (100) direction of GaAs. The bonded areas are separated by channels which show strong bending contours. The formation of channels can be seen as an indication that during annealing mass transport takes place in the interface. Bubble-free bonding can be achieved by bonding and annealing the wafers in a hydrogen ambient [285].

6.4. Bonding of silicon carbide

Silicon carbide (SiC) is a wide-band-gap material for high-temperature, high-speed, power and radiation applications. It is also used as a substrate for the epitaxial growth of GaN-layers in the fabrication of blue-light emitting diodes and lasers. Since single-crystalline SiC is an expensive material it would be highly desirable to develop methods which allow the fabrication of thin SiC layer on cheaper substrates like silicon, sapphire or polycrystalline SiC. One approach to thin single-crystalline SiC layer transfer involves the growth of SiC on silicon by chemical vapour deposition and subsequent transfer onto oxidised silicon by wafer bonding [231,287]. Recently, SiC layer transfer has been accomplished by a procedure which uses wafer bonding and a subsequent layer splitting of a hydrogen implanted SiC layer (smart cut) [288–290]. The latter approach yields 6H- or 4H-SiC layers of a quality comparable with that of bulk single-crystalline SiC wafers. The polishing

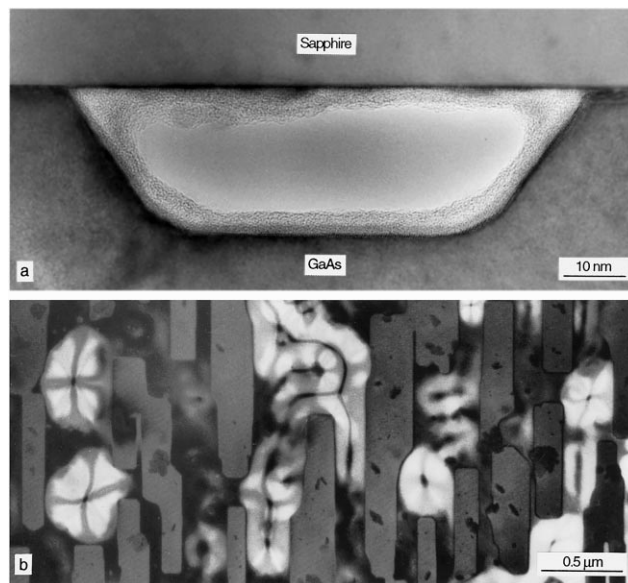


Fig. 44. Gallium arsenide/sapphire bonding. (a) Cross-sectional transmission electron micrograph of a bubble formed at the bonding interface. The bubble is filled with an amorphous material. (b) Plane view transmission electron micrograph of an area with voids and channels (after Ref. [285], with kind permission of the authors).

of SiC surfaces down to a roughness suitable for direct bonding presents a problem. The material is very hard and the state of the art polishing technique presently only yield a rms roughness of about 2 nm for SiC. Thus, intermediate bonding layers consisting of silicon dioxide or polysilicon are typically deposited onto the SiC surface before bonding. These intermediate layers can be polished down to a rms roughness of 0.5 nm and are thus readily bondable.

6.5. Bonding of ferroelectric materials

Recently, efforts have been undertaken to apply wafer bonding to ferroelectric materials. Research in this field is aimed at the formation of stacked structures and fabrication of new material combinations. Particularly, the integration of ferroelectric material into semiconductor technology is of interest.

Haisma reported the room temperature bonding of BaTiO₃ and LiNbO₃ in 1994 [16]. LiTaO₃ [291] as well as LiNbO₃ [292] single crystals have been joined by wafer bonding. The joining of both materials with each other has also been reported [293]. After cleaning the surfaces using a SC1 cleaning solution (see chapter 3), the crystals are joined at room temperature and subsequently heated to 350°C to increase the adhesion. LiTaO₃ or LiNbO₃ can be bonded to silicon wafers at room temperature. An annealing step at 200–500°C in nitrogen ensures strong bonding [294]. Heterostructures comprised of silicon and Bi₄Ti₃O₁₂ (BiT) or Pb(Zr, Ti)O₃ (PZT) have also been produced by wafer bonding [295,296]. Thin films of BiT or PZT were deposited onto a silicon wafer using chemical solution deposition and subsequently crystallized by rapid thermal annealing. The films were polished to prepare a smooth surface suitable for wafer bonding and directly bonded to a silicon wafer. Through a subsequent annealing step the adhesion is increased. The silicon handling wafer is removed by etching and polishing, so that a metal–ferroelectric–silicon structure is obtained. The bonding interface was characterised by cross-sectional transmission electron microscopy. Fig. 45(a) shows a cross-sectional TEM micrograph of a PZT film deposited directly onto silicon with subsequent heat treatment by rapid thermal annealing (RTA) [296]. PbO apparently has diffused into the silicon where it reacts with the host to yield an amorphous intermediate layer of PbSi_xO_y, and leaving voids in the PZT layer. Fig. 45(b) shows a cross-sectional HRTEM-micrograph of the interface formed upon bonding of a PZT film on silicon and subsequent annealing. The amorphous interlayer is caused by the native silicon oxide present on the silicon surface prior to bonding [296].

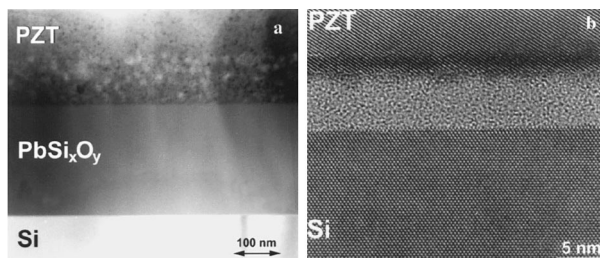


Fig. 45. Lead zirconium titanate (PZT) deposited from metallo-organic precursor solution onto silicon [296]. (a) Cross-sectional transmission electron micrograph of a PZT-film deposited directly on silicon and crystallized by rapid thermal annealing at 700°C for 60 s. The reaction of lead oxide and silicon caused a thick amorphous PbSi_xO_y interphase and voids in the PZT layer. (b) Cross-sectional high-resolution transmission electron micrograph of a bonded PZT/Si interface. The PZT layer had been crystallized on a sacrificial silicon wafer and then was transferred through bonding. As indicated by the different scales, only a thin amorphous interphase formed in this case and a high-quality ferroelectricum/silicon structure is obtained (reproduced with kind permission of the authors).

6.6. Bonding of magnetic materials

The bonding of magnetic materials was first reported by Haisma et al. who joined the permanent magnetic compound $\text{Sm}_2\text{Co}_{17}$ with fused silica and soft magnetic material CoFe by wafer bonding [249]. Recent efforts have focused on the bonding of magneto-optic crystals to III–V compound semiconductors. Totoki et al. have studied the bonding of the magnetic garnet $\text{Gd}_3\text{Ga}_5\text{O}_{12}$ (GGG) to InP [297–300]. The samples were cleaned, contacted at room temperature and annealed in an H_2 -ambient at 450–750°C. The rare earth iron garnet $(\text{LuNdBi})_3(\text{FeAl})_5\text{O}_{12}$ (LNB) grown on GGG also has been bonded to III–V compound semiconductors [301].

6.7. Miscellaneous materials

Other interesting material combinations joined by direct bonding include diamond/GaAs pn-junctions [302,303], a buried C_{60} layer between silicon wafers [304] and silicon/zinc sulphide for composite IR windows [305]. Polymeric materials including polymethylmetacrylate (PMMA), polyacrylate, polyimide and polycarbonate have been bonded to themselves, to other polymeric materials and to inorganic substrates like silicon and fused silica [306,307].

6.8. Wafer bonding via intermediate layers

Several low temperature bonding methods utilising intermediate layers including metals, glass or organic compounds of variable thickness have been reported in recent years. Problems associated with reliability, stability, thermal stress or incompatibility with IC technology have until now prevented a broad application of bonding via interlayers. Nevertheless, for some application the bonding through interlayers represents an interesting alternative to conventional bonding, particularly since it is usually less demanding on surface topography and cleanroom environment. Although some of these methods do not exactly fulfil the criteria for direct bonding, they will be discussed briefly.

6.8.1. Metal interlayers

One of the methods described is based on eutectic bonding between silicon and gold. A thin layer of titanium (which acts as adhesion promoter) and subsequently 1.2 μm of gold is deposited on thermally oxidised silicon wafers. The wafers are brought into contact and heated above the Si/Au eutectic temperature of 362°C. Strong bonding is obtained [308]. One of the drawbacks of this technique is the fact that gold atoms readily diffuse into the silicon lattice and strongly influence the electronic properties.

Silicon wafers with a thin layer of titanium bond firmly to each other when heated to 700°C in an oxidising atmosphere [309]. The bonding is believed to be based on the formation of an interfacial titanium silicide layer. A similar reaction occurs if a silicon wafer with a native oxide layer is bonded to another silicon wafer which has a thin tantalum layer on top of a thermal oxide [310]. The buried metal layer is used as a low-resistive layer for bipolar transistors.

6.8.2. Glass interlayers

Glasses exhibiting a low melting point including boron oxide [311–313] and borophosphosilicate glasses (BPSG) [109] have been used as intermediate layers for low temperature bonding. The glass layer is deposited onto silicon wafers by spin-coating or spraying. After the bonding at room temperature the wafer pair is heated above the flow temperature (typically 200–

400°C) of the glass. Upon cooling to room temperature the wafers are firmly joined. There are several explanations for the increase in energy of adhesion in the presence of glass layers. Water is known to diffuse very fast through these glasses which may accelerate the condensation reaction of interface silanol groups [109]. Moreover, the condensation reaction may be further enhanced due to the presence of boron and phosphorous [109].

Strong adhesion at low temperature can also be achieved by depositing a thin layer of sodium silicate [169,314,315]. For low temperature wafer bonding layers which possess thicknesses of 7–80 nm were deposited by spin-coating of highly diluted aqueous sodium silicate solutions. After contacting two pre-treated wafers the wafer pair was annealed at 150–300°C and strong bonding was obtained.

The joining ability of sodium silicate is well-known and widely used [316,317]. Sodium silicate layers are thought to planarise the wafer surface leading to a reduced microscopic roughness [314,315]. Additionally, alkali ions like sodium may facilitate the condensation reaction of silanol groups [314,315]. Another interesting effect which alkali ions have in silicon chemistry is that they catalyse the reaction between silicon and water to yield silicon dioxide and hydrogen [318]. As a consequence, when carrying out silicon wafer bonding in the presence of an intermediate layer containing alkali ions, the water which diffuses out of the interface is readily consumed through the reaction with bulk silicon at low temperature. The overall condensation rate of silanol groups increases. Ammonium silicate [169,314] and aluminium phosphate [314] layers also have been used in low temperature silicon bonding. Unfortunately, the mobile alkali ions present in glasses often are incompatible with IC-technology. Sodium silicate layers also have been employed in the low temperature bonding of glass parts for the microfabrication of chemical analysis devices [248].

6.8.3. *Organic interlayers*

Intermediate layers consisting of polymers are another attractive alternative for low temperature bonding. They offer several advantages including a low bonding temperature (usually below 200°C), the absence of any metal ions which could alter the electronic properties, a very high fracture surface energy and the possibility to relieve stress due to their elastic properties. If layers consisting of polymethylmetacrylate (PMMA) are spin-coated onto silicon wafers prior to bonding high fracture surface energies are reached upon annealing the wafer pair at 180°C [319]. PMMA is a thermoplastic, insulating and transparent polymer and is readily soluble in organic solvents. The polymer layer applied exhibits a thickness of about 1 µm. The solvent has to be removed from the layer by a pre-annealing step prior to bonding. The compound is photo-patternable and thus selective bonding of certain wafer areas by bonding patterned PMMA films can be achieved. Other polymers which have been used in low temperature bonding are negative photoresist, polyimide and epoxy [320]. The layers are spin-coated onto silicon substrates; the thickness varies between 130 nm and 1 µm [320].

7. **Electronic properties**

As we have seen, wafer direct bonding can form mechanically robust metallurgical junctions between like or different materials. The bonding seam may be associated with an interphase, as which for instance one can regard the silicon oxide layer between bonded hydrophilic silicon wafers, or the bonding seam may best be described as a grain boundary between two more or less misaligned 'grains'. High-temperature annealed silicon wafers joined through hydrophobic bonding would be an example for the latter case. The mechanical stability of the joint is not the only parameter to be considered for device applications. Devices located in the neighbourhood of the joint may be

influenced by elastic stresses resulting when two surfaces are brought into mutual conformity, or by charges trapped in the joint. A case in point would be silicon-on-insulator wafers where such concerns could be raised. On utilising the freedom in combining materials without many of the restrictions imposed on more conventional approaches, the joint may even be integrated into the device, for example electrical contacts or pn-junctions. The viability of such schemes strongly depends on the electronic and electric properties of the bonding interface.

In general, the spectrum of electrical properties observed strongly resembled the variety of electrical properties known of grain boundaries in covalent crystals [218]. Intrinsic and extrinsic factors together determine the electronic structure of the interface. Because of the unavoidable misorientation of the two ‘grains’, not all atoms of the boundary can satisfy their ideal bonding configurations, resulting in distorted or broken (dangling) bonds. This structural frustration constitutes the intrinsic cause why the electrical properties of bond interfaces differ from the bulk properties. Impurities in the bonding seam are the extrinsic origin of the electronic states associated with a bonding interface. Those impurities may be present on the wafer surfaces prior to bonding or they may segregate to the boundaries after the initial contacting of the wafers. The extrinsic sources of electronic interface states may be the cause of the differing observations made. How significant intrinsic sources are to the potential barrier formation has not been resolved conclusively [218]. The effect charges, irrespective of their extrinsic or intrinsic origin, have on transport across charged semiconductor grain boundaries has been simulated recently [321–324].

Here, we will briefly summarise the main electronic characteristics of bonded interfaces studied, first for the silicon/silicon system, then for the III–V/III–V compound semiconductor system. Bengtsson [14], for instance, has reviewed the early work on the electronic properties of bonded silicon wafers.

7.1. Silicon bonding

7.1.1. Charge trapping in the bonding seam of hydrophilic silicon wafers

For real surfaces are not perfectly oriented and two wafers are never ideally aligned, the bonding interface incorporates structural defects. Additionally, in spite of meticulous cleaning, the interface of a bonded sample generally will contain a higher concentration of contaminants than the bulk crystal: First, the structural defects make the interface to a precipitation or gettering site, as has been shown for instance for oxygen, gold and copper [325–328], and secondly, adsorption of gaseous species onto the wafer surfaces prior to bonding cannot be eliminated completely. A notorious example of an electrically active contaminant of the silicon surfaces is boron (Fig. 46), giving rise to a p-type interphase between n-type wafers [329]. This boron contamination has been known from the boron spike between an silicon epilayer grown by molecular beam epitaxy (MBE) and its substrate [330]. At the interface between directly bonded hydrophilic silicon wafers, approximately $1 \times 10^{12} \text{ cm}^{-2}$ boron has been found, in agreement with observations in Si MBE studies [329–331]. The origin of the boron contamination most likely has to be sought in atmospheric contamination where boric acid (H_3BO_3) represents the major fraction of boron-containing species [332]. In particular, high efficiency particulate air (HEPA) filters used in cleanrooms and in wet benches reportedly are sources of boron [333]. Boron in its compounds has an affinity for silicon dioxide with which upon dehydration it can form Si–O–B bonds [334] which, however, are hydrolytically unstable [335]. Hence storing the wafers under water, or thorough rinsing may assist in minimising the contamination with boron originating from airborne species. With the oxide layer removed, hydrophobic silicon surfaces consequently exhibit a strongly reduced boron surface coverage [330,336,337].

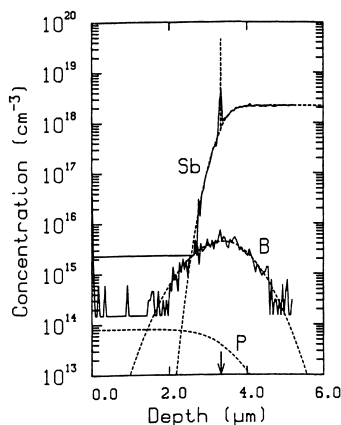


Fig. 46. The SIMS profiles of antimony and boron across an interface (marked with an arrow in the graph). The broken lines represent a simulation of the dopant profiles while the solid lines are the experimental data. Two n-type (111) oriented Si wafers, one doped with phosphorus, the other with antimony, had been bonded and annealed [329].

Charge trapping at the bonding interface of hydrophilic silicon wafers was investigated using standard capacitance–voltage techniques, on MOS or Silicon–Insulator–Silicon (SIS) structures; for a review, see Ref. [14]. For the characterisation of interfaces between hydrophobic wafers with the oxide layers removed in aqueous hydrofluoric acid, this technique had not been found applicable. The MOS structures employed were fabricated by selectively etching off the upper silicon layer onto the interfacial oxide layer, exposing the silicon oxide layer to various chemicals prior to metallisation. SIS structures offer the advantage that they are less susceptible to a change in the oxide charges during sample preparation [338]. Fig. 47 compares the SIS structure to the MOS structure.

From capacitance–voltage measurements, an areal density of ca. 4×10^{10} – $2 \times 10^{11} \text{ cm}^{-2}$ negative charges was deduced [106,339–341]; there is some controversy whether the charges did not form a sheet charge at the bonding interface but were distributed uniformly across the oxide thickness [340] or not [342]. The origin of the negative charges was attributed to electron traps which were ascribed to Si–O–H groups from water in the oxide, resulting from the condensation reaction during annealing [340,343]. The incorporation of hydrogen into the oxide was given as an explanation for the enhancement of hole trapping in bonded oxide layers compared to non-bonded oxide layers, seen in Fig. 48 [343].

In addition to the charges intrinsic to the hydrophilic bonding process, charges resulting from contamination of bonded interfaces need to be taken into account, as for instance discussed above for boron. Such contaminants reportedly formed large amounts of fixed charges or donor-type interface

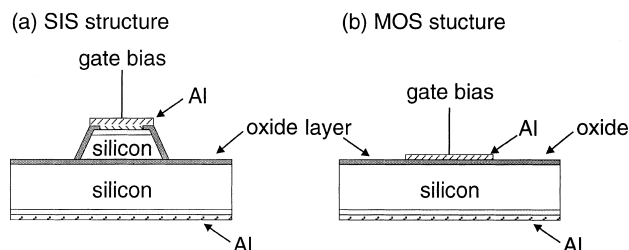


Fig. 47. Schematic cross-section of an SIS structure (a) and a MOS structure (b) [338].

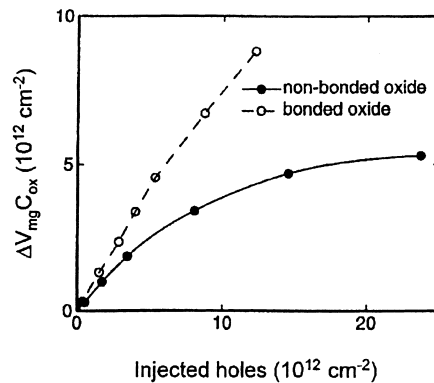


Fig. 48. Hole trapping in 100 nm dry thermal oxide before and after bonding [343]. After bonding, the wafers were annealed at 1100°C, thinned and, following metallisation, annealed at 350°C.

traps; the interface trap concentration could be considerably reduced through annealing at 1100°C [340,341].

The minority carrier lifetime generally is reduced through the recombination centres associated with the bonding seam. This has implications for device applications, with for example power device fabrication taking advantage in adjusting the minority carrier lifetime.

7.1.2. Charge transport across bonded interfaces

Charge transport across the bonding interface has been investigated for hydrophilic silicon (with native or very thin thermal oxide) as well as for hydrophobic silicon. The simplest system to consider are unipolar structures of n/n- or p/p-type. Frequently, non-ohmic current–voltage characteristics had been observed across those isotype junctions. Charged electronic levels at the interface or in the interphase cause potential barriers which restrict the charge transport across the bonding seam [14,218]. There is ample evidence that ohmic conduction across the bonding seam can be attained when suitable measures are taken to reduce or eliminate the extrinsic sources of interface charges. In the case of hydrophilic silicon interfaces, it had been implied that after thermal dissolution of the silicon oxide interphase an interfacial potential barrier was absent [44,344]. These authors observed ohmic current–voltage characteristics for bonded p⁺ (0.002 Ω cm) (100) oriented Si wafers, from 0.22 to 110 A cm^{−2} current density.

Ohmic current–voltage characteristics were achieved more consistently when, prior to bonding, the silicon oxide layers had been etched off in an aqueous solution of hydrofluoric acid, as first demonstrated by Bengtsson and Engström [153]. Fig. 49 compares the current–voltage characteristics of n/n-type junctions prepared through hydrophilic or hydrophobic bonding and subsequent annealing [153]. Post-bonding annealing of n-type or p-type unipolar junctions at 400°C for 9 h or 24 h [345], at 600°C, 700°C or 1000°C [346,347] or at 1100°C [153,348] resulted in ohmic current–voltage characteristics from which no potential barrier could be inferred. However, annealing at 800°C was found reproducibly to cause non-linear current–voltage characteristics at room temperature [346,347]. The height of the potential barrier was reportedly 0.1 V. Its origin was either sought in the activation of interfacial boron [347], or in some analogy to the emergence of so-called ‘new donors’ of Separation-by-Implantation-of-Oxygen (SIMOX) material [346].

It has also been attempted to reduce the intrinsic sources of an interfacial potential barrier. Before the wafers were brought into contact, a regular square array of grooves with a pitch of ca. 200 μm was etched into one of the bonding partners [349–352]. During annealing, the grooves

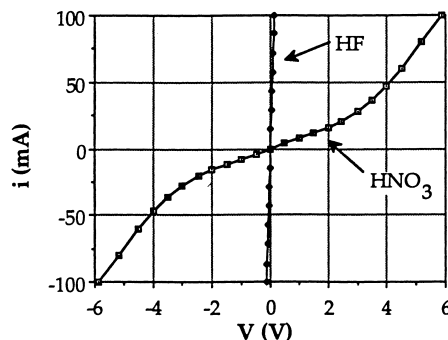


Fig. 49. Comparison of the current–voltage characteristics. After hydrophilic bonding (marked HNO_3) or hydrophobic bonding (marked (HF), the samples had been annealed at approximately 1100°C [153].

reportedly acted as sinks for the dislocations, as schematically shown in Fig. 50. No electrical characterisation of unipolar junctions had been provided; however, the current–voltage characteristic of a pn-junction had been reported [349].

pn-junctions were fabricated through the bonding of p-type wafers with n-type wafers. For the electrical characteristics of junctions made by bonding hydrophilic wafers, see [14,353] and references therein. In the case of bonding hydrophobic silicon, Kub et al. report a low reverse leakage current density of ca. 40 nA cm^{-2} [347]. For pn-junctions made through the bonding of hydrophobic and grooved silicon surfaces with subsequent annealing at 1100°C , current densities of ca. 250 A cm^{-2} at a forward bias of ca. 1.5 V were reported [349,352,354]. After thermal desorption

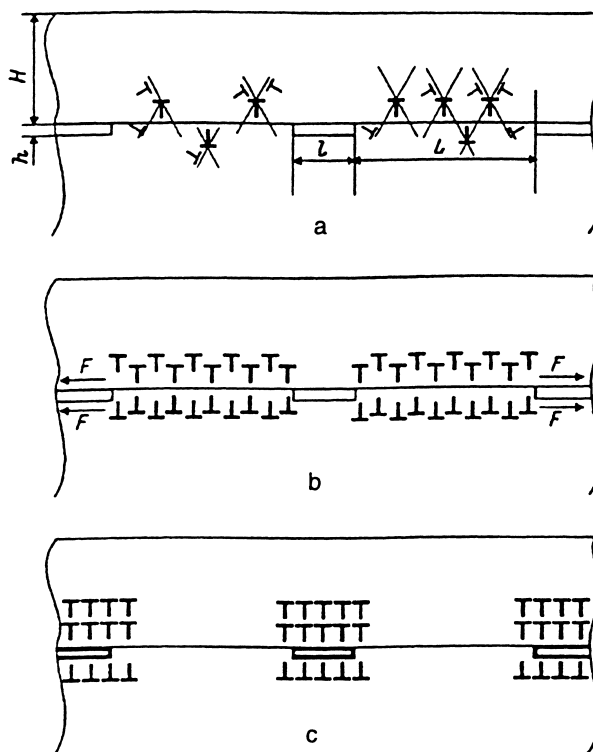


Fig. 50. Cross-section through a bonded wafer pair, schematically explaining the proposed dislocation gettering. Nucleation (a) and evolution (b,c) of the interfacial dislocations during annealing [351].

of the hydrogen passivation in ultra-high vacuum, Hobart et al. bonded their wafers at 400°C and reported a reverse leakage current density of ca. 100 nA cm⁻² and a diode ideality factor of about 1.2 [201,212].

7.2. III–V Compound semiconductor bonding

The combination of III–V compound semiconductors has been particularly attractive in situations of mismatched materials where epitaxy would have compromised the opto-electronic properties through a high density of threading dislocations. Most authors report that their wafer-bonded hetero-interfaces are free of threading dislocation which could degrade devices layers in the vicinity. Moreover, when studying devices transferred via wafer bonding to another substrate, the device performance usually did not deteriorate noticeably [266,271,272].

Key to the viability of incorporating the wafer-bonding interface into a device, often is a low electrical resistance across the bonded hetero-junction. Therefore, the current–voltage characteristics of a variety of hetero-junctions formed through wafer bonding has been investigated. Studies of GaAs/InP and GaP/GaInP hetero-junctions of either p- or n-type as well as n-GaAs/n-GaAs and p-GaInP/p-GaInP homojunctions reported no consistent behaviour for the electrical resistance of the bonding interface [255,276,277,355–357]. In some cases ohmic conduction was observed, in others the current–voltage characteristics were distinctly non-linear. The quality of the bonding may cause the large discrepancies, as some authors mention amorphous interphases, whereas others observe atomically sharp crystalline interfaces, often with misfit dislocations accommodating the lattice mismatch at the hetero-junction [255,271,274–276,355,356]. In addition, it has been convincingly demonstrated that for a bonding procedure yielding consistently a good structural bond quality, the variation of the relative orientation between the wafers alone can account for the changes in electrical properties [356,357]. Experimentally, it was found that low-resistance ohmic conduction can be achieved if the relative misorientation between the mating crystals was kept below ca. 4° in any direction; with increasing misorientation, also the degree of non-linearity increased, apparently saturating for misorientations larger than 15–20°, as illustrated in Fig. 51 [357]. Electrically charged dislocations or extended dislocation structures were seen as the cause of the non-ohmic majority carrier transport [356,357]. Srikant et al. studying the electron transport across low-angle pure tilt grain boundaries phenomenologically with quasi-classical molecular dynamics simulations elaborated this line of thought, and found a critical misorientation angle of about 2.6°. They attributed the diminished electrical conductivity to the increasing density of charged edge dislocations [321,322]. From the study of homo- and hetero-interfaces, it had been concluded that bonded interfaces with insufficient relative crystallographic alignment of the two wafers exhibit a

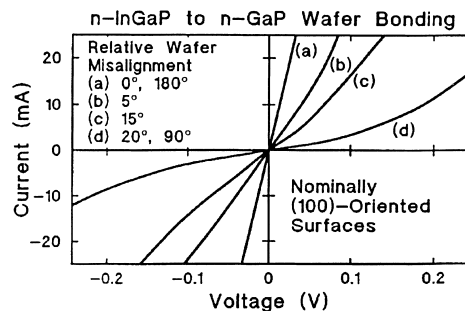


Fig. 51. Twist angle dependence of the current–voltage characteristics of n-GaP/n-Ga_{0.5}In_{0.5}P heterojunctions ($\approx 500 \times 500 \mu\text{m}^2$ die area) [357].

high electrical resistance, whereas well-aligned wafers formed low-resistance ohmic contacts irrespective of ‘any shift of composition or lattice constant that may exist across the wafer-bonded interface’ [270,356]. In its generality this statement is surprising as lattice mismatch clearly can result in misfit dislocations, and edge dislocations accommodating the lattice mismatch indeed have been observed [356]. For the (100) surfaces studied, networks of edge or screw dislocations with Burgers vectors, b , of the $a/2 \langle 110 \rangle$ -type would accommodate mismatch caused by pure lattice misfit or pure tilt misorientation on the one hand, or pure twist misorientation on the other. The spacing of the dislocations, d , approximately is given by $d_{\text{misfit}} = a_1 a_2 / \sqrt{2}(a_1 - a_2)$ with a_1, a_2 the two lattice constants, by $d_{\text{tilt}} = b/\omega$, with b being the modulus of the Burgers vector and ω the small tilt angle, or by $d_{\text{twist}} = b/\theta$, with θ being the small twist angle. Therefore the experimentally observed critical misorientation of 4° would translate into a relative misfit $(a_1 - a_2)/a_2$ of ca. 7%, a regime of misfit for which no data have been provided.

Although the electronic properties of the interface also depend on the conduction and valence band discontinuities at the wafer bonding hetero-interface, there is a scarcity of information on band off-sets [273,355].

8. Examples of applications utilising wafer bonding

Through the appropriate choice of bonding procedure and conditions, wafer direct bonding permits adjusting the adhesion between two solids from weak, reversible, bonding based on van der Waals forces up to irreversible joints as strong as the cohesion of the materials involved. This flexibility recommends wafer direct bonding for a great many of applications. Amongst the numerous hitherto suggested applications, four areas so far have been technologically and commercially most important: Silicon-on-insulator, power electronics, high-brightness light emitting diodes (LEDs) and micromechanical devices. While the silicon-on-insulator technology was a most influential stimulus in the development of silicon wafer direct bonding, in the development of III–V compound semiconductor wafer direct bonding it arguably were high-brightness LEDs. In addition to those mainstream applications, some selected further examples illustrate the diversity of problems for which a solution involving wafer direct bonding had been thought useful. A whole number of further examples has been detailed in the book by Tong and Gösele [22].

8.1. Silicon-on-insulator

The idea of electrically insulating the thin layer at the wafer surface carrying the devices from the bulk wafer used as mechanical support has been pursued for more than three decades. Fabricating devices in such a thin device layer offers a variety of advantages which result from the reduction or elimination of unwanted interactions between the devices and the bulk substrate. Reduced parasitic source and drain capacitances, absence of latch-up, improved transconductance, ease of making shallow junctions are some of the benefits associated with SOI technology [358]. SOI-based devices consequently can operate at lower voltages. The associated low power consumption recommends SOI technology in the area of consumer electronics especially for mobile wireless applications and other hand-held devices.

The device layer may be placed either directly onto an insulating substrate, or in a sandwich structure a thin insulator layer may separate the silicon device layer from the silicon bulk. For the realisation of a silicon-on-insulator (SOI) substrate, many methods have been tried, for example hetero- or homo-epitaxy, recrystallization with laser or electron irradiation or through zone melting.

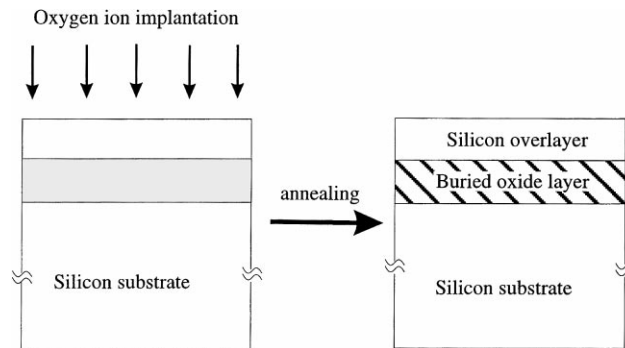


Fig. 52. Principle of SIMOX technique for silicon-on-insulator production.

A description of the various techniques can be found for instance in Ref. [358]. Of the many contenders, separation-by-implantation-of-oxygen (SIMOX) and wafer direct bonding techniques currently are the front-runners, with silicon-on-sapphire, a variant of the hetero-epitaxial technique, having established itself in the niche of radiation-hard devices. In the SIMOX process a large dose of oxygen ions is implanted into a silicon wafer which during the post-implantation annealing react with the host to form the buried silicon dioxide layer, as schematically shown in Fig. 52. Alternatively, wafer direct bonding of oxidised silicon wafers can create the buried oxide layer of the SOI substrate. One of the wafers then is thinned down to the desired thickness of the device layer; the other wafer, the ‘handle wafer’ [45] serves as mechanical support. The required thickness of the device layer usually may take any value between 50 nm and 100 μm , depending on the specific SOI application in mind. The SOI fabrication techniques utilising wafer bonding mainly differ in their choice of thinning technique. One can distinguish between the bond-and-etch-back approaches and the layer splitting techniques. The bond-and-etch-back methods can be divided into those using no etch stop and those which do; the latter one may be subdivided according to the etch-stop chosen. The future device layer on the sacrificial layer can be regarded as an example of an arbitrary layer which is to be transferred from one substrate to another. In that sense, the fabrication of SOI wafers through bonding is just an example for the use of wafer direct bonding for free material integration through layer transfer.

The bond-and-etch-back methods in their simplest form start with one wafer carefully oxidised so as to minimise defects at the interface between silicon and silicon dioxide and another hydrophilic silicon wafer. After bonding, the pair is annealed to form covalent bonds. Then the originally oxidised wafer is mechanically thinned. Accurate thickness mapping combined with numerically controlled local plasma-assisted chemical etching (PACE) [359] may allow to thin the device layer down to less than 100 nm with a thickness variation of less than 10 nm, depending on the waviness of the initial wafer [360]. To alleviate the difficulties in attaining thin device layers with good thickness uniformity, various etch-stops have been suggested [12,106,361–365]. The future device layer is separated by an etch-stop layer from the remainder of the wafer. After bonding, during the thinning process, the etch-stop protects the device layer until the sacrificial wafer has been removed. The removal of the etch-stop then leaves a uniform device layer. The etch-stop, for instance, can be a p^+ or a carbon-rich layer. To compensate the limited selectivity of the etch-stops, frequently two etch-stop layers have been used. The epitaxial layer transfer (ELTRAN[®]) exploits the high etch-selectivity between porous and non-porous silicon. A thick layer of porous silicon is the only etch stop needed for the device layer which had been epitaxially grown onto the porous silicon through chemical vapour deposition [366–369].

The layer-splitting approaches are inspired by an elegant idea of Bruel who ‘married’ implantation with wafer direct bonding [370,371]. This wafer-scale ultra-microtomy usually is referred to as exfoliation or ‘smart cut’. However, strictly speaking Smart Cut[®] refers to a proprietary process sequence, and alternative suggestions as to how to realise the layer splitting have been demonstrated successfully. The general principle of Bruel’s idea is deceptively simple: Excessive irradiation with ions can make a material blister at its free surface, a phenomenon well known from the study of nuclear reactor materials. By stiffening the surface through bonding a second wafer to the implanted surface, the radiation damage does not result in blistering but in layer splitting, as Bruel et al. demonstrated [370–372]. For the silicon-on-insulator production, hydrogen is implanted through the future buried oxide layer into the silicon wafer, typically at a dose of $2 \times 10^{16} - 1 \times 10^{17} \text{ cm}^{-2}$ protons [370]. The thickness of the device layer can be defined through the appropriate implantation energy (about 8 nm keV^{-1} in silicon) [370]. Annealing after wafer bonding causes the implanted silicon wafer to split in the damage layer where precipitation of implanted hydrogen builds up pressure in the implantation-induced microvoids. After a second annealing step and a final ‘touch polishing’ which removes only some tens of nanometres of the device layer, the surface and crystal quality of the SOI wafer’s device layer is comparable with commercial bulk wafers (Fig. 53) [372]. Besides the thickness uniformity of ca. 10 nm, the great advantage of this splitting technique is its economy, as after polishing the split wafer can be used again, either as a handle wafer or for another ion-beam sectioning. Whereas usual BESOI methods consume two silicon wafers to give one SOI substrate, the combination of wafer bonding with ion implantation in the layer splitting approach effectively produces one SOI wafer for each silicon wafer used. Perhaps with the exception of ELTRAN wafers, other BESOI approaches no longer seriously are considered for large-scale SOI production [373]. The SOI-wafers fabricated with a Smart Cut[®] technique are offered under the tradename Unibond, in all standard silicon wafer diameters up to 300 mm [372]. Again, ‘unibond’ is sometimes used to refer generally to the layer splitting techniques for fabricating SOI substrates.

So far SOI substrates mainly have found application in niche markets for radiation-hard devices, power devices, or micromechanical structures. The appeal for mainstream IC fabrication on SOI substrates comes from the possibility to reduce the power consumption, to increase the speed of the devices and of extending the usability of current process technology to next generation device performance. Recently, IBM committed itself to mass production on SOI substrates. They will use partially-depleted devices in silicon films more than $0.15 \mu\text{m}$ thick. Although IBM initially will use SIMOX wafers, this move amounts to a breakthrough for SOI technology, irrespective of the

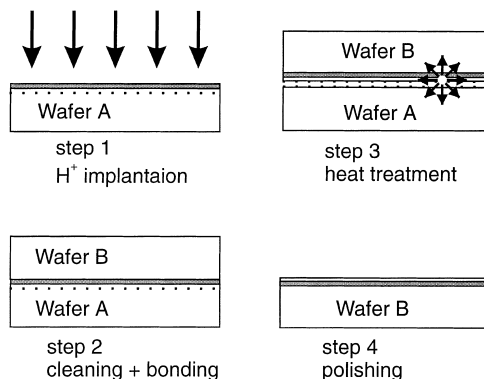


Fig. 53. Principle of smart cut technique, shown here for silicon-on-insulator production (after Ref. [370]).

technique chosen for fabricating the substrate. Much of SOI technology will depend on how IBM fares with its SOI line.

The ion-beam sectioning technique described is not restricted to silicon or to group-IV semiconductors and because of its potential for a range of other problems, it will be discussed below separately.

Recently, SOI-substrates based on the SIMOX or on the smart cut process have been compared with respect to their electrical properties, for example in Refs. [374–376]. In addition, the self-heating effect has been compared for SIMOX and Unibond substrates [377].

In addition to the electronic applications, for example for high-voltage or power devices through dielectric isolation advantages, or for integrated circuits or memory chips, silicon-on-insulator wafers also are a commercially available convenient material for silicon surface micromachining. In silicon surface micromachining, structures are formed from thin layers deposited or grown on the silicon substrate. The buried oxide (BOX) layer functions as sacrificial etch-stop with high selectivity against device layer and substrate. Simultaneously, the BOX layers can serve as electrical insulation or as spacer layer. The device layer provides mechanical and electrical properties of bulk-like quality which polysilicon layers grown on oxidised silicon cannot offer, and the handle wafer acts as mechanical support. Device and BOX layer thicknesses can be chosen as the design requires. An additional advantage of SOI substrates as starting material for silicon surface micromachining is the compatibility with microelectronic technology permitting the integration of the mechanical device into a microelectromechanical system.

Using BESOI substrates, an ultrasharp stylus of high aspect-ratio has been fabricated for scanning Maxwell-Stress Microscopy [378]. In addition, in-plane cantilevers with the thickness defined by the initial device layer thickness of the SOI substrate and tip radii of 4 nm have been reported for investigation of high-density data storage based on the phonograph concept [379].

8.2. *Bonding in micromechanics*

Bonding not only can provide the SOI substrates for silicon surface micromachining. It has established itself quickly as an integral step in the surface or bulk micromechanical fabrication of sensors and actuators. Direct bonding not only obviates glues or other adhesive interlayers which may not be compatible with the application, but also the electric fields necessary for field-assisted bonding, a technique also used in micromechanics [15,380].

The aerospace and automotive industries, for instance, use micromachining in the manufacturing of accelerometers and pressure sensors. A commercial high-precision acceleration sensor fabricated through the direct bonding of five bulk-micromachined silicon wafers may illustrate a typical application of silicon direct bonding in the sensor production. Fig. 54 schematically explains the principle of the differential capacitor acceleration sensor [381]. The pendulum in the middle wafer serves as seismic mass. The damping characteristics of the pendulum can be adjusted with the gas pressure which is being enclosed during wafer direct bonding. Further examples of wafer direct bonding for micromechanic sensors and actuators may be found, for example in Refs. [18,22,382].

If the components to be joined via wafer direct bonding rule out high-temperature bond strengthening annealing, a number of low-temperature bonding techniques outlined above are available. When components need to be insulated from one another with a thick thermal oxide layer, it is advantageous to bond a thick oxide layer against a native oxide layer rather than bonding two oxides each with half the required thickness [165]. After surface activation procedures like treatment in hydrolysed tetramethoxysilane or in an oxygen plasma, fracture surface energies sufficient for all

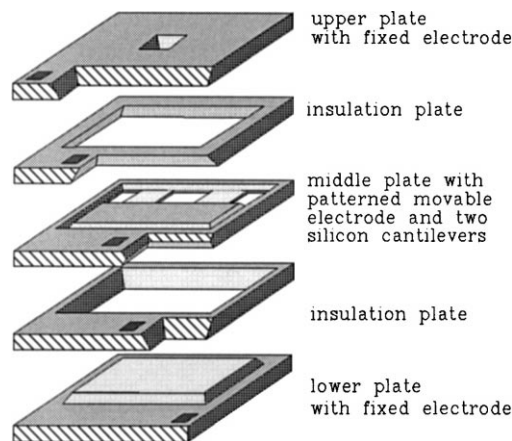


Fig. 54. Explosion diagram of a precision accelerometer made through bonding five silicon layers [381].

practical purposes have been achieved at annealing temperatures below 500°C [165]. Alternatively, the so-called ‘low vacuum bonding’ technique permits even lower temperatures. The bonding of pure silicon surfaces can be used to form covalent bonds at room temperature. Although typically performed in ultra-high vacuum, in principle an inert gas which does not re-passivate the silicon surface through adsorption could be used so that the encapsulated cavities are filled with a gas at a specific pressure [200].

Wafer direct bonding offers leak-tight sealing [39,40,120,383]. Therefore, wafer bonding often is used for the construction of pressure sensors or for the hermetic encapsulation of microelectromechanical devices. In the case of hydrophobic bonding, 600°C annealing, and 400°C for standard hydrophilic bonding resulted in air leakage rates lower than 10^{-14} mbar l s⁻¹ [120,383]. However, as outlined above, depending on the bonding technique chosen, the bonding reaction may entail gaseous reaction by-products which gather in cavities. This limits the ultimate pressure attainable. In the case of standard hydrophilic bonding, this is mainly water or, when the water has been consumed in thermal oxidation of silicon at higher annealing temperatures, that is hydrogen gas [83,84]. The gas pressure in cavities after hydrophobic bonding generally tends to be lower than for hydrophilic bonding; the gas is mainly comprised of hydrogen [83,84].

Of paramount importance for the wafer direct bonding methods to work is a sufficiently smooth and plane surface. Microchannels of 6 nm depths were sufficient to degrade the leak tightness of the bonding [383]. However, sufficient smoothness can be attained on processed surfaces through planarisation layers and polishing [62]. As anodic or frit-glass bonding can cope with larger surface roughness, sometimes these methods have been preferred [380].

8.3. High-voltage and power devices

The potential of wafer direct bonding for the fabrication of high-voltage and power electronic devices has been recognised at the inception of modern silicon direct bonding technology and soon been applied commercially. Bonding is either used as a means to fabricate silicon-on-insulator structures, as discussed above, to dielectrically insulate individual devices in high-voltage integrated circuits, or as a substitute for deep dopant diffusion or the growth of thick epitaxial layers. Direct bonding offers the advantage of reduced wafer warpage, avoidance of autodoping, low thermal budget and an increased flexibility in the design of layer thickness and doping.

The small area needed for isolation, low parasitic capacitance and absence of latch-up all recommend dielectric isolation for power electronic circuits. The problem of wafer warpage which afflicts the epitaxial passivated integrated circuit method can be overcome with the aid of wafer direct bonding [227,228]. In the laminated dielectric isolation technique a silicon wafer is bonded against a polished polysilicon layer deposited onto an oxidised silicon wafer containing V-grooves. The polysilicon covered wafer is then thinned until the silicon islands are separated from each other [228].

Wafer bonding is used in the fabrication of insulated gate bi-polar transistors (IGBTs) [384]. Nakagawa et al. reported a wafer-bonded IGBT with improved on-resistance and device breakdown voltage of 1800 V [385,386]. The bonding interface generally has been found to reduce the minority carrier lifetime. Therefore the switching time and ON state voltage in IGBTs could be controlled without the usual gold diffusion or high-dose electron irradiation, just through the position of the bond interface [79]. In addition, the interface does not impede dopant diffusion [79], so that the electrically active junction can be shifted from the bond interface by annealing. Further examples of wafer direct bonding applications in power devices can be found for instance in Refs. [73,75,345,387,388].

8.4. High-brightness light emitting diodes

In the spectral range from yellow to red, AlGaInP light emitting diodes (LEDs) reportedly exhibit the highest luminous efficiency of all current solid-state light emitters [266,267,269,270,389]. The high performance has been achieved through a combination of epitaxial growth techniques and wafer direct bonding. This decoupled the requirements which crystal growth and optical design place on the substrate so that the optimum material for hetero-epitaxy could be chosen and later be changed for a material more suitable for achieving high efficiency during device operation.

For the reportedly most efficient LEDs, hetero-epitaxial structures are grown which sandwich the direct-bandgap active layer between two confining layers of larger bandgap [267,270]. The active layer material determines the emitted light wavelength. As dislocations accommodating the misfit most often degrade the device performance, hetero-epitaxy requires suitably lattice-matched substrates. For the quaternary system AlGaInP, GaAs recommends itself as the growth template [390], as seen from Fig. 55. At Hewlett-Packard a process was pioneered where a sandwich with $(\text{Al}_x\text{Ga}_{1-x})_{0.5}\text{In}_{0.5}\text{P}$ ($x \geq 0.7$) as confining layers and an $(\text{Al}_x\text{Ga}_{1-x})_{0.5}\text{In}_{0.5}\text{P}$ ($0 \leq x \leq 0.55$) has been grown on GaAs [391]. Then a GaP layer of tens of micrometres thickness is deposited via hydride transport vapour phase epitaxy. This layer functions as current-spreading contact, as window, and as mechanical stabiliser when the substrates are exchanged.

The efficiency of any LED is the product of its internal efficiency and the efficiency with which light can be extracted from the device. Fig. 56 illustrates the light extraction for various LED geometries. The cones schematically indicate that total internal reflexion at the solid-air interface limits the emission of light from the device. Through more interfaces more light can be extracted. A transparent substrate significantly could enhance the LED efficiency. Growing directly onto a transparent substrate would be the most direct approach. However, no suitable transparent substrate is available which simultaneously satisfactorily functions as template for hetero-epitaxial growth of the diode structure. In this situation, wafer direct bonding gives the freedom to fulfil the requirements sequentially, as they occur in the manufacturing process [356]. The absorbing GaAs substrate is chemically etched away, freeing the AlGaInP LED structure. The ca. 45 μm thick top layer provides the necessary mechanical rigidity for wafer handling. Due to the strain in the LED-

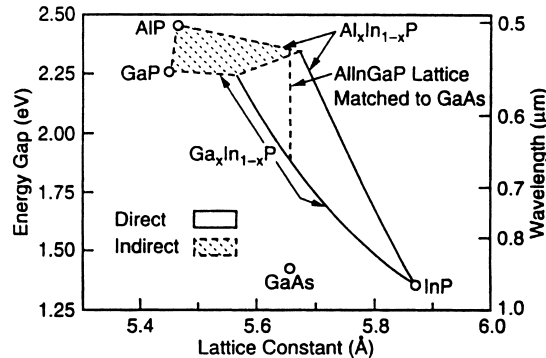


Fig. 55. The energy gap of the quaternary group III–V system AlGaInP as a function of lattice constant. Although the transparency in the relevant spectral range would make GaP a suitable substrate, the growth of high-performance LEDs in this system requires GaAs substrates (after Ref. [390]).

cum-top-window stack, the self-supporting structure is significantly bowed. Uniaxial force brings the device structure and new substrate in contact. With the aid of III–V compound semiconductor wafer bonding techniques described above, the absorbing GaAs growth template is substituted by an GaP substrate which is transparent in the spectral range of the AlGaInP LEDs. The wafer bonding step does not degrade the electrical or the optical performance of the LEDs. On the contrary, the substrate substitution via wafer bonding is said to improve the device performance two-fold [268,270]. The currently brightest LEDs in the red–yellow spectrum are attained this way, meeting the luminosity per power performance of unfiltered incandescent lamps [270,392]. The LEDs reportedly provide traffic lights with better visibility under all illumination conditions at a 38% saving in energy, and may be applied in the automotive industry [392]. Additionally, a lifetime in excess of 120 000 h has been predicted after accelerated life time testing [270].

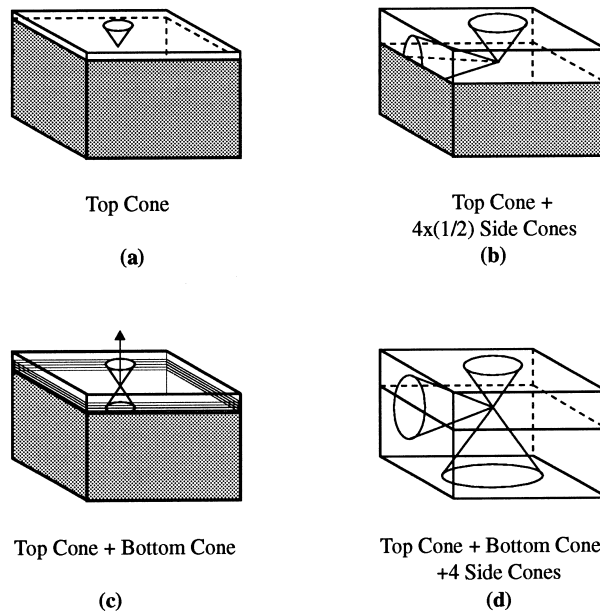


Fig. 56. Light extraction cones for various LED structures (after Ref. [270]). (a) Thin window layer (the absorbing substrate in grey), (b) 'thick' window layer, (c) distributed Bragg's reflectors below active layer, and (d) transparent substrate.

8.4.1. Other opto-electronic applications

Other applications of wafer direct bonding in opto-electronics are, for example, vertical cavity surface emitting lasers [19,393–395]. With the aid of a wafer bonding step, the epitaxial substrate for the light emitting device and for the Bragg reflectors can be chosen independently, again allowing to optimise the device performance free of lattice-match-constraints [19,251]. Bonding has also been proposed as means to combine components grown on different substrates.

Perhaps of a more exploratory nature are applications of bonding for non-linear optics or the realisation of photonic bandgap materials. Quasi-phase-matching (QPM) structures for second-harmonic generation may be generated when (110) GaAs plates which each are one coherence length thick are stacked in a way that they are alternately rotated about their $(1\bar{1}0)$ direction [256–258,396]. Direct bonding at elevated temperature was used to produce a bonded stack of GaAs plates for non-linear optics applications [256,257]. Although inadequate bonding procedures initially lead to unacceptable optical losses and hence to poor device performance, after recent process improvements [259] optical losses as low as 0.1–0.3% per interface for a stack consisting of 50 layers of (100) GaAs and 40 layers of (110) GaAs wafers have been claimed [258].

A three-dimensional photonic crystal for the optical wavelength region has been constructed through GaAs direct bonding [397,398]. This was realised by growing an AlGaAs layer followed by a GaAs layer on a GaAs substrate. A two-dimensional structure was then formed on the top GaAs layer by applying electron beam lithography and reactive ion etching. A pair of etched structures was then stacked and bonded to each other by heating the assembly in an H_2 atmosphere. One side of the substrates including the AlGaAs etch stop layer was removed and the bonding step was repeated. A structure exhibiting a band-gap in the 10 μm wavelength range was obtained [397]. A method has been proposed to align the individual crystal components adequately [398].

8.5. Smart cut techniques

The principle of the layer splitting techniques has been described above in the section on SOI substrate fabrication: stiffening of surface layer after implantation, formation of microcracks, build-up of gas pressure in microvoids, ripening of voids to critical void size, avalanche-like coalescence of voids and splitting off of stiffened surface layer. For the method to work, clearly a number of conditions must be met.

- A dose higher than the minimum dose must be implanted in order to induce layer splitting [399].
- The implantation dose must be low enough not to degrade the layer to be transferred.
- After implantation, the void size must be subcritical so as to prevent surface blisters which would be detrimental for the film quality and bondability.
- The adhesion at the bond interface must be sufficient to prevent delamination of the stiffener and formation of blisters.
- For materials with differing thermal expansion, bond strengthening or void ripening should take place below the temperature for which mismatch in thermal expansion causes delamination or fracture of one of the wafers.

Currently the physical and chemical basis of the layer splitting phenomenon are investigated, on the one hand so as to gain control over the individual process parameters, on the other hand in order to determine the range of materials which can be sectioned with this technique. Hydrogen apparently plays a pivotal role in the smart cut process in passivating the internal surfaces of platelet-like microcracks [130]. The whole process is thermally activated, with contributions from bond splitting and diffusion [372]. Boron, and to a lesser degree also aluminium, can lower the temperature

necessary for splitting [243,400]. The synergistic effect is particularly pronounced when boron was implanted prior to hydrogen, at the same depth, without activating it as a dopant, although it can be seen in uniformly boron-doped crystals, too. In the case of a boron pre-implantation at an off-set depth, the splitting reportedly occurred near the boron layer [401]. In addition, the boron pre-implantation lowers the requisite hydrogen dose [243,400]. A reduced critical hydrogen dose also has been found in the case of helium post-implantation [402]. A judicious allocation of the thermal budget needed for the various processes gives additional freedom when combining different materials [243,290]. One may implant at an elevated temperature just low enough that for the time span needed the microcracks do not become supercritical. The bonding, bond strengthening and splitting may be performed at lower temperatures [290]. High-speed implantations like plasma immersion implantation further widen the time-temperature window of the ultra-microtomy process [403].

Although initially the chemical interaction between hydrogen and silicon was taken to imply a restriction of the smart cut techniques to silicon, it soon was demonstrated that other group IV crystals like diamond or germanium form the microcracks [404]; also compound materials like silicon carbide [288,290,404–406] could be sectioned with this technique. Later iso-electronic materials like GaAs [265], InP or the wide-bandgap material gallium nitride (GaN) [403] were found to split and meanwhile even very different materials like LaAlO_3 successfully have been sliced with smart cut [403]. Again, it may be of advantage to implant at high temperatures [290], but the optimum conditions apparently need to be determined for each material individually.

8.6. Surface protection by room temperature bonding

In microelectronics, the preservation of semiconductor surface cleanliness has become an important issue. Usually wafers are stored in plastic boxes during transport and storage on site. Volatile ingredients of plastics (plasticizers) are known to contaminate the wafer surface [407]. The determination of the contact angle of a drop of water on a silicon wafer taken out of a plastic box is a quick and simple method for probing the contamination with organic compounds. Contact angles greater than 10° suggest a contamination by organic components. One approach to avoid surface contamination is to protect the surfaces through room temperature wafer bonding, as first suggested by Lehmann et al. [408]. If clean wafer surfaces are bonded before transport or storage a contamination by particles or organic compounds can be prevented [131,408]. Standard room temperature bonding is reversible and thus the bonded wafers can be separated just prior to their use in device processing.

Long storage of bonded wafers at room temperature or storage at elevated temperatures (say 100°C) as they may occur during shipping may lead to an effect already described, namely an increase in fracture surface energy. This is undesirable when the wafers are to be separated again. When using hydrophobic surfaces instead of hydrophilic ones, the adhesion is generally diminished and the susceptibility to bond strengthening during shipping or storage is eliminated. One drawback of this surface protection technique is that there is up to now no elegant way to separate the wafers. The separation is usually achieved by inserting a wedge at the rim of the wafers. The concern has been raised that this may damage the wafer surfaces. It has been suggested to trap a drop of liquid in the interface between two bonded wafers for easy debonding. Water was thought to be the most suitable liquid for this purpose since it is available in high-purity and fully compatible with VLSI technology. A water droplet was put on the surface of a hydrophobic silicon wafer followed by bonding to a second hydrophobic wafer. Upon heating beyond the boiling point of water the wafers could be separated [409–411].

Provided a simple procedure can be established with which large diameter wafer pairs can be debonded without running the risk of perhaps damaging the wafer surface, there is little doubt that surface protection via room temperature wafer bonding will become an important step in semiconductor processing. Until such time, the technique will be restricted to research usage. In the authors' laboratory, the method is successfully employed for wafer transfer between different rooms. The method also can be advantageously employed in the sample preparation for UHV-bonding [202,207]. In addition, an ultra-high vacuum application of the method has been suggested whereby in vacuo hydrogenated silicon surfaces are bonded to preserve atomically clean silicon surfaces [412]. Also the analysis of surface impurities reportedly may benefit from protective bonding as an alternative to encapsulating the surface to be investigated with the deposition of an amorphous or an polycrystalline silicon film [158].

8.7. Miscellaneous applications

8.7.1. Strong albeit reversible bonding

In conventional wafer direct bonding, usually the reversibility of the initial bonding is sacrificed for higher mechanical stability. In spite of covalent or metallic adhesion, in a number of cases it may be possible to regain the reversibility of conventional bonding if the joints have been formed through room temperature covalent bonding. This interesting concept has been proposed by Suga [413], mainly with a view to waste management and recycling (Fig. 57). For instance, thermomechanical stresses between dissimilar materials may be used to separate different materials during a heating cycle aimed at splitting the joint. In addition, with the aid of UHV-bonding materials can be joined which could be welded only with difficulty. So, for instance, aluminium and stainless steel have been bonded [209]; annealing at the alloying temperature then induced the formation of a brittle intermetallic interphase and the joint was de-bonded [414]. In another example, Hosoda proposed loading the joint with hydrogen to cause embrittlement and eventually de-bonding [415].

8.7.2. Spin valves

Another prospective area for direct bonding is magneto-electronics. A metallic spin-valve multilayer as base has been coupled to a monocrystalline silicon emitter to yield a spin-valve

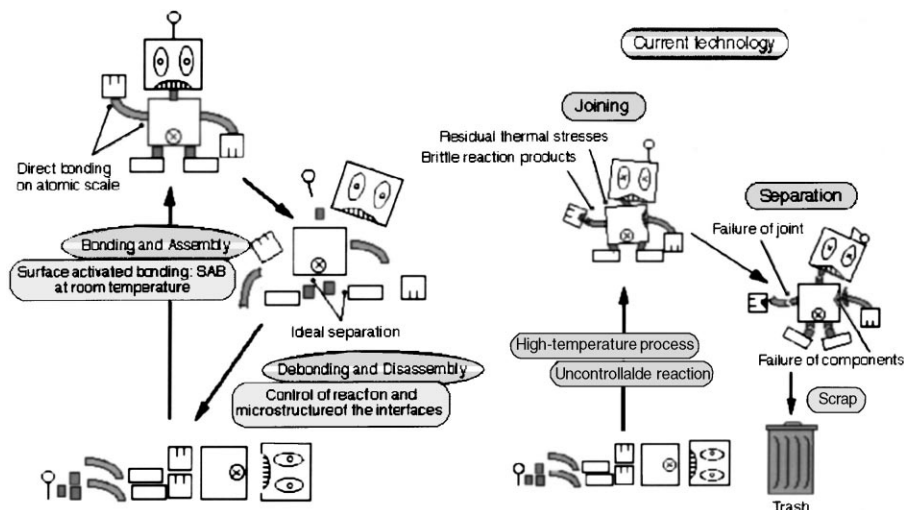


Fig. 57. Schematic explanation of the reversible interconnection concept [413] (diagram courtesy Prof. T. Suga, University of Tokyo).

transistor. Originally, a hydrophobic silicon emitter was bonded to the top cobalt layer of the spin-valve structure [416]. Bonding was chosen to obtain crystalline silicon on the metal layers, at room temperature. The fracture surface energy consequently was weak, preventing subsequent lithographic processing; moreover, the current gain of the spin-valve transistor amounted only to 5% at room temperature because of insufficient electron injection at the weakly bonded emitter Schottky barrier [417]. Strong chemical bonds can be formed at room temperature through ‘UHV-bonding’, as discussed above, and after refining the experimental method by incorporating an ‘UHV-bonding’ step, thin metal layers deposited on both silicon components formed spontaneously metallic bonds upon room temperature contact for microroughnesses smaller than ca. 2 nm [206]. Employing the method for the bonding of thin platinum layers deposited onto silicon, surface energies of 4.1 J m^{-2} were estimated based on an in situ blade test [113].

8.7.3. Compliant substrates

Previous examples in the context of hetero-epitaxy showed wafer direct bonding as a substitute for or complement to hetero-epitaxial film growth: two materials which in view of their structural differences were not suited for hetero-epitaxy were joined through wafer direct bonding. Thus dislocations threading through the film had been avoided. As seen above, this combination of two materials across an artificial (bonded) grain boundary with the ensuing loss of epitaxial relationship can be a perfectly viable solution. Nevertheless, as hetero-epitaxy frequently is the only means of generating large-area monocrystalline films, lack of a substrate with suitable lattice properties may limit the film quality which can be obtained. A compliant substrate would remedy at least the threading dislocation problems caused by the mismatch in lattice constants. Before the epitaxial film needs to relieve strain in misfit dislocation generation, a thin substrate of a lattice suitable to act as growth template but not necessarily matching lattice constant would elastically adjust to the lattice constant of the new material under the elastic influence of a growing film. Notwithstanding the experimental validity of the concept [418], a free-standing substrate below its critical thickness [419,420] is only nanometre thick and hence impractical to work with. A thin film mechanically supported by a handle wafer without restricting it to contract or expand laterally appeared as the ideal compliant substrate. A variety of methods have been tried to attach a thin film to a substrate without restraining it too much. An SOI wafer with an ultra-thin superficial silicon layer served as a first approximate implementation. Relaxation seen in X-ray diffraction data after annealing the grown $\text{Si}_{0.85}\text{Ge}_{0.15}$ layer was attributed to slippage at the interface between the buried oxide and superficial silicon layer. Subsequently, compliance of an SOI substrate has been reported for a number of other systems.

To put the idea of a thin film gliding on a mechanical support into practice, thin films bonded onto a low-viscosity glass have been investigated by Kuech et al., as mentioned in Ref. [421]. In spite of the persuasiveness of the concept, the relaxation times to be anticipated for wafer-scale substrates may be prohibitively long [422].

Whereas the previous examples used bonding perhaps as a means to transfer the thin layer onto its mechanical support, the ‘compliant universal’ substrate relies on bonding to generate a twist boundary, as shown in Fig. 58 [423–426]. A thin (3–10 nm thick) GaAs layer grown onto a AlGaAs etch stop on (100) GaAs was bonded under pressure, at ca. 550°C , in a hydrogen atmosphere onto another GaAs crystal, twisted around the common surface normal. Hetero-epitaxial $\text{In}_{0.35}\text{Ga}_{0.65}\text{P}$ [423,424] or InSb [424] films grown on those substrates reportedly were free of dislocations, in spite of their thickness exceeding the critical thickness by more than one order of magnitude. The compliance was reported for lattice mismatch between -1% ($\text{In}_{0.35}\text{Ga}_{0.65}\text{P}$) and $+15\%$ (InSb).

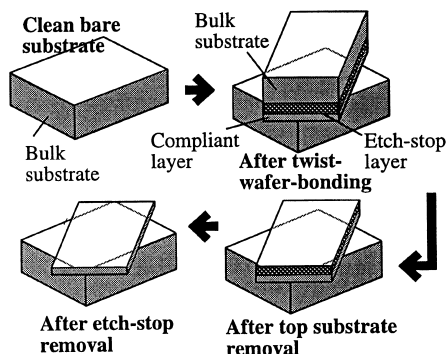


Fig. 58. Process flow for twist-bonded compliant universal substrate fabrication [424].

It has been argued that twist angles of 10° – 30° with the concomitant merging of dislocation cores at the interfacial screw dislocation network dramatically decrease the adhesion in the interface, and thus essentially free the thin film to shrink or expand in accordance with the requirements of a growing film [427]. This proposition, however, may not be tenable. Tan and Gösele speculated about alternative explanations for the reported compliance of the twist bonded substrate [428]. Instead of the global elastic deformation of a truly compliant substrate they introduced the idea that a local mechanism of strain relief might be the basis for the apparent compliant substrate effect. They hypothesised that the screw dislocations on one hand foster the correlated generation of misfit dislocations, so that few dislocation segments were left threading through the hetero-epitaxial film; on the other hand, they effectively getter contaminants thus suppressing the growth of stacking faults [428]. Kästner et al. put the concept of local plasticity underlying the apparent compliance on a firmer basis by working out a dislocation reaction model of dislocation splitting and slip motion [429]. Because of the dearth of substantive information on the crystallographic structure of the hetero-epitaxial film-compliant substrate system, the implications of this mechanism presently cannot be compared to experimental evidence so that the proposal for the time being remains a bold conjecture.

In the meantime, Lo reported a twist-bonded silicon–silicon substrate [430]. He found small twist angles to work as well [431]. The explanation offered [431] did not assume a global elastic deformation of the thin substrate layer but supposed a model for the alleged compliance effect in spirit not dissimilar to the proposal of Ref. [428].

When fabricating a twist-bonded compliant substrate, obviously the integrity of its nanometre-thick top layer needs to be maintained. After growing a pseudomorphic film on a twist bonded substrate whose superficial GaAs film was damaged and thus contained pinholes, recently a hetero-epitaxial film has been observed with dislocation-free lattice-relaxed areas. In this case, however, the reason for the relaxation could not be attributed to compliance, as during growth misfit dislocation segments could glide to the edges of those ‘grains’ [432].

9. Summary and conclusions

In the paradigmatic case of silicon direct bonding, the tailoring of the adhesion has been demonstrated. Through suitable surface preparation, the spontaneous adhesion between two silicon pieces can be varied from weak bonds based on van der Waals forces in hydrophobic bonding (surface energy ca. 50 mJ m^{-2}) over weak chemical bonds in the case of hydrophilic bonding

(surface energy ca. 150 mJ m^{-2}), or surface modification via specially designed monolayers (surface energy ca. 0.45 J m^{-2}) up to covalent bonds in the case of UHV-bonding (surface energy ca. 2 J m^{-2}). In addition, the adhesion can be varied through the choice of bonding conditions, as illustrated by the hydrophilic bonding of silicon. Whereas originally temperatures of 1100°C were felt necessary to convert the hydrogen bonds to covalent bonds, nowadays 200°C may be more than sufficient to accomplish the strengthening. Without the steric constraints of the bond interface, the silanol groups are known to condense already at, or near, room temperature. The reaction may only proceed as long as the accumulation of reaction by-products, in this case water, does not shift the equilibrium towards hydrolysis. In addition, entrapped gases locally preventing intimate contact may be consumed only at high temperatures. With appropriate alteration of the bonding conditions aimed at removing the hindrances imposed by the steric confinement, the adhesion obtained at a given temperature can be adjusted between weak chemical bonds up to covalent bonds, as demonstrated in the case of hydrophilic silicon surfaces.

Much of the progress in wafer direct bonding has been achieved based on a purely heuristic approach, often without a detailed investigation or understanding of the underlying interface chemistry. With some of the methods developed for investigating the interfacial chemistry in the case of silicon bonding, the bonding procedures for other material systems may be put on a firmer basis. Direct bonding technology may benefit from a closer incorporation of chemists who may study chemical reactions under unusual constrained conditions.

Silicon-on-insulator wafers fabricated with a bonding step are now available in all current silicon wafer sizes, with device layers apparently in bulk-like quality. With IBM embarking on SOI technology for mainstream IC fabrication, direct bonding may see a boost, too.

The layer splitting techniques are not restricted to the fabrication of silicon-on-insulator substrates for which they originally had been developed. As it emerges that an ever wider variety of materials may be split with this novel microtomy technique, it opens up new possibilities for material combination. In addition, as it is not subjected to the size constraints imposed on the etching step of the standard epitaxial lift-off technique, the layer splitting techniques may aid realising the integration potential of the ELO concept.

Direct bonding technology may best be viewed as supplying a tool box. The applications presented clearly do not define the area of applicability, and with the aid of those tools a great many of hitherto unforeseen areas may benefit from the freedom gained in materials combination or integration.

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