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Reduction of the PtGe/Ge Electron Schottky-Barrier Height by Rapid Thermal Diffusion of Phosphorous Dopants

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The electron Schottky-barrier height (SBH) of platinum germanide diodes on germanium (PtGe/Ge) is tuned by means of incorporation of phosphorous dopants from a spin-on-dopant resist. Thereby a highly doped surface layer on Ge substrates is formed in a rapid thermal diffusion process before the formation of PtGe. Applying a diffusion process of the P atoms at temperatures above 580°C, an ohmic contact behavior is found for the originally Schottky-type barrier diodes and evidence is given for a lowered electron SBH. The contacts exhibit barrier heights to electrons as low as $\Phi_{B,e} = 0.16$ eV. In contrast, increased barrier heights for holes of $\Phi_{B,h} = 0.45$ eV are found. The results of the electrical characterization are further supported by time of flight secondary-ion mass spectrometry measurements where a pileup of P dopants at the PtGe to Ge interface region is observed. In summary, a damage-free process scheme for the reduction in the electron SBHs in PtGe/Ge diodes is given. The presented approach can pave the way to ohmic-type n-contacts to germanium and is applicable to planar as well as three-dimensional device structures.
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A focus of recent complementary metal oxide semiconductor (CMOS) research is set on germanium (Ge), which is a candidate to replace Si as the channel material due to the increased hole and electron mobilities, and, in terms of processing, lower dopant activation temperatures.[1,2] Nevertheless, several challenges remain; one is the realization of ohmic drain and source contacts. The main issues are the low solid solubility of dopants in Ge, enhanced diffusivities of n-type dopants, and incomplete activation after the implantation of dopants.[3] The motivation for the research in Schottky barriers (SBs) with low barrier heights is their possible integration into the source and drain contacts of metal oxide field effect transistors. By this, the problem of high parasitic resistance of the source and drain regions, which corrupts the higher drive currents obtained on Ge substrates for small gate lengths, can be overcome. For this reason low Schottky-barrier heights (SBHs) for both electrons and holes are needed for a complete CMOS integration scheme.[4] Dimoulas and co-workers showed that, in general, low SBHs for holes exist, considering metal/Ge SB contacts, due to the Fermi-level pinning around the charge neutrality level near the valence band.[5] However, SBHs for electrons are reported to be high.[5] Inserting a thin interfacial layer of, e.g., Al_2O_3,[6] Ge_3N_4,[7] or SiN [8] between the metal and Ge is a promising method to reduce the electron barrier height. Nevertheless, using this approach, problems concerning high contact resistances due to the interfacial layer remain.[4] Besides that, the formation of germanides, which show a lowered SBH for electrons and offer a lower sheet resistance,[5] is a promising pathway to reduce the electron SBH. Introducing a layer of the highest dopant concentration (n + layer) in between the germanide and the Ge substrate results in a strongly decreased width of the SB, and therefore in an increased contribution of the tunneling current.[4] Furthermore, the advantage of this approach is to maintain the self-aligned formation of the source and drain regions.

Mueller et al. showed that SBHs in Ge can be significantly lowered by the dopant segregation mechanism induced by the germanidation process, where the n + dopant layer is consumed during the germanidation, and the dopants are accumulated at the germanide/Ge interface.[9,10] This pileup of dopants is most likely related to the snowplow effect caused by the germanidation, and was first investigated on Si substrates.[11] The formation of the highly doped n + interfacial layer relies on the incorporation of dopants by their implantation into a thin surface layer of Ge before the germanidation of the metal/Ge contact. A low barrier height for electrons of 0.34 eV is reported for implanting P, and 0.19 eV for implanting As before the formation of NiGe contacts, as well as 0.05 eV for As- and 0.07 eV for P-implanted PtGe contacts.[9,10]

Papers so far focus on the incorporation of the dopant species by implantation, where problems with implantation damage and channeling remain an issue. Furthermore, shadowing problems and doping of high aspect ratio structures are challenging. However, sharp box-shaped dopant profiles can also be obtained by the diffusion of dopants from a solid-state diffusion source. By this approach, junction depths below 20 nm on Si substrates are reported by Usami and co-workers.[12] Posthuma and co-workers investigated the diffusion of P atoms for the formation of shallow emitter structures on Ge substrates for photovoltaic devices.[13] Although rather long diffusion times between 4 and 10 min are used in their work, box-shaped doping profiles are achieved. This is probably due to the effect of an enhanced diffusion in the presence of high dopant concentrations, where the diffusion coefficient in regions of higher dopant concentrations is enhanced. Thus, sharp diffusion profiles can be achieved if the respective diffusion source has a high concentration of dopants. The question arises whether SBHs can be effectively tuned by a rapid thermal diffusion (RTD) process for the formation of the n + interfacial layer.

Several dopant sources for solid-state diffusion doping (SSD) exist. Chui and Saraswat investigated the properties of heavily doped phosphosilicate glass deposited by low pressure chemical vapor deposition at 400°C for the formation of shallow source/drain junctions on Ge.[14] However, using this SSD source no considerable out-diffusion was obtained at process temperatures below 800°C. Another possible dopant source is a highly doped spin-on-glass (SOG) resist, also referred to as spin-on-dopant (SOD) resist, which offers integration advantage due to the ease of handling of the resists. These resists are available in a variety of dopant concentration levels and species, and owing to their resist nature, they can be applied even to three-dimensional device structures.

In this work we investigate the applicability of the approach of supplying dopants by SSD to form an n + doped Ge surface from an SOD resist. The studies are performed on planar substrates, but the results can also be applied to other device structures, such as nanowire-device architectures[15] or fin field effect transistor devices[16] scaled down to structure sizes up to 20 nm. We start with

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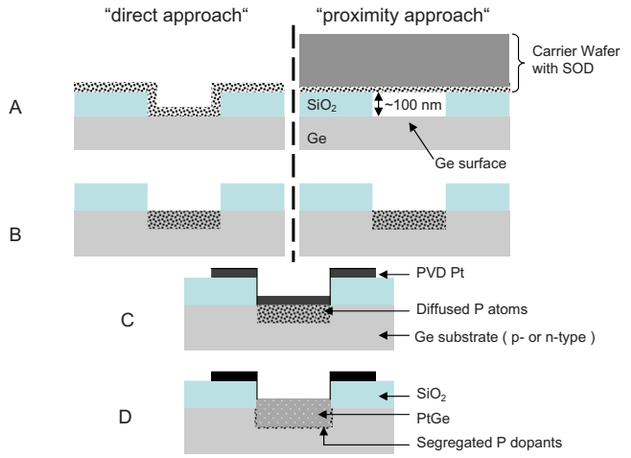

Figure 1. (Color online) Process flow for the formation of the SB diodes. (A) SOD resist is deposited on patterned Ge/SiO_2 wafers (direct contact, left) or onto a Si carrier wafer (proximity contact, right) which is placed onto the Ge/SiO_2 mask structure. (B) The diffusion process is applied and the resist is stripped off. Carrier wafer is taken away and the substrate is cleaned. (C) Pt is deposited by physical vapor deposition and structured using a lift-off process. (D) A germanidation process is applied to form PtGe.

the identification of a temperature process window, and give suitable parameters for an RTD process. Two methods of supplying the dopants from the SOD resist layer are then compared to each other. In the first approach, further referred to as the "direct contact" approach, the SOD layer is brought in direct contact with the Ge substrate. In the second approach, further referred to as the "proximity contact" approach, the SOD layer is first deposited on a carrier wafer, which is subsequently placed about 100 nm above the Ge surface during the diffusion process.[17] Concerning the proximity contact approach, where the SOD layer is not in direct contact with the Ge substrate, but is placed in the proximity of the substrate, the resulting diffusion process is exerted out of the gas phase, as described by Zagozdzon-Wosik and co-workers.[17] The conclusions of the electrical characterization by current–voltage (*I-V*) measurements are related to the results of time of flight secondary-ion mass spectrometry (TOF-SIMS) measurements.

Experimental

Antimony (Sb)-doped wafers with a resistivity of 6–10 Ω cm were used as n-type Ge substrates. For p-type Ge substrates, gallium (Ga)-doped substrates with a resistivity of 4–14 Ω cm were applied. An ~100 nm thick hard mask layer of SiO_2, deposited by plasma enhanced chemical vapor deposition, was used to align the diffusion process. Therewith, only the uncovered parts of the Ge substrates, either p- or n-type, were exposed to the SSD source. As the diffusion source, the SOD resist P-8545 from Allied Signals containing P dopants was applied. For the formation of the SB diodes on n- and p-type substrates, an RTD process was performed.

For the direct contact approach, the SOD resist layer was deposited on the Ge/SiO_2 structure, after the thin GeO_2 layer was removed by diluted HF (2%), schematically shown in Fig. 1A (left). The SOD resist was spin-deposited using a speed of 3000 rpm for 30 s, resulting in homogeneous films with a thickness of ~100 nm. For the proximity contact approach, the SOD layer was deposited onto a carrier substrate. After both types of deposition of the SOD layer, an annealing process was applied at 200°C for 30 min to evaporate all solvents. The temperature was ramped up from room temperature to 200°C with a ramp rate of 15 K/min to avoid the formation of cracks in the SOD layer. The final concentration of phosphorous dopants in the annealed SOD layers was in the range of 5×10^{21}–10×10^{21} ions/cm^3,[18] much higher than the equilibrium solid solubility of P in Ge, which amounts to 2×10^{20} ions/cm^3.[19]

For the direct contact approach, the RTD was performed at temperatures ranging from 500 to 650°C with a duration of 5 or 60 s. Before the Pt metal electrode was deposited for the formation of the SBs, the SOD layer was removed by cyclic dipping in buffered hydrofluoric acid (BHF) and deionized water, leaving the Ge substrate and the SiO_2 mask layer. For the proximity approach, the Si/SiO_2 carrier substrate with the SOD layer on top was placed directly onto the Ge/SiO_2 mask structure, also depicted in Fig. 1A (right). The SiO_2 mask serves as a spacer and was designed to yield a gap of approximately 100 nm to the Ge substrate, taking into account the loss of SiO_2 during the substrate cleaning. The RTD was applied at temperatures ranging from 600 to 700°C with a duration of 60 s. After the carrier wafer was removed, the Ge/SiO_2 substrate was cleaned by cyclic dipping in BHF and deionized water.

Finally, the SB diodes were fabricated from a 60 nm Pt film, sputter-deposited on the SiO_2/n-type Ge directly after the cleaning procedure. The adjacent germanidation was performed at 400°C in forming gas atmosphere (90% N_2 and 10% H_2) for 5 min, which resulted in a platinum monogermanide (PtGe) film.[20] Figure 1 summarizes both the process flow in direct contact and of the proximity contact approach for the formation of the SB diodes. The area of the circular diode structures amounts to 0.785×10^{-4} cm^2. Back-contact layers are formed to reduce the series resistance of the diode structures by resputtering of the Ge wafer back side in argon plasma and an in situ sputter deposition of layers of titanium and gold.

TOF-SIMS measurements were performed using an Ion TOF-SIMS [5] instrument in the dual beam mode.[21] Here a Bi_1^+ primary ion beam (25 keV) was used to analyze the sample surface on a 100 × 100 μm area. Alternating with the Bi_1^+ ions, a second beam of Cs_1^+ ions was used to ablate the surface on a 300 × 300 μm field of view. The sputter rate of Ge as well as the sputter rate of the formed PtGe film was determined by the measurement of the depth of the eroded sample area. TOF-SIMS profiles were obtained on n-type substrates using the direct contact doping approach described above. Identical diffusion processes as for the formation of the SB diodes were applied, but without the deposition of a SiO_2 mask structure. The results of these chemical analyses were compared to the electrical performance of the respective diode structures.

SBHs were extracted from temperature-dependent *I-V* characteristics in the temperature range from 80 to 385 K. A typical extraction of the barrier height can be obtained from the slope of an Arrhenius plot of the reverse current density. The extracted barrier heights were plotted as a function of the applied diode voltage. The SBH was extracted at zero bias $\Phi_{B0,e}$ from the intercept of the fitting curve to the linear region of $\Phi_{B,e}$ at 0 V.[22] The reverse current density is well described by the model of thermionic emission current, e.g., for electrons as

$$I = AA^*T^2 \exp[-\Phi_{B,e}/(k_B T)]\{\exp[q(V - IR_s)/(nk_B T)] - 1\} + (V - IR_s)/R_p \quad [1]$$

Here A^* is the Richardson constant for thermionic emission and A is the active contact area of the Pt–Ge contact. The series resistance R_s is mainly affected by the resistance of the low doped n-type bulk Ge, as well as the quality of the back contact, if effects from the measurement setup are not to be considered. The parallel resistance R_p that describes possible leakage currents is not addressed in the simple thermionic emission theory.

Although in general an extraction of the SBH is possible from the linear fit of Eq. 1, the temperature dependence of the saturation current should be used for the determination of the effective SBH, as the active contact area may not be clearly determined by the contact geometry alone. The *I-V* curves were measured in a temperature range from 80 to 300 K using an Agilent semiconductor parameter analyzer (4156 B). *I-V* measurements from 300 to 385 K were performed by using a microneedle prober setup in combination with a Keithley 4200 SCS measurement system.

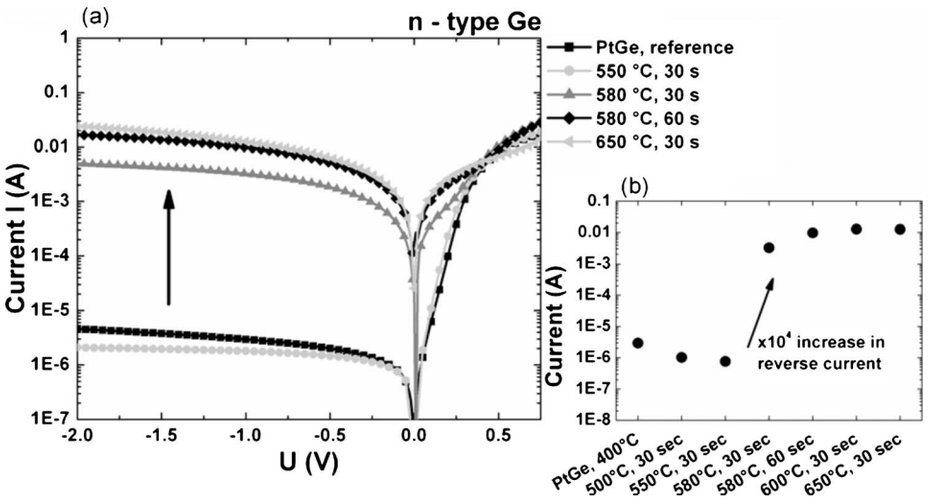

Figure 2. Comparison of room-temperature *I-V* SB characteristics, shown in (a), obtained for different annealing treatments after the deposition of the RTD and PtGe contact formation. The formation of germanide is performed at 400°C in forming gas atmosphere. In (b) the comparison of the current contribution in the saturation regime at −1 V as a function of different SOD diffusion parameters is shown. A clear increase in the reverse current density can be achieved by applying a diffusion process at temperatures of 580°C or above.

Results

Comparison of the direct contact and the proximity contact approach.— First, the impact of diffusion temperature and diffusion time, using the direct contact diffusion approach and n-type Ge, on the *I-V* curves at room temperature is compared in Fig. 2a. The results show a clear increase in the saturation current in the reverse voltage regime for the diffusion-modified SB diode structures at higher annealing temperatures, which would be expected from a lowering of the effective electron SBH. Different RTD pretreatments before the formation of the SB diodes are compared. Figure 2b summarizes the diode current in the reverse region at a voltage of −1 V. Only a small impact on the reverse *I-V* characteristics can be found at diffusion temperatures below 550°C. Raising the temperature of the diffusion process for the P atoms before the germanidation above 580°C, the contribution to the current in the reverse voltage region is increased by a factor of 10^4–10^5. As expected for an ohmic contact and a lowered electron barrier height, the *I-V* characteristics are also linear in the high temperature diffusion process.

For the proximity contact approach, a qualitatively similar increase in the reverse current of the PtGe SB diode is achievable. Figure 3a shows the obtained *I-V* characteristics measured at room temperature for different RTD pretreatments of 60 s at temperatures ranging from 600 to 700°C. As in the direct contact diffusion approach, a comparison is given for a reverse current at −1 V and can be seen in Fig. 3b. The current is increased by applying a diffusion temperature above 600°C, although the magnitude is much less pronounced for the proximity contact approach. An explanation for the smaller change in the reverse current may be the lower dopant concentration of P atoms at the Ge surface during the diffusion process, as the amount of P atoms relies on the transport of P from the gas phase to the Ge substrate, as pointed out in Ref. 17. To achieve the same increase in the reverse current, a much higher diffusion temperature has to be applied. Therefore, further studies concentrate on the direct contact diffusion approach because here, lower processing temperatures can be applied.

Applying the direct contact approach to the SB diodes fabricated on p-type Ge substrates, the reversed effect, compared to the results on n-type Ge substrates, can be found. Starting from a mere ohmic characteristic due to the low SBH of platinum and PtGe on p-type substrates, a clear formation of an SB diode characteristic is obtained, if applying different diffusion steps in a temperature range from 600 to 650°C before the formation of PtGe. Thus, an increase in the SBH for the holes is found.

Extraction of the SBH.— Analyzing mere PtGe electrodes, a barrier height of 0.67 eV to electrons can be found. Additionally, from the fit of the *I-V* curves to the model of Eq. 1, a series resistance of ~10 Ω is determined, which mainly results from the low doped substrate and limits the current for high forward voltages. Addressing diffusion-modified SB diodes on p- and n-type sub-

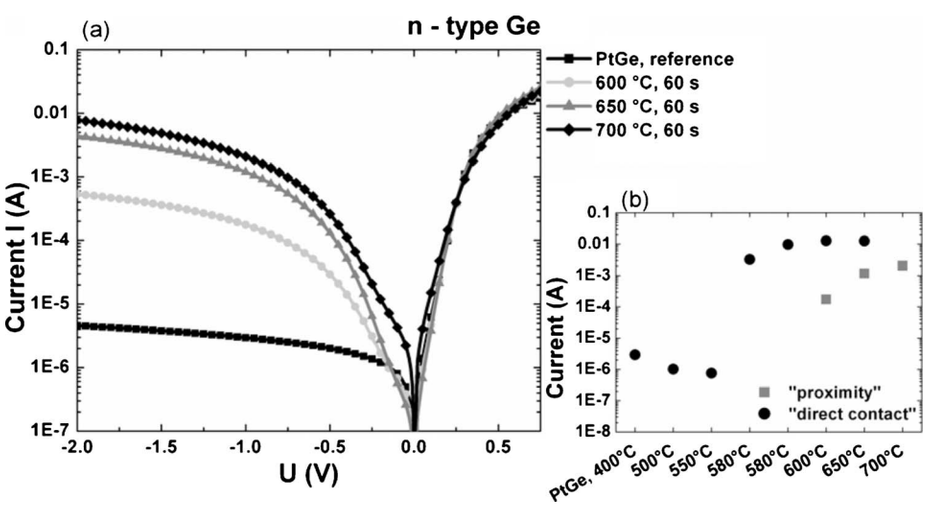

Figure 3. Comparison of room-temperature *I-V* SB characteristics (a) obtained for different annealing treatments for the proximity contact approach. The formation of germanide is performed at 400°C in a forming gas atmosphere. In (b) the comparison of the current contribution in the saturation regime at −1 V as a function of different SOD diffusion parameters is shown and the results to the direct contact diffusion approach are plotted.

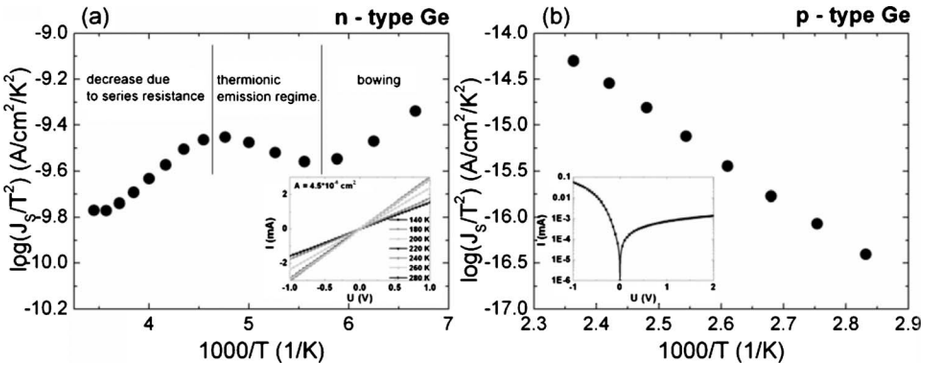

Figure 4. Arrhenius plot of the measured reverse current at a reverse voltage of −0.1 V for the "direct" diffusion approach with an applied diffusion process at 650°C for 30 s on (a) n- and (b) p-type substrates. The insets show the respective *I-V* characteristics measured at 140–280 K for (a) n-type Ge substrates. The inset of (b) shows the *I-V* characteristics measured at 300 K for p-type substrates.

strates, the inset in Fig. 4a and b shows the *I-V* characteristics for both substrates, where the diffusion process is applied at 650°C for 30 s. For Ge n-type substrates, a linear *I-V* characteristic is observed. For temperatures above 240 K a small reduction in the current is observed if the temperature is increased. This is most likely due to the impact of the growing series resistance at higher temperatures. In the temperature regime below 240 K, the current is increasing with higher temperature. The ohmic *I-V* characteristic is still preserved.

To determine the corresponding conduction process, an Arrhenius-type plot is applied (displayed in Fig. 4a). For the intermediate temperature range, the current originates from a thermionic emission current over the resulting SBs. Nevertheless, the region is mainly affected by other contributions to the current, which cannot be addressed by a simple thermal emission process. This could result in an indistinct determination of the SBH. Therefore, a more advanced analysis would be necessary to determine the exact effective barrier height, as given in Ref. 23. At temperatures below 160 K, the values are increasing again. Here, the current cannot be described by a simple Arrhenius-type plot. The bowing observed is usually addressed by the concept of an inhomogeneous distribution of barrier heights at the Ge interface. This can be explained by introducing a Gaussian distribution for the barrier heights to the substrate, resulting in a modified dependency of the extracted barrier height[24]

$$\Phi_{B,e}^{ap} = \Phi_{B,e} - q\sigma_0^2/(2k_BT) \quad [2]$$

Here $\Phi_{B,e}^{ap}$ is the apparent barrier height and σ_0 is the standard deviation assuming a Gaussian distribution. Applying the data to the model of Eq. 2, a barrier height of $\Phi_{B,e} = 0.16$ eV and a standard deviation of $\sigma_0 = 0.05$ eV are obtained.

For the results of the p-type substrate, a linear relationship can be found in the measured temperature range. From the slope of the Arrhenius plot, a barrier height for holes of 0.46 eV is obtained. Table I summarizes the results of both p- and n-type substrates.

Impact of diffusion time.— To investigate the impact of the diffusion time, we applied an RTD treatment at 600°C while keeping ramp rates of heating and cooling constant. Starting at room temperature the temperature is ramped to 500°C at a ramp rate of 10 K/s, and from 500 to 600°C with a rate of 20 K/s. The diffusion times applied are 5, 10, 20, and 30 s at 600°C. The actual diffusion time may be larger due to the finite temperature ramp of heating to and cooling from 600°C. To compare results, the barrier height was extracted on p-type substrates. As can be seen in Fig. 5, a small decrease in the barrier height extracted from the Arrhenius plot is observable for an increase in the applied diffusion time. One possible explanation for this behavior could be an increase in the extent of the n-doped surface layer next to the PtGe surface. As a consequence, the doping profile may not be sharp enough and therefore effective tunneling may be suppressed. Therefore, by applying a faster ramp rate and shorter diffusion times, it may be possible to even increase the pileup in the doping profiles obtained, and therefore improve the tuning ability of the SBH of the diffusion approach.

Spatial resolution of dopant profiles from TOF-SIMS analysis.— In Fig. 6, we compare the results of the TOF-SIMS measurements on PtGe diode structures to the results of diffusion-modified PtGe diode structures. The respective diffusion process is applied at 600°C for 5, 20, and 600 s. A clear pileup of P dopants at the PtGe/Ge interface can be observed. The position of the interface of PtGe to Ge is determined from the position of the O peak related to a small amount of oxygen at the interface region. The sputter rate of PtGe was determined to be ~0.6 nm/s and that of Ge was determined to be ~0.7 nm/s. From the TOF-SIMS analysis we found that a pronounced and well-defined peak of phosphorous atoms is formed at the PtGe to Ge interface. An increasing diffusion time results in the broadening of the detected P signal and in an increased peak height.

Series resistance and cleaning procedures.— To further study the impact of the fabrication process parameters on the electrical properties of SB diodes, we compare the series resistance of the SB diode structure. Compared to the mere PtGe diodes, a decreased current density is observed in the forward regime applying a diffusion process before the germanidation. The extent of this reduction depends on the applied diffusion process conditions. The series resistance can be approximated from the slope of the linear *I-V* characteristics on n-type Ge substrates at 300 K, because the series resistance is dominating the *I-V* properties at these temperatures. A value of ~380 Ω is found for the samples where the SOD diffusion process from the SOD layer is applied at 650°C for 30 s. The series

Table I. Summarization of experimental results for SB diodes with and without dopant segregation. A clear decrease in the barrier height for electrons by the RTD approach can be observed. Additionally, there is an increase in the barrier height for holes.

n-type substrate			p-type substrate
Pt/Ge as deposited 0.65 eV	PtGe 0.67 eV	PtGe SOD 650°C, 30 s 0.16 eV	PtGe SOD 650°C, 30 s 0.46 eV

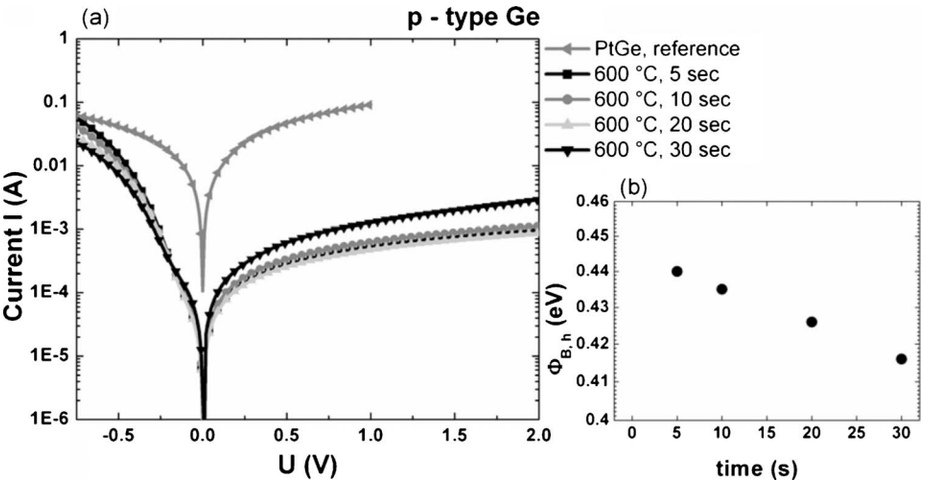

Figure 5. Comparison of room-temperature *I-V* SB characteristics (a) obtained for different annealing treatments after the deposition of the SOD resist layer in the "direct approach" on p-type Ge. The formation of germanide is performed at 400°C in forming gas atmosphere. In (b) the extracted hole SBH at 0 V for different RTD times applied at 600°C for SB diodes fabricated on p-type Ge substrates is shown.

resistance is much higher than the observed 10 Ω series resistance observed for the PtGe sample. If any effect of the back contact on the SB diodes can be neglected, this increase in the series resistance could result from an unoptimized cleaning of the sample surface after the SOD anneal. One drawback of the SOD resist films is that a thin interfacial layer, which is observed after the diffusion process, exists at the wafer surface. This soft interfacial layer is a carbon-rich film and cannot be diluted in HF.[17] It is believed that this film might cause a degradation of the interfacial layer of the Pt/Ge stack before the germanidation process, and finally an increased series resistance. In addition, the effect of bowing, which is modeled by means of a Gaussian distribution of barrier heights, could result from the impact of this interfacial layer. Here, a suitable cleaning procedure that is different from a cyclic BHF and H_2O treatment would be important. One solution could be an additional oxidation step of the topmost Ge surface at temperatures low enough to avoid further diffusion of P dopants. Another option avoiding a high temperature oxidation step could be a plasma oxidation step to remove contaminants from the SOD resist layer before the formation of the PtGe diode structure.

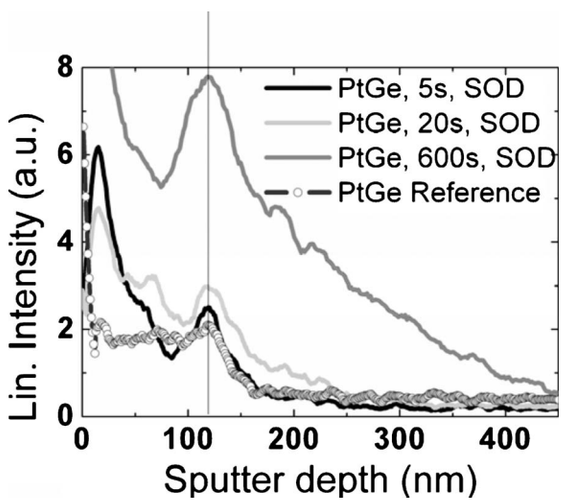

Figure 6. TOF-SIMS measurements on PtGe reference diodes formed on n-type Ge substrates are compared to diffusion-modified samples, where the diffusion process was applied at 600°C for 5, 20, and 600 s. The PtGe/Ge interface, determined from the oxygen peak position, is located at ~120 nm and is indicated by the black bar as a guide for the eyes.

Conclusions and Outlook

We present a method for the reduction in an SB diode on n-type Ge by applying a phosphorous SOD resist for the formation of a highly doped surface layer in a rapid thermal annealing process before the formation of germanide SB diodes. Platinum was used to form the germanide layer. The thermal budget applied can be kept as low as 580°C. Diffusion-modified diodes exhibit the lowest SBH of 0.16 eV and a hole barrier height of 0.46 eV. Thus, the RTD from a solid diffusion doping source is effective in reducing SBHs of platinum germanide SB diodes on Ge. The thermal budgets applied during the diffusion processes are comparable to the activation temperatures used after implantation, while implantation related damages can be avoided. TOF-SIMS measurements show a pileup of the dopants at the PtGe to Ge interface region.

Moreover, the approach may be applicable to three-dimensional device structures owing to the liquid nature of the SOG resist. A challenge remains in the process optimization of surface cleaning after the diffusion process.

Acknowledgments

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