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Low-Defect-Density Ge Epitaxy on Si(001) Using Aspect Ratio Trapping and Epitaxial Lateral Overgrowth

J.-S. Park,[z] M. Curtin, J. M. Hydrick,[*] J. Bai, J.-T. Li, Z. Cheng, M. Carroll, J. G. Fiorenza, and A. Lochtefeld

AmberWave Systems Corporation, Salem, New Hampshire 03079, USA

Low-defect-density Ge epitaxy was fabricated using aspect ratio trapping combined with epitaxial lateral overgrowth techniques. Dislocations from the Ge/Si interface were trapped inside oxide trenches, and then Ge was laterally grown to form 20 μm wide, 6 mm long strips. Chemical mechanical polishing of Ge was used to planarize the faceted strips. Uncoalesced Ge strips showed a defect density as low as 1.6×10^6 cm^{-2} from plan-view transmission electron microscopy, while coalesced Ge had higher defect density. This approach shows great promise for the integration of low-defect-density Ge and III–V materials on Si.
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Epitaxial growth of lattice-mismatched semiconductors on silicon (Si) has been an active area of research for many years. Interest in this area is driven by the many applications which would benefit from the combination of the unique properties of germanium (Ge) and III–V materials with those of Si. These applications are wide-ranging and include high-mobility channel metal-oxide-semiconductor field effect transistors which could enable the continuation of complementary metal oxide semiconductor (CMOS) performance scaling[1,2] and optical devices integrated with Si electronic devices for low-cost, highly integrated photonic circuits.[3] The main barrier to the epitaxial growth of usable Ge and III–V films on Si is the high threading dislocation density (TDD) that occurs in these films due to the lattice mismatch between these materials and Si. For example, Ge directly grown on Si has a TDD of 10^8–10^9 cm^{-2} due to the 4.2% lattice mismatch. Various techniques have been developed to reduce the TDD, such as the use of compositional grading[4,5] and postepitaxial growth high-temperature annealing.[6,7]

Recently a new technique called epitaxial necking[8] or aspect ratio trapping (ART) has begun to show promise.[9,10] ART utilizes high-aspect-ratio holes[8] or trenches[9,10] etched through dielectric films to trap dislocations, greatly reducing the surface dislocation density. This technique has been shown to be effective for growing low-TDD Ge and GaAs selectively on Si in trenches as wide as 400 nm and of arbitrary length.[9,10] A noteworthy advantage of the ART technique is that it uses a very thin dislocation elimination layer, typically just a few hundred nanometers thick. ART thus avoids the thick buffers and high thermal budget typical of other heteroepitaxial techniques, making it much more suitable for integration with Si CMOS processes. However, one shortcoming of ART is that it has been demonstrated to be effective only for small holes or narrow strips with dimensions less than 1 μm. Large areas of Ge and GaAs have been demonstrated using ART by growing out of closely spaced trenches,[11] but additional defects such as dislocations, stacking faults, and twins are generated upon the coalescence of material from adjacent trenches.[8,11-14]

In this study, we demonstrate that the combination of ART with epitaxial lateral overgrowth (ELO) can produce large areas of high-quality lattice-mismatched materials on Si. Using ART + ELO, the fabrication of low-defect-density, 20 μm wide, 6 mm long strips of Ge on Si is demonstrated. We show that the TDD of these films is as low as 1.6×10^6 cm^{-2} and that chemical mechanical polishing (CMP) can be used to produce flat, large areas of Ge on Si with a thickness of less than 1 μm over the Si.

These experiments began with 200 mm diam p-type Si(001) substrates with an 800 nm thick thermal oxide. The oxide layer was patterned into trenches along $[1\bar{1}0]$ having 250 nm width, 6 mm length, and 20 μm spacings. Conventional photolithography and reactive ion etching (RIE) were used to produce trenches. A 25 nm thick sacrificial oxide was formed after the trench etching to remove a fluorocarbon residue on the Si surface caused by the RIE. A dilute HF cleaning was carried out prior to Ge growth. The Ge epi layer was selectively grown from the trenches and over the oxide by reduced-pressure chemical vapor deposition using a process similar to that in Ref. 9 but optimized for high lateral overgrowth. There was no change in the growth conditions of Ge inside the trench and lateral growth over the oxide. CMP of the faceted Ge[15] over the oxide was performed using a Strasbaugh 6EC to flatten the Ge surface.[16] The films were characterized using scanning electron microscopy (SEM), cross-sectional transmission microscopy (XTEM), and plan-view transmission microscopy (PVTEM). The triple-crystal mode of X-ray diffraction (XRD) was used for a high-resolution reciprocal space map (RSM) of diffraction from {004} planes using a Philips X'Pert diffractometer.

Figure 1 shows a schematic of the ART + ELO structures that are the subject of this paper. Ge was grown within the trenches, where the defects were trapped, and then low-defect-density Ge was grown laterally above the trenches for a large distance. Growth conditions were determined which favor the lateral overgrowth at the expense of the vertical growth in order to form thin and wide Ge regions. The triangular facet which forms makes the structures unsuitable for device fabrication and therefore, CMP was used to flatten the tops of the Ge, as shown in Fig. 1b.

Figures 2a and b show cross-sectional and tilted SEM images, respectively, of the structures drawn in Fig 1. The Ge over the oxide is faceted on the {113} plane, which forms a 22° angle between the facet plane and the oxide surface. The ratio between the lateral growth rate and the vertical growth rate was about 3:1. Figure 2c

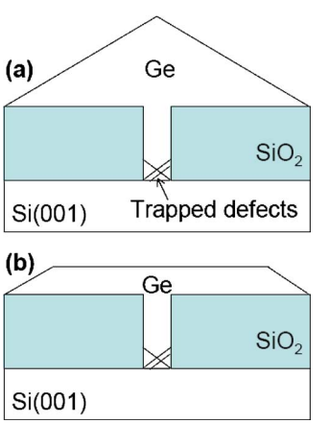

Figure 1. (Color online) Schematics of ELO Ge with ART (a) after Ge overgrowth and (b) Ge CMP.

* Electrochemical Society Active Member.
[z] E-mail: jpark@amberwave.com

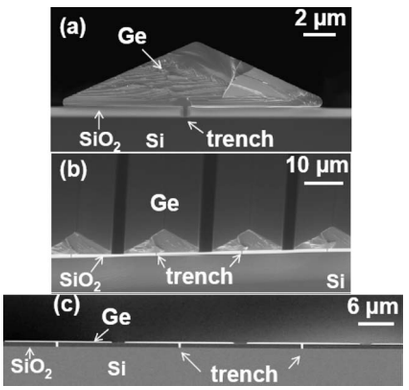

Figure 2. (a) Cross-sectional and (b) tilted SEM images of uncoalesced Ge ELO with ART after Ge overgrowth and (c) cross-sectional SEM image after Ge CMP.

shows a sample in the post-CMP condition where an 18 μm wide, flat surface suitable for device fabrication has been produced.

The defect density of the Ge over the oxide was evaluated using transmission electron microscopy. XTEM images of the left and right sides of the Ge ELO regions grown from the same trench are shown in Fig. 3a and b. Defect trapping is clearly shown inside the trench as indicated by the arrows. Upward-growing threading dislocations associated with misfit dislocations at the Si/Ge interface are trapped by the oxide sidewall in the lower part of the trench, leaving the upper part of the trench nearly defect-free. The material remains

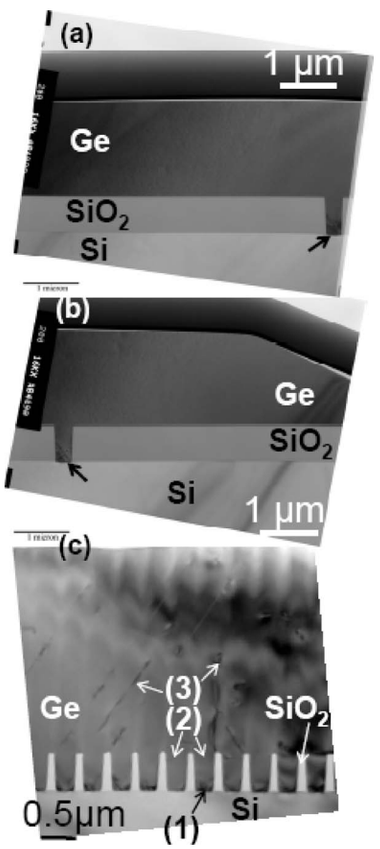

Figure 3. XTEM images of uncoalesced Ge ELO with ART in the (a) left and (b) right side of the same trench indicated by arrows and of (c) coalesced Ge over the oxide trenches with 0.25 μm width and spacing.

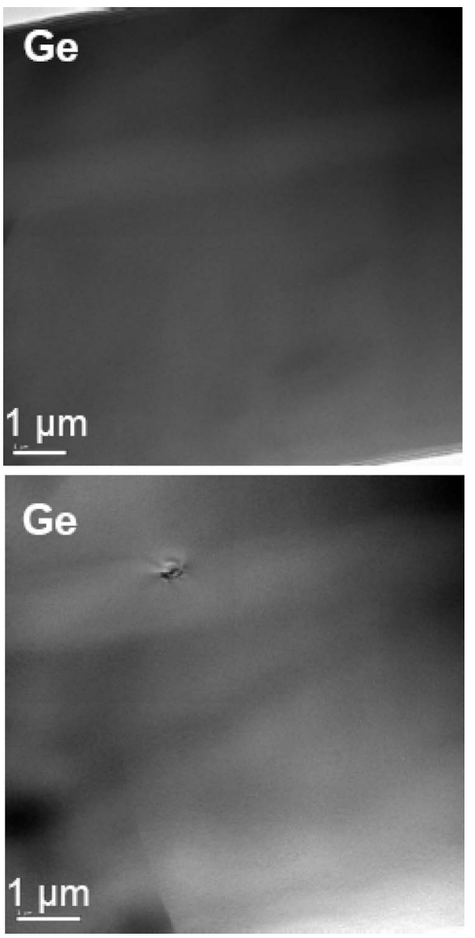

Figure 4. Representative PVTEM images of uncoalesced Ge ELO with ART after Ge CMP.

nearly defect-free as the growth proceeds beyond the trenches. Previous attempts to produce large areas of overgrown film focused on coalescence from adjacent trenches. Figure 3c shows an XTEM image of coalesced Ge over the oxide trenches with 250 nm width and spacing, similar to that demonstrated in Ref. 11. As with the ART + ELO process, growth begins with defects being trapped in the lower regions of the trenches followed by growth into the defect-free upper trench regions, as indicated by (1) and (2), respectively, in Fig. 3b. However, the coalesced Ge over the oxide has additional defects generated upon coalescence, as indicated by (3) in Fig. 3c. The TDD of the structure shown in Fig. 3a was measured by analyzing 19 PVTEM images (Fig. 4), and the TDD, extracted from a cumulative area of about 1900 μm^2, was calculated to be 1.6×10^6 cm^{-2}. It is believed that they are not untrapped dislocations originating from the trench. The dislocations were found uniformly across the film and were not seen to be preferentially found near the trench.

{004} reciprocal lattice space maps of uncoalesced Ge ELO after CMP are shown in Fig. 5a and b along the trench direction and perpendicular to the trench direction, respectively. In both RSMs, Ge has two split peaks along the Q_y. It is believed that the lower intensity peak is from the Ge inside the trench and the higher intensity peak is from the overgrown Ge. The strain level of the two peaks was determined by comparison with the theoretical relaxed Ge peak. The Ge in the trench has a small amount of tensile strain, while the Ge outside the trench has a small amount of compressive strain. From the 2Θ values of lower (65.79°) and higher (66.10°) intensity peaks (2Θ of unstrained Ge {004} is 66.004° from Ge

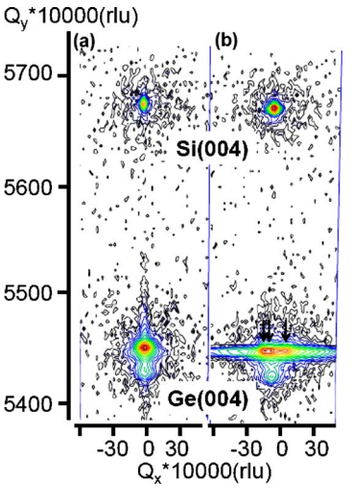

Figure 5. (Color online) RSM of uncoalesced Ge ELO with ART (a) along the trench and (b) perpendicular to the trench.

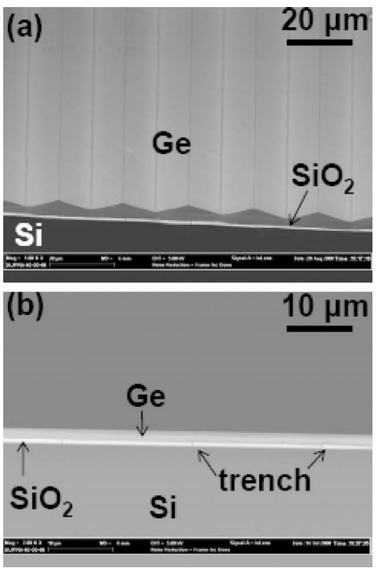

Figure 6. (a) Tilted and (b) cross-sectional SEM images of coalesced Ge ELO with ART after Ge overgrowth and CMP, respectively.

lattice constant 5.657 Å), the lattice constant of the lower and higher peaks was calculated to be 5.673 and 5.650 Å, respectively. From our studies to date, we have seen that the magnitude of the strain does not vary significantly with the thickness or width of Ge strips.

In the case of the RSM for the perpendicular orientation shown in Fig. 5b, the Ge peak has a large spread along Q_x. This spread peak is comprised of three split peaks, indicating that the peak spread perpendicular to the trench may be caused by the tilt of the Ge ELO area. The asymmetric distribution of these three peaks may be ascribed to the uneven ELO growth rates to the left and right of the trench, as shown in Fig. 2a. The residual stress within the trench and in the overgrowth region, as well as some of the peak spread, may be explained by thermal expansion coefficient mismatch between the epi layers and the substrate, the built-in strain in the masking material, and the adhesion and interaction of epi layers with the masking material.[17-19]

For certain device applications, even larger areas of coalesced flat Ge would be preferable. Figure 6a shows coalesced Ge over the oxide prior to the CMP step. A uniformly faceted Ge surface is exhibited. By polishing the Ge down to the bottom of the valley of the {113} facets, a very large area of flat Ge was achieved, as shown in Fig. 6b. The TDD near the coalesced regions was high, about 1×10^8 cm^{-2}, but the defect density in the middle parts of the strips was lower, about 8×10^6 cm^{-2}. In this research, we demonstrate a 20 μm wide and 6 mm long Ge strip with low defect density. From this work we can estimate the maximum allowable trench spacing for a coalesced film. It will be set by the thermal expansion coefficient mismatch between the Ge layer and the Si substrate. The maximum thickness of Ge on Si is about 5 mm, and thicker layers crack because of the thermal expansion mismatch.[20] The {113} facet dictates that 5 μm vertical growth corresponds to 10 μm of lateral growth, and therefore the maximum trench spacing is 20 μm. Greater trench spacing can be used only if the lateral-to-vertical growth rate ratio is increased.

In summary, ART combined with ELO was demonstrated to create large areas of low-defect-density Ge on Si. Dislocations were trapped inside oxide trenches, after which Ge was grown laterally to form very long, 20 μm wide strips. Germanium CMP was used to flatten the faceted strips to make the film suitable for device application. Uncoalesced Ge strips showed a defect density as low as 1.6×10^6 cm^{-2}. XRD measurements indicate that the Ge ELO is nearly fully relaxed but retains small levels of residual strain and tilt. Coalesced, 20 μm wide strips were also grown and polished to form a contiguous layer of Ge. The dislocation density of the coalesced strips was increased relative to the uncoalesced ones. This work demonstrates that the combination of ART + ELO is a viable method to integrate large areas of low-defect-density Ge on Si. This technique may be widely useful for the heterointegration of Ge and III–V electronic and optoelectronic devices on Si.

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