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Impact of Forming Gas Annealing and Firing on the Al_2O_3/p-Si Interface State Spectrum

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The interface-state spectrum at the Al_2O_3/p-Si interface is investigated by Deep-Level Transient Spectroscopy on Metal-Oxide-Semiconductor (MOS) capacitors. It is shown that a Forming Gas Anneal or firing step leads to a significant reduction of the density of interface states (D_{it}). At the same time, it is found that the peak activation energy of the D_{it} distribution lowers towards the valence band of Si. From a comparison with the DLTS data on 5 nm SiO_2 MOS capacitors, it is concluded that the same type of states is observed for both dielectrics, implying that the interface properties are determined by the thin interfacial SiO_2 layer.
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One of the first so-called high-k dielectrics that received considerable research interest from the Complementary Metal-Oxide-Semiconductor (CMOS) scaling community was Al_2O_3.[1,2] When screening high-k materials for the fabrication of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), Al_2O_3 appears to be a good candidate because of its excellent dielectric properties – a high band gap and a reasonable high k value – its strong adhesion to dissimilar materials and its thermal and chemical stability. This explains the strong research interest in the interface and trapping properties of the Al_2O_3/Si system at some point in time.[3–5] Meanwhile, it has become clear that for device scaling alternative high-k materials offer better perspectives, but at the same time, SiO_2/Al_2O_3 bilayer stacks can also be employed for the development of non volatile memories.[6,7] Quite recently, it has been demonstrated that the negative fixed oxide charge in Al_2O_3 is favorable for reaching a good field-induced surface passivation of p-type silicon for solar cell applications.[8–10] This has triggered quite some investigations on the electrical properties of the Al_2O_3/Si system[11–17] and it has been pointed out that both chemical and field-effect passivation play a role in the improvement of the surface recombination properties.[8–10,18,19] A related point of interest is whether the density of interface states (D_{it}) can be reduced by hydrogen passivation, using for example a post-Al-metallization Forming Gas Anneal (FGA).[20–22] At the same time, one should address the question of the stability of the Al_2O_3 properties under a high temperature firing process, which is typically applied between 700 and 850°C.[20]

The present work investigates the interface properties of Al/Al_2O_3/p-Si Metal-Oxide-Semiconductor (MOS) capacitors after various processing steps, namely, as-deposited, after a 30 min FGA (10% H_2 in N_2) at 350°C and after a firing step, consisting of a Rapid Thermal Processing (RTP) with a peak temperature above 800°C for 1–2 s.[23] The FGA and firing steps have been applied after Al gate deposition. Initial results on the surface recombination properties have been recently reported.[24] Deep-Level Transient Spectroscopy (DLTS) is used to generate a D_{it} distribution versus activation energy with respect to the valence band edge E_V. Earlier studies on Atomic Layer Deposited (ALD) 5.8-nm thick Al_2O_3 layers revealed deep-level peaks at 0.19, 0.24, 0.29 and 0.37 eV, respectively.[25] At the same time, it was observed that a FGA at 450°C reduced the D_{it} significantly from 10^{12} $cm^{-2}eV^{-1}$ to 4×10^{11} $cm^{-2}eV^{-1}$ at $E_V + 0.35$ eV. It is shown here that both FGA and firing of 5 nm Al_2O_3 layers result in a clear reduction of the D_{it}, whereby also the activation energy, corresponding with the DLTS peak maximum reduces. A similar behavior is observed for 5 nm thermal SiO_2 reference samples, indicating that the observed interface states are related with the thin interfacial SiO_2 layer which is formed upon Al_2O_3 deposition.

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Before deposition, the 200 mm diameter p-type Czochralski Si substrates were cleaned in a hot H_2O_2:H_2SO_4 1:4 solution, followed by an HF-dip and a water rinse. Forty cycles of ALD Al_2O_3 was performed in a Savannah tool at 200°C, with H_2O as the oxygen precursor and trimethyl-aluminum (TMA) as the Al precursor, resulting in a thickness of 5 nm. The pulsing sequence was H_2O, TMA, H_2O. This was followed by the sputtering of 500 nm thick Al gate electrodes with different diameters. The 5 nm SiO_2 reference capacitors were fabricated using *in-situ* steam generated oxidation at 850°C.

Before DLTS, 1 MHz Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements have been performed at room temperature in order to define a proper bias-pulse range for the DLTS measurements. It turns out that the typically 500 μm diameter Al capacitors generally suffer from a rather high forward gate leakage current from the 1 μA to the several 100 μA range at -2 V, which affects the 1 MHz C-V characteristics in the accumulation region, as shown in Fig. 1. The tendency for leaky devices increased for the FGA or fired samples, suggesting a correlation with the damaging or degradation of the oxide by creating trapping centers. For reasons of sample-mounting in the DLTS holder, only large-diameter ($\geq$400 μm) dots could be handled. Whenever possible, capacitors with low gate current have been characterized by DLTS. Alternatively, a pulse bias V_P was chosen sufficiently into accumulation to fill the interface traps but avoiding a high gate current (e.g. >-1 V in Fig. 1), which may result in electron injection and recombination and gives rise to negative, minority-carrier deep-level peaks.

DLTS has been performed using a Fourier-Transform-based digital system. Spectra have been obtained either from a frequency scan at room temperature or a temperature scan from 75 to 320 K, typically, whereby the capacitors are repetitively pulsed from a depletion bias (V_R) into accumulation (V_P), during a pulse time t_p. Further experimental details have been reported before.[26,27]

According to the isothermal DLT-spectra of Fig. 2, a pronounced deep-level peak is observed in the as-deposited samples at room temperature. It is also clear that the associated traps occur at the Al_2O_3/p-Si interface since the spectrum recorded in depletion from 4 to 2 V, which only probes traps in the Si substrate, is essentially flat. After FGA or firing, the magnitude of the peak has drastically reduced, suggesting partial passivation of the underlying interface states by atomic hydrogen. At the same time, the peak maximum shifts to a lower sampling period t_w, indicating a lowering of the activation energy towards the valence band. Note that in Fig. 2 the DLTS amplitude has been divided by the steady-state capacitance in order to have a better quantitative comparison of the spectra for the different samples.

Since the spectra of Fig. 2 are associated with interface states, a D_{it} spectrum can be calculated, following the procedures outlined elsewhere.[26,27] The result is displayed in Fig. 3, confirming the conclusion derived from Fig. 2, namely, that FGA and firing lowers the D_{it} at the Al_2O_3/p-Si interface and at the same time moves the distribution towards lower activation energies. In the calculation of the

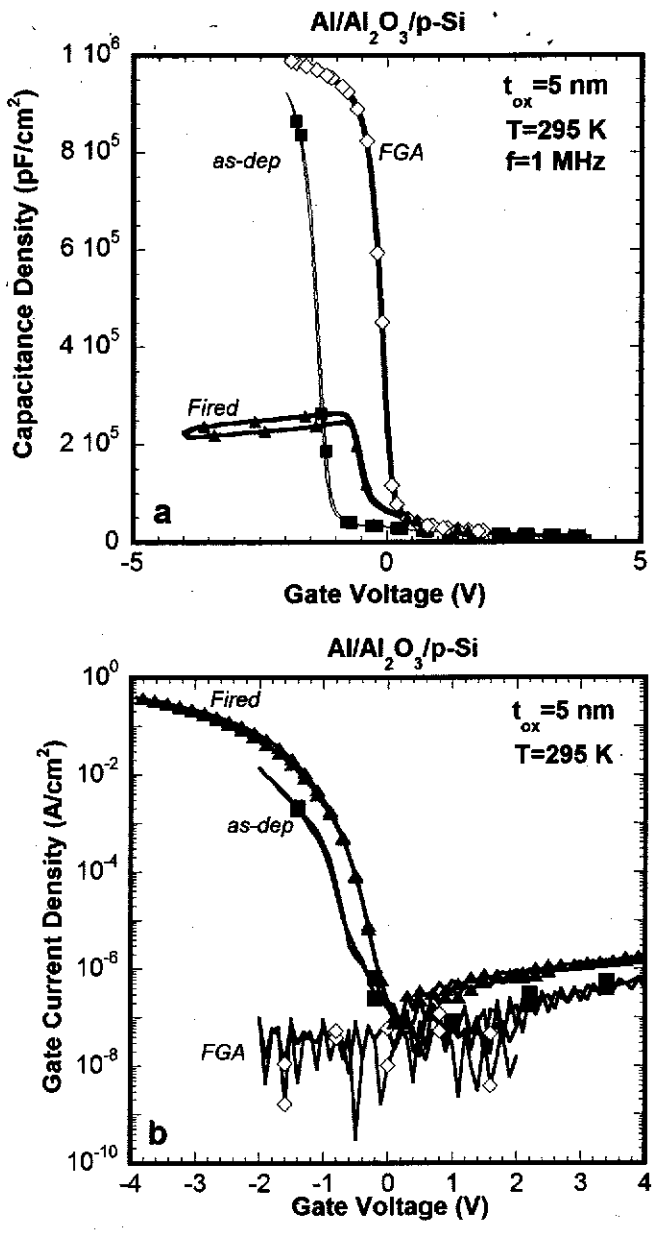

Figure 1. Capacitance-Voltage at 1 MHz (a) and Current-Voltage (b) characteristics at room temperature for a 5 nm Al_2O_3 MIS capacitor as-deposited (■); after FGA (◇) and after a firing step (▲).

activation energy, a constant hole capture cross section of 10^{-15} cm^2 was taken, which corresponds with the energy-averaged value, that has been derived from the intercept of the Arrhenius plots obtained from small-pulse-height measurements as a function of temperature. The peak D_{it} values for the as-deposited Al_2O_3 sample are rather high, but are on the same order of magnitude as was reported recently for plasma ALD and O_3-ALD, where C-V measurements revealed densities in the range $\sim 10^{13}$ $eV^{-1}cm^{-2}$.[28] However, much lower values on the order of 3×10^{11} eV^{-1} cm^{-2} have been found for H_2O-ALD layers on p-Si.[28] In addition, a D_{it} below 10^{11} $eV^{-1}cm^{-2}$ was reported for as-deposited H_2O-ALD Al_2O_3 layers from conductance measurements using a mercury probe.[29] This suggests that the Al-gate deposition may also be partly responsible for the "as-grown" D_{it}.[30] Previous reports demonstrated a significant lowering of the D_{it} by FGA at the Al_2O_3/p-Si interface.[22,28] At the same time, it is shown that a low D_{it} is also obtained after a firing step only, in perfect agreement with the observations of Benick et al. and confirming the stability of the surface passivation after solar cell processing.[20]

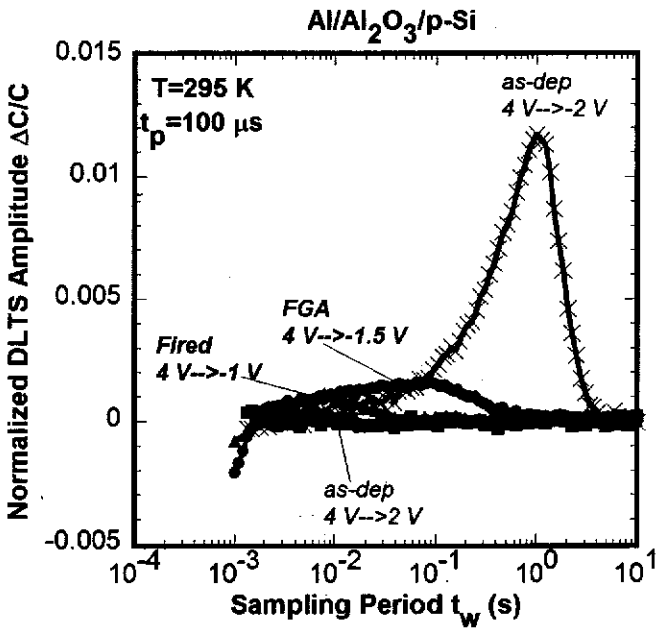

Figure 2. (Color online) Isothermal frequency scan at room temperature for Al_2O_3 MOS capacitors on p-Si, corresponding with: as deposited layer [pulse 4 V–>−2 V (x) and 4 V–>2 V (■)]; after FGA [4 V–>−1.5 V (•)] and after firing [4 V–>−1 V (▲)]. A fixed pulse duration of 100 μs was used.

Comparing the D_{it} distribution of Fig. 3 for Al_2O_3 capacitors with the 5 nm SiO_2 reference samples in Fig. 4, one can conclude that rather similar results are obtained in both cases: a reduction of the D_{it} upon FGA and a shift towards lower activation energies. Note that according to the data of Figs. 3 and 4, FGA seems to be more effective in the case of Al_2O_3, which could be related to the presence of atomic H in the high-k layer coming from the H_2O precursor. Note that the peak D_{it} value for as-grown SiO_2 is on the high side, compared with data obtained on 25 nm SiO_2 layers on p-type Si.[31] Especially after FGA, the remaining D_{it} is still rather high

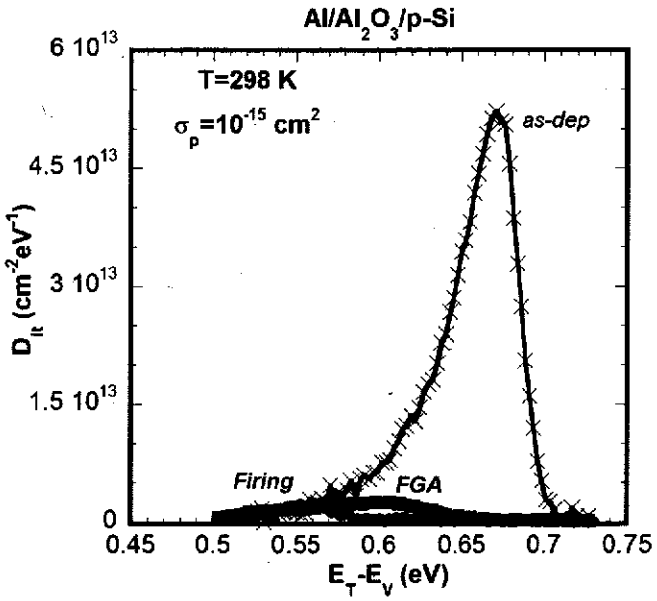

Figure 3. (Color online) Density of interface states versus energy with respect to the valence band maximum for an as-deposited Al_2O_3 sample, after FGA and after a firing step. A hole capture cross section of 10^{-15} cm^2 has been assumed.

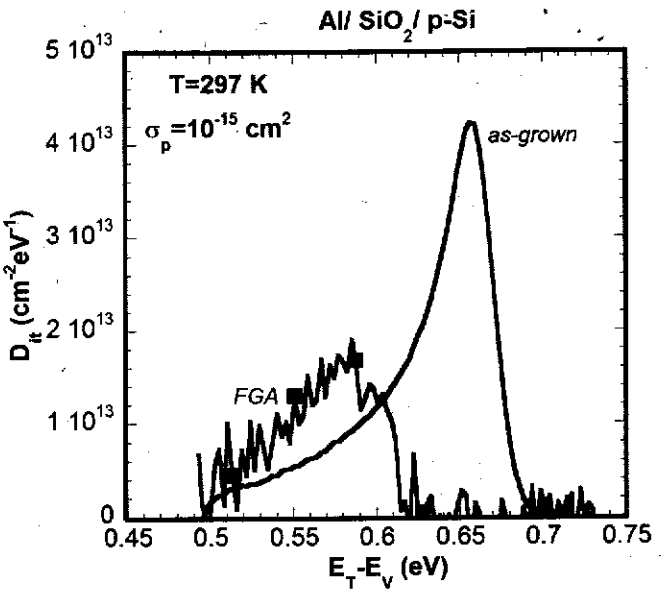

Figure 4. (Color online) D_{it} distribution for 5 nm SiO_2 MOS capacitors on p-type Si: as-grown and after FGA.

indicating that the hydrogen passivation is not so effective for the observed mid-gap interface states, in line with other recent observations.[22,26,27] Note finally that the FGA conditions chosen here are not optimal for interface state passivation but have been selected to yield the best recombination lifetime for our process conditions.

At the same time, one should be cautious in drawing too strong quantitative conclusions, as the DLTS and D_{it} spectra can exhibit quite some device to device scatter, as illustrated by Fig. 5. However, the similarity of both distributions in Figs. 3 and 4 strongly suggests that the same type is of interface traps are being probed, namely associated with the Si/SiO_2 interface. In the case of the Al_2O_3 samples, the interface states are formed at the thin SiO_2 interfacial layer. X-ray Photo-Electron (XPS) spectroscopy revealed no detectable SiO_2 in the as-deposited samples, but after FGA and firing, a regrowth occurs, yielding a thickness of 0.26 and 1.51 nm, respectively. This is also confirmed by Electron Spin Resonance (ESR), showing the presence of $\sim 10^{12}$ cm^{-2} dangling bond centers, typical for the SiO_2/Si interface.

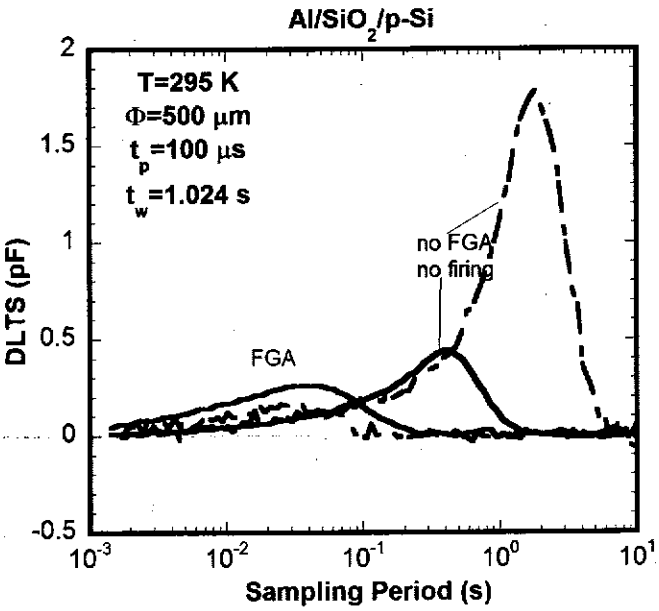

Figure 5. (Color online) DLT-spectra for two 5 nm SiO_2 samples without post-metallization treatment (no FGA, no firing) and two samples after FGA, showing the sample-to-sample dispersion.

In summary, it has been shown by DLTS that the density of interface states is strongly reduced after post-Al-metallization FGA or firing of $Al/Al_2O_3/p$-Si MOS capacitors, while at the same time, the activation energy of the interface states shifts to lower values. Both factors should contribute to the improvement of the surface recombination properties of Al_2O_3 passivated p-type Si.

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