STUDY OF PZT FILM STRESS IN MULTILAYER STRUCTURES FOR MEMS DEVICES

E. ZAKAR, M. DUBEY, R. POLCAWICH*, B. PIEKARSKI, R. PIEKARZ,
J. CONRAD, R. WIDUTA
US Army Research Laboratory, Adelphi, MD 20783, ezakar@arl.mil
*GTS contractor

ABSTRACT

Residual stress in the multilayer Si/Dielectric/Pt/PZT/Pt stack was measured as a function of annealing conditions, sol-gel derived PZT (Lead Zirconate Titanate -52/48) thickness, SiO_2 and/or Si_3N_4 dielectric films thickness. Residual stress in the Si_3N_4 layer varied from -201 to +1275 MPa and from -430 to + 511 MPa in the SiO_2 layer. Furnace annealing of the bottom Pt film reduced the stress over rapid thermal annealing (RTA). Stress due to PZT films was the controlling factor for the final stress of the stack. Upon increasing PZT thickness, stress became less tensile for Si_3N_4 dielectric and more tensile for SiO_2. The deposition of the top Pt on PZT followed by RTA at 300°C in nitrogen had a minimal effect on the final stress of the stack. The average tensile stress for the Si/SiO_2 /Pt/PZT/Pt and Si/Si_3N_4/Pt/PZT/Pt stacks was140 ± 25 and 476±235 MPa respectively.

INTRODUCTION

Optimum performance of PZT MEMS devices is highly dependent on the mechanical properties (e.g. residual stress) of the underlying films. Knowledge of stress in the Si/Dielectric/Pt/PZT/Pt stack with SiO_2 and Si_3N_4 dielectric layers is also valuable for developing novel devices requiring release processes such as cantilevers and bridge structures. A fabrication process has been reported for development of a prototype PZT pressure sensor [1] and microresonator [3] using sol-gel derived PZT films [2]. Study of PZT stress has been reported [4,5,6] but is limited. In the present study, residual stress of each layer in the stack was measured with varying thickness of dielectrics and PZT, along with annealing conditions. We also compared the stress in the bottom Pt electrode due to RTA and furnace annealing.

EXPERIMENT

Plasma Enhanced Chemical Vapor Deposition (PECVD) was used to deposit SiO_2 and Si_3N_4 films at 250°C on 3-inch Si substrates. The SiO_2 thickness was 250, 600, and 700 nm, and Si_3N_4 was155 and 300 nm. Stress in the dielectric films was measured using as-deposited as well as RTA films at 700°C for 60 sec in nitrogen. Bottom platinized electrode was prepared using sputter deposited Pt (170 nm) on top of a Ta (20 nm) adhesive layer on the dielectric followed by RTA at 700°C for 60 sec in nitrogen. Sol-gel PZT film was spin coated [2] on the platinized substrates and crystallized at 700°C for 60 sec in air. Top Pt electrode was sputter deposited and RTA at 300°C for 60 sec in nitrogen.

Residual stress due to PZT film thickness was studied using 250, 500, and 1000 nm thick PZT on a 600 nm thick SiO_2 film in the Si/Dielectric/Pt/PZT/Pt stack. The effect of RTA and

Mat. Res. Soc. Symp. Proc. Vol. 605 © 2000 Materials Research Society

furnace annealing was studied by annealing the Si/Dielectric/Pt stack at 700°C in RTA, 60 sec, as well as in furnace @15°C/min ramp rate.

Tencor FLX-2908 system was used to measure the changes in the radius of curvature of the substrate caused by deposition of the films. Measured negative values for stress indicated a compressive stress and positive ones a tensile stress. We utilized the in-situ heating capability of the system to perform the furnace annealing and stress measurement.

RESULTS AND DISCUSSION OF STRESS MEASUREMENTS

Measured stress data were mainly categorized in four groups. The first group, reported in section1 below, consisted of measured stress on the SiO_2 and Si_3N_4 films having different thickness, Pt deposited on the dielectric (as-deposited, as well as RTA annealed) films, RTA of the deposited bottom Pt, spin-coated PZT film (500 nm) on the bottom Pt, deposition of Pt on the PZT, and RTA of the top Pt.

The second group of the measured data (section 2) was related the different thickness of the PZT films on a platinized substrate having a fixed (600 nm) SiO_2 film thickness.

The third group data (section 3) was taken with incremental increases of 250 nm PZT films on two different types of platinized substrates, one having SiO_2 (700 nm), and the other Si_3N_4 (300 nm) films under the bottom Pt layer.

The fourth group data (section 4) was obtained after annealing the platinized substrates separately in furnace and RTA followed by PZT deposition on both.

1.a. Si/Dielectric/Pt stack:

Stress was measured on a Si/Dielectric/Pt stack with several dielectric layer (SiO_2, Si_3N_4) thicknesses at various stages of deposition and annealing. The results are shown in table 1. Stress due to deposition of bottom Pt films on as-deposited SiO_2 did not change appreciably, while it increased compressively for Si_3N_4 as show in table 1. But in all cases the stress changed to tensile and increased to over 1000 MPa after annealing the stack in RTA at 700°C. This is due to film recrystallization during annealing. After cooling to room temperature, a large tensile stress developed due to the larger thermal expansion of Pt compared to Si [6].

Table 1. Stress of the (Si/ Dielectric/Pt) stack at various stages with as-deposited dielectric layers.

	SiO_2 thickness (nm)			Si_3N_4 thickness (nm)	
	250	**600**	**700**	**155**	**300**
Stress (MPa)					
1. Dielectric as-deposited	-400	-450	-460	-88	-201
2. Pt-bottom as-deposited	-425	-455	-465	-311	-380
3. RTA (700°C)	1001	1100	1145	1190	1260

Effect of annealing of as-deposited dielectric films, before Pt deposition, was also investigated. The as-deposited (Si/Dielectric) stacks were RTA at 700°C followed by Pt

deposition and RTA at 700°C. Stress measurements on these stacks at various stages of deposition and annealing are shown in table 2.

Measured stress changed from compressive to tensile upon annealing of both SiO_2 and Si_3N_4 layers. Annealing of SiO_2 eliminates micropours in the film that accommodate water vapor [7]. In the case of Si_3N_4 films, trapped hydrogen is released leaving the film tensile. Measured stack stress subsequent to the final process step 4 of table 2 with SiO_2 dielectric was substantially lower than similar SiO_2 dielectric stack of table 1. It appears that for every 100 nm addition of the SiO_2 layer, the tensile stress was reduced by approximately 80 MPa. Stress for the SiO_2 stack was reduced below 1000 MPa while it remained above 1000 MPa for the Si_3N_4 stacks.

Table 2. Stress of (Si/ Dielectric-annealed /Pt) stack

	SiO_2 thickness (nm)			Si_3N_4 thickness (nm)	
	250	**600**	**700**	**155**	**300**
Stress MPa)					
1. Dielectric as-deposited	430	430	430	-88	-201
2. RTA (700°C)	50	50	50	467	1160
3. Bottom Pt dep.	-75	-75	-75	-420	601
4. RTA (700°C)	511	283	201	1148	1275

1.b. Si/Dielectric/Pt/PZT stack:

The above stack of table 2 was spin coated with a 500 nm thick layer of PZT and RTA crystallized at 700°C for 60 sec as shown in step 5 of table 3. The measured stress data shown in this table indicate a resultant reduction in tensile stress upon PZT deposition and annealing.

Table 3. Stress of (Silicon/ Dielectric/Pt/PZT) stack

	SiO_2 thickness (nm)			Si_3N_4 thickness (nm)	
	250	**600**	**700**	**155**	**300**
Stress (MPa)					
5. PZT crystallized	155	201	151	345	725

1.c. Si/Dielectric/Pt/PZT/Pt stack:

The stacks, exhibited in table 3, were further used for deposition and annealing of Pt electrode as shown by steps 6 and 7 of table 4. Subsequent stress measurements were performed and the results are shown in this table. The stress of the SiO2 and Si_3N_4 stacks did not change considerably after RTA at 300°C, 60 sec. Tensile stress for the SiO_2 stack was in the range of 110-165 MPa and for the Si_3N_4 in the 242-711 MPa range.

Table 4. Stress of Silicon/Dielectric/Pt/PZT/Pt stack

	SiO_2 thickness (nm)			Si_3N_4 thickness (nm)	
	250	**600**	**700**	**155**	**300**
Stress (MPa)					
6. Top Pt	109	159	142	239	704
7. RTA (300°C)	110	165	145	242	711

2. Si/SiO_2/Pt/(PZT-variable thickness) film:

Stress due to variation in the PZT thickness on a fixed SiO_2 thickness layer was also measured. Base wafers, with 600 nm thick SiO_2 were platinized as described in table 2 (steps 1, 2, 3, 4). Several PZT films of 250, 500, and 1000 nm thickness were deposited on the base wafers along with Pt layers deposited and annealed as shown by steps 5, 6, and 7 of table 5. Stress measurements were performed at each step, and the results are shown in this table. The 1000 nm thick PZT film stack produced 257 MPa stress compared to 183 MPa for the 250 nm PZT film stack.

Table 5. Stress due to variation in PZT thickness on (Si/SiO_2-600 nm-annealed/Pt) stack

	PZT film thickness (nm)		
	250	**500**	**1000**
Stress (MPa)			
5. PZT crystallized	183	208	257
6. Pt top deposition	105	155	190
7. RTA (350°C)	110	161	196

3. Effect of incremental addition of PZT thickness:

Stress was also studied as a function of incremental increase of PZT thickness on two different types of (Si/Dielectric/Pt) stacks. Two test wafers had a dielectric of 700 nm SiO_2 while another test wafer had a 300 nm Si_3N_4 layer. Figure 1 shows the stress variation due to subsequent 700°C RTA, Pt deposition and annealing, and incremental addition of PZT thickness.

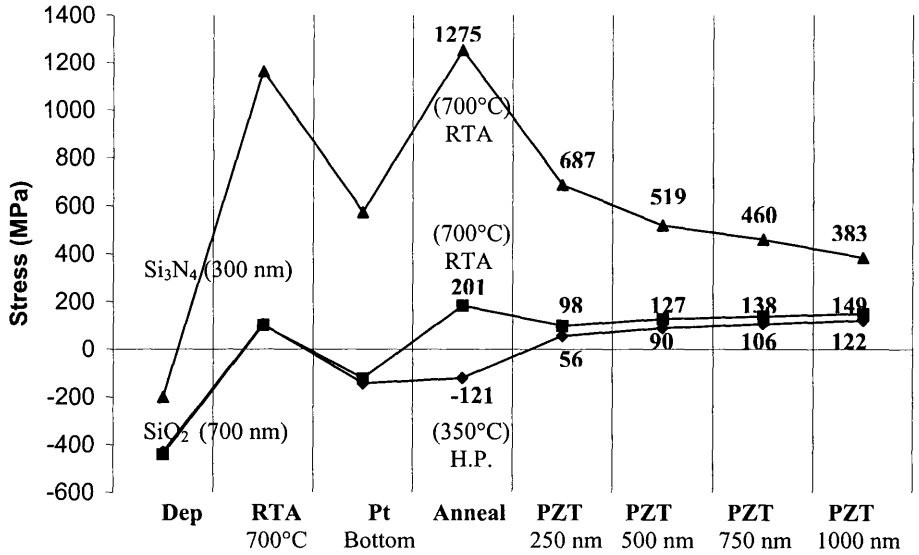

Fig 1. Measured stress at different deposition and annealing steps for two SiO2 and one Si_3N_4 dielectric test wafers.

The first 250 nm increment of PZT film deposited on $Si/Si_3N_4/Pt$ reduced the stress from 1275 to 687 MPa, and it further decreased to 519, 460, and 383 MPa after successive increments of 250 nm in the PZT thickness (i.e. 500, 750, and 1000 nm respectively).

When the first 250 nm film of PZT was deposited on $Si/SiO_2/Pt$, with Pt RTA at 700°C, the stress reduced from 201 to 98 MPa. However, during successive increments of 250 nm PZT thickness (500, 750, and 1000 nm), the stress increased to 127, 138, and 149 MPa respectively.

In another experiment, Pt was deposited on a SiO_2 test wafer and annealed at 350°C on a hot plate for 2 min. The measured stress was -121 MPa, but with successive increments of 250 nm PZT thickness (250, 500, 750, 1000 nm), the stress increased to 56, 90, 106, 122 MPa respectively, which followed the trend of the sample RTA treated at 700°C.

4. Stress due to RTA and Furnace annealing of bottom Pt:

Stress on the bottom Pt electrode due to RTA and furnace annealing was also measured. Two Si/SiO_2 base wafers with SiO_2 (600 nm, RTA 700°C), and as-deposited Pt layers were used for this comparison. Stress in the one wafer was 204 MPa after furnace annealing at 700°C, while stress in the other was 283 MPa after RTA at 700°C. When the furnace-annealed sample was further re-annealed in RTA at 700°C, stress increased from 204 to 281 MPa. Similarly, when the RTA treated sample was further re-annealed in a furnace at 700°C, stress decreased from 283 to 222 MPa. In figure 2 it appeared that furnace annealing produced lower stress than RTA.

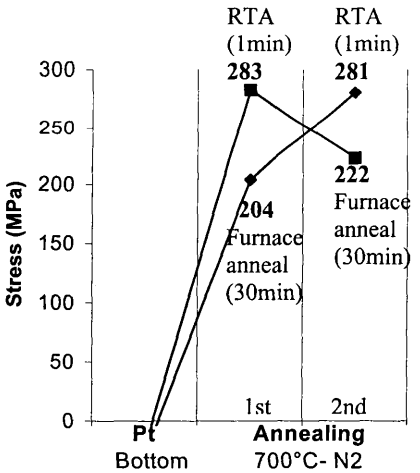

Fig 2. Effect of two separate annealing treatments on platinized oxide substrates.

The reasons for the difference in stress due to annealing conditions could be due to interfacial reactions [8].

CONCLUSIONS

The Si/Dielectric/Pt/PZT/Pt stacks with Si_3N_4 dielectric films had very large stress variations as function of dielectric thickness, compared to those with SiO_2 films. Annealing of the deposited dielectric films in nitrogen reduced the stress of the stack. It appears that furnace annealing of PZT films may produce lower residual stress in the films compared to RTA. Stress due to PZT film had a dominating effect on the final stress of the Si/Dielectric/Pt/PZT/Pt stack, and was thickness dependent. For the stack prepared with SiO_2 as the base film and PZT in the thickness range 250-1000 nm, the residual stress values were within 140 ± 25 MPa tensile.

ACKNOWLEDGEMENT

Authors are grateful to Dr. R. Zeto, G. McLane of GTS for their constructive comments and suggestions.

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