Uniformity studies of inductively coupled plasma etching in fabrication of HgCdTe detector arrays

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ABSTRACT

Inductively coupled plasma (ICP) chemistry based on a mixture of CH_4, Ar, and H_2 was investigated for the purpose of delineating HgCdTe mesa structures and vias typically used in the fabrication of second and third generation infrared photo detector arrays. We report on ICP etching uniformity results and correlate them with plasma controlling parameters (gas flow rates, total chamber pressure, ICP power and RF power). The etching rate and surface morphology of In-doped MWIR and LWIR HgCdTe showed distinct dependences on the plasma chemistry, total pressure and RF power. Contact stylus profilometry and cross-section scanning electron microscopy (SEM) were used to characterize the anisotropy of the etched profiles obtained after various processes and a standard deviation of 0.06 μm was obtained for etch depth on 128 x 128 format array vias. The surface morphology and the uniformity of the etched surfaces were studied by plan view SEM. Atomic force microscopy was used to make precise assessments of surface roughness.

Keywords: HgCdTe, inductively coupled plasma (ICP), etching, mesa, via, etch rate, $CH_4/Ar/H_2$, detector array

1. INTRODUCTION

Mercury cadmium telluride (MCT) is the material of choice for the fabrication of high performance infrared photon detectors. Significant developments have been made over the past decades in the growth of high quality MCT by molecular beam epitaxy (MBE)[1,2] and in the processing technology for fabricating devices with the grown material. A principal bottleneck in the processing technology for next generation devices is the etching of the semiconductor active areas, specifically in that the latent mask pattern developed in the photoresist needs to be transferred without distortion into the wafer. The semiconductor industry has witnessed several etching technologies over the years, particularly in the development of metal-oxide-semiconductor (MOS) devices. However, the fabrication of devices over large areas requires significant improvements in the control of etch uniformity and reproducibility in order to achieve high yields. The third generation of infrared detectors features complex device architectures for large format two color detectors, avalanche photodiodes, and hyperspectral focal plane arrays that have higher sensitivity and performance over the conventional devices fabricated in the last two generations. The fabrication process for HgCdTe infrared detectors has been primarily based on Br/Methanol wet etching process that limits the delineation of small pixel features due to the isotropic nature of the etch process. The damage threshold of HgCdTe to high-energy ions is low and hence it is a major challenge to develop a low damage anisotropic dry etch process that facilitates a high fill factor and good uniformity over large areas.

The development of an etch process for MCT is a complex endeavor because the etch parameters are not always predictable. Wet etching has been widely used for MCT since the early days of growth of this material, with alcoholic solutions of bromine being the most reported wet etchants[3]. Wet etching is isotropic, so the resultant uniformity is low, which limits the size of the devices produced. Advanced devices such as two color, avalanche photodiodes and

[1] R. Sporken, S. Sivananthan, K.K. Mahavadi, G. Monfroy, M. Boukerche, and J.P. Faurie, Appl. Phys. Lett., 55, 1879 (1989).
[2] S. Sivananthan, Y. P. Chen, P. S. Wijewarnasuriya, J. P. Faurie, F. T. Smith and P. W. Norton, Proceedings of the 7th International Conference on Narrow Gap Semiconductors (1995).
[3] I.M. Kotina, L.K. Tukhonen, G.V. Patsenkina, A.V. Schucharev, and G.M. Gusiniskii, Semicond. Sci. Technol., 13, 890 (1998).

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superlattice-based detectors require mesa isolation from the contacts and hence require deep etching with high aspect ratios and minimum structural damage. These requirements motivate the development of dry etch processes for MCT. Dry etch technology offers the ability to produce anisotropic etch profiles, resulting in more photodiodes per unit area. In addition to the anisotropic nature of etching, which is critical for accurate dimensional control, dry etching provides greater uniformity, smaller amounts of hazardous waste and an in situ vacuum processing capability[4]. Dry etching is a standard process technology used in the fabrication of Si and III-V semiconductor devices, but the application of this technique to MCT device production has been rather limited because of the low damage threshold of MCT. Various dry etch mechanisms have been developed for MCT, and extensive research is still underway to develop the best possible technique.

Dry etching eliminates the handling of hazardous acids and solvents, provides high resolution and cleanliness, better process control and less undercutting. There are two types of dry etching: ion-beam-assisted and plasma-assisted dry etching.

In ion beam etching, a substrate surface is slowly etched with a stream of high energy (200-1500 eV) ions. This is a purely physical process that is capable of highly anisotropic pattern transfer, but its selectivity is poor and it can induce both mechanical and electrical damage. The ion beam milling of HgCdTe has been reported to damage the stoichiometry even to the extent of converting p-type material to n-type[5].

Plasma etching is a relatively new technique in the fabrication of integrated circuits. It was introduced in the seventies for stripping photoresist and by the eighties it became a mature technique to etch layers and was introduced in the production of integrated circuits. Plasma etching with H_2, Ar and CH_4[6] has been reported as being extensively used for MCT. Initially, reactive ion etching (RIE) technique was the primary plasma etching technology, but new techniques such as electron cyclotron resonance (ECR) plasma etching and inductively coupled plasma (ICP) etching now have been developed. Reactive ion etching is a combination of physical and chemical etching, which gives a good anisotropic etch for fabricating mesas with high aspect ratios. Various groups have used RIE with a CH_4/H_2 plasma to etch MCT with reasonable success, but the process leads to a high surface roughness. Also, the material is not immune to type conversion due to the physical component of the etch process.[7] ECR is a plasma etching technique that generates a high-density plasma with low ion energies. A microwave frequency matched to the cyclotron resonance frequency of the electrons in a constant magnetic field is used as the means of generating a high-density plasma. These plasmas are denser than RF plasmas and possess lower ion energies. They produce smooth, damage-free surfaces after etching. The ECR plasma etching of MCT has been performed by various groups with various gas mixtures, such as CH_4/H_2,[8] $CH_4/H_2/Ar$,[9] $CH_4/H_2/Ar/N_2$[10] and Ar/H_2.[11] ECR etching has shown reasonable success for etching high-aspect-ratio trenches and mesas for avalanche photodiodes and focal plane arrays, yet it has not shown good uniformity over large area wafers. An alternative high density plasma etching technique is inductively coupled plasma (ICP) etching. This is a preferred technique for the etching of larger wafers to be processed with high uniformity, and also allows a greater automation capability than does ECR plasma. ICP etch process has been previously reported to produce greater etch uniformity relative to ECR process for fabricating 30 μm pixels[12].

In this paper, we present an analysis of ICP etch processes performed on HgCdTe using a variable area mesa device mask and also a 128x128 pixel format array featuring 10 μm vias on a 25 μm pitch. Unlike the mesa pixels that are generally reported, we report etch process results on trench unit cells that can be used for two color detectors. The etch rate as a function of the process conditions, CH_4 gas flow, Ar gas flow, RF Power, ICP power and chamber pressure, is evaluated to develop a viable etch process for fabricating pixels with reduced dimensions.

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[4] J.E. Spencer, H.H. Dinan, P.R. Boyd, H. Wilson, and S.E. Buttrill, J. Vac. Sci. Technol., A 7, 676 (1989).
[5] R. Haakennaasen, T. Coloin, H. Steen and L. Trosdahl-Iversen, J.Electron. Mater., 29, 849 (2000).
[6] M.A. Foad, C.D. Wilkinson, C. Dunscomb and R.H. Williams, Appl. Phys. Lett., 60, 2531 (1992).
[7] J. Antoszewski, C.A. Musca, J.M. Dell, and L. Faraone, J. Electron. Mater., 32, 627 (2003).
[8] C.R. Eddy Jr, E.A. Dobisz, J.R. Meyer, and C.A. Hoffman, J. Vac. Sci. Technol. A11, 1763 (1986).
[9] R.C. Keller, M. Seelman Eggbert, and H.J. Richter, J. Electron. Mat., 24, 1155 (1995).
[10] J. Kim, T.S. Koga, H.P. Gillis, M.S. Goorsky, G.A. Garwood, J.B. Varesi, D.R. Rhiger and S.M. Johnson, J. Electron. Mater., 32, 677 (2003).
[11] A.J. Stoltz and J.D. Benson, J. Electron. Mater., 32, 692 (2002).
[12] E.P.G. Smith, J.K. Gleason, L.T. Pham, E.A. Patten and M.S. Welkowsky, J. Electron. Mater., 32, 6, 816 (2003).

2. EXPERIMENTAL DETAILS

Etching was carried out in a Plasmalab System 100 ICP380 system. The system has a ceramic ICP tube 380 mm in diameter. The ICP source was supplied with 2 MHz power from a 5000 W capacity generator. The bottom electrode of the ICP chamber was a fixed height 240 mm aluminum electrode independently biased with 13.56 MHz RF power from a 600 W capacity generator. The electrode has a wide temperature option (control in the range -150°C to +400°C). Helium backside temperature control was used to maintain a room temperature process in the chamber to avoid any damage to the HgCdTe layers. Gas sources of CH_4, Ar and H_2 were primarily used for the etch chemistry on the samples. MBE grown multiple layer HgCdTe samples were used for performing a detailed study of the ICP etch process. The HgCdTe samples were mid wavelength infrared (MWIR) epilayers with a total thickness of ~16 μm on CdTe/Si substrates.

Photolithography was performed on four 10 mm x 10 mm samples with a positive photoresist SPR 1818. A variable area device mask with mesa dimensions in the range 40 μm -300 μm was used to fabricate the latent patterns in the photoresist with a MJB-3 mask aligner. A second set of five samples was patterned with a 128 x 128 pixel array to open windows in the photoresist to evaluate the ICP etch process on small pixel arrays. Vias replicating 10 μm x 10 μm on a 25 μm pitch were developed in the photoresist for the array samples. The delineation of deep square trenches will be suitable for two color detectors, which have been previously reported with wet etch processing[13]. Tencor stylus profilometer was used to record the thickness of the photoresist before the etch process. Various sets of process parameters, $CH_4/Ar/H_2$ gas flow, chamber pressure, RF power and ICP power, were used to sample the data from the etch process. These process conditions were designed to evaluate the etch rate, etch depth, the sidewall profile and the etch uniformity on the samples. A combination of $CH_4/Ar/H_2$ etch chemistry was used for the study of etching on mesa device samples. The mesa device samples were characterized with the photoresist mask left on the samples after the etch process to characterize the selectivity of the process. Surface roughness measurements were performed on mesa device samples with a Veeco digital instruments atomic force microscope (AFM). A summary of the ICP etch process parameters used for the variable area mesa device samples is given in Table1.

	Ar (sccm)	CH_4 (sccm)	H_2 (sccm)	ICP power (watts)	RF power (watts)	Chamber pressure (mTorr)
Sample 1	30	15	0	750	75	20
Sample 2	0	15	0	750	75	20
Sample 3	30	15	20	750	75	20
Sample 4	30	50	15	750	100	25

Table 1: ICP etch process conditions for variable area mesa device samples

The surface roughness of HgCdTe has been shown to be higher with the use of H_2 in the etch chemistry[14]. We explored the possibility of using only CH_4/Ar chemistry to etch HgCdTe on the array samples. Smooth sidewalls and etched surfaces are required to achieve good passivation and minimize recombination processes in devices[15]. The array samples were subjected to an oxygen plasma to clean the photoresist on the surface following the etch process. Plan view and angular view scanning electron microscopy (SEM) measurements were performed on all the samples with a

[13] W.E. Tennant, M. Thomas, L.J. Kozlowski, W.V. Mclevige, D.D. Edwall, M. Zandian, K. Spariosu, G. Hilderbrandt,and V. Gil, J. Electron. Mater., 30, 6, 590 (2001)
[14] J. Pilkington, L. Hipwood, R. Catchpole and M. Ordish, 1st EMRS DTC Technical Conference, B11 (2004).
[15] E.P.G. Smith, G.M. Venzor, P.M. Goetz, J.B. Varesi, L.T.Pham, E.A. Patten, W.A. Radford, S.M. Johnson, A.J. Stoltz, J.D. Bensen, and J.H. Dinan, J. Electron. Mat., **32**, 821.(2003).

Hitachi S-3000N scanning electron microscope. The ICP etch process conditions used for the array samples are presented in Table 2.

	Ar (sccm)	CH_4 (sccm)	H_2 (sccm)	ICP power (watts)	RF power (watts)	Chamber pressure (mTorr)
Array sample1	20	5	0	1000	25	5
Array sample 2	10	5	0	1000	25	5
Array sample 3	20	10	0	1000	25	5
Array sample 4	15	12	0	1000	30	5
Array sample 5	30	15	0	1000	30	5

Table 2: ICP etch process conditions used for the 128 x 128 array samples

3. RESULTS AND DISCUSSION

Figure 1 shows angular view SEM images of the mesa device samples etched with the conditions listed in Table 1.

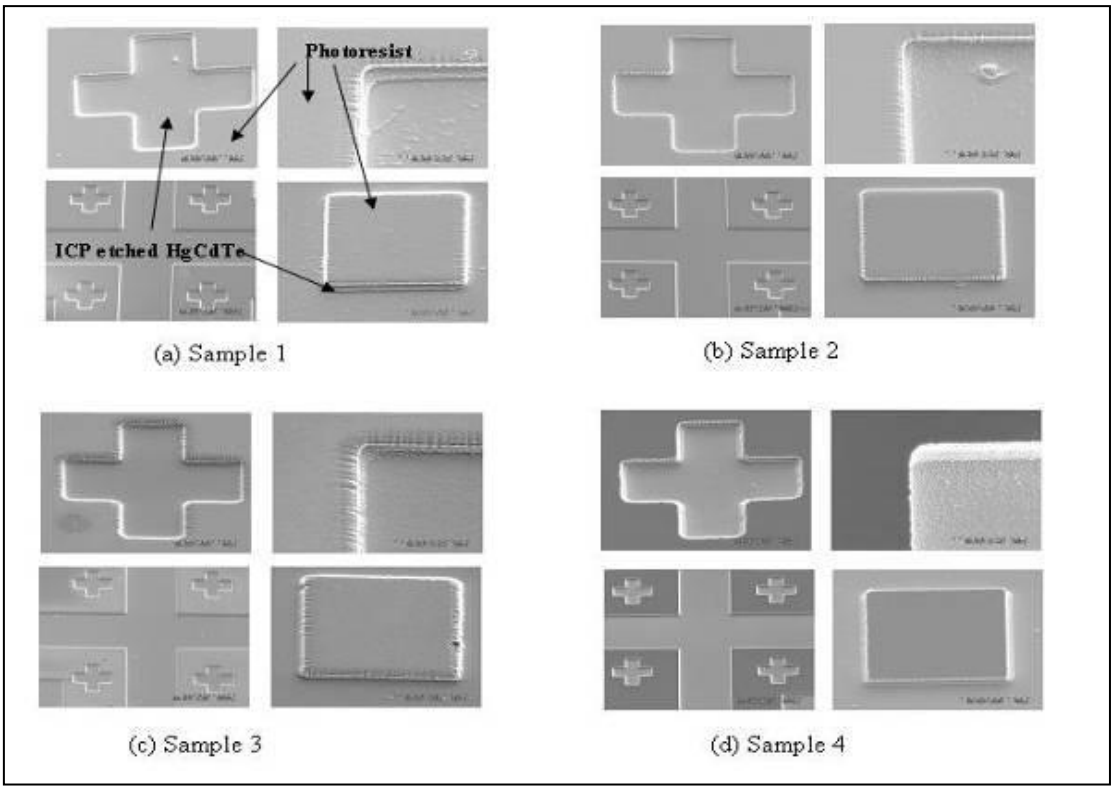
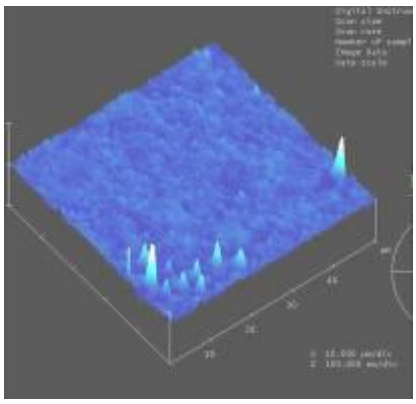
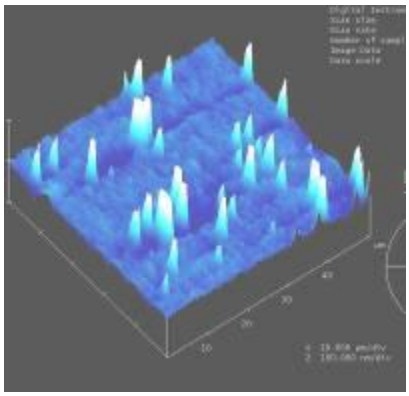


Figure 1: Angular view SEM images of mesa device samples etched with ICP

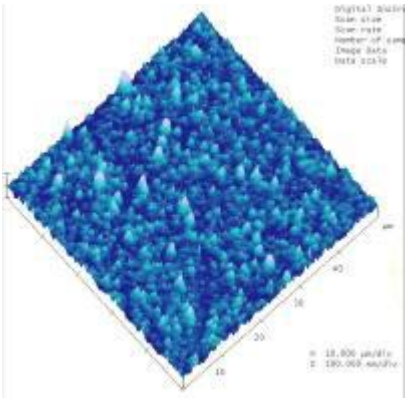
The align keys and a mesa defined with the ICP etch are shown for each sample in Figure 1. The lateral dimensions of the align keys are 200 μm while the mesa dimensions are 40 μm x 40 μm .The mesa device samples showed distinct etch rates of 0.46, 0.8, 0.76 and 0.72 μm/min respectively for the four samples. The etch depth for the samples were recorded between 4.6 μm-5.8 μm respectively. All the four processes resulted in etching HgCdTe with the retention of the mask features but the contrast difference from the SEM images indicate that the degree of selectivity is higher for the sample 4. High CH_4 flow combined with a high RF power generate a high density of methyl radicals and also impart high kinetic energy for ion bombardment, which results in a higher selectivity for this process. It can also be seen that the integrity of the photoresist is higher during this etch process. AFM measurements show surface roughness value of 3.2 nm on sample 4 while values of 3.9nm, 5.6nm and 18.7nm were recorded for samples 1, 3 and 2, respectively. AFM images of the four samples are shown in Figure 2.



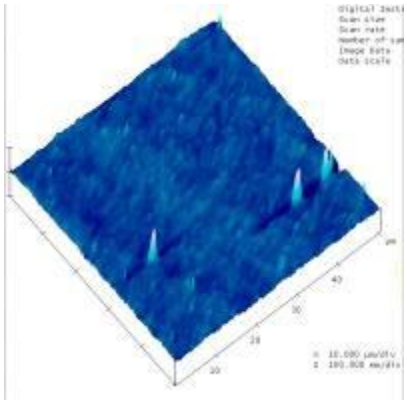
Sample 1



Sample 2



Sample 3



Sample 4

Figure 2: AFM images of mesa device samples etched with ICP

It is possible that the high surface roughness of the sample 3 is attributed to the higher concentration of H_2 used in the etch process, which probably created active atomic hydrogen species that increased ion bombardment, leading to a rough surface as evident in the AFM image of Figure 2. The plasma etch process for HgCdTe can therefore be modified by limiting the use of H_2 as a source gas in the chemistry.

Figure 3 shows optical microscope images of the 128 x 128 format array developed in the photoresist on MWIR HgCdTe samples.

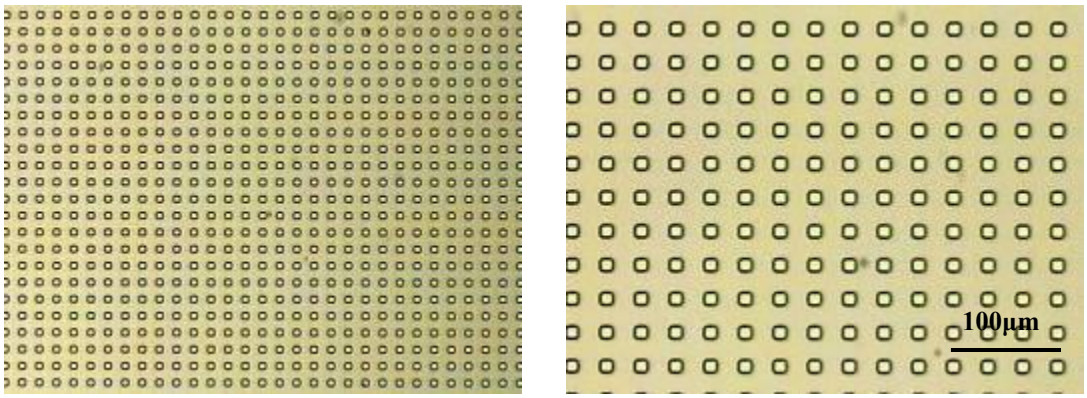


Figure 3: Optical microscope images of 128 x 128 format array vias on HgCdTe samples after lithography

The thickness of the photoresist measured on the samples before the etch process as measured by the stylus profilometer was ~2.02 µm. The array samples were etched purely with the CH_4/Ar chemistry to explore the possibility of obtaining smooth sidewalls and surface morphology. Figure 4 shows plan view and angular view SEM images of array sample 1 etched with the ICP conditions listed in Table 2. The sample was cleaned with oxygen plasma after the ICP etch process, but a thin residue of the photoresist is seen at the edges of the vias and on the surfaces between the vias on the sample. The etch depth of the vias on the sample is ~2.8 µm and the etch rate was evaluated to ~0.288 µm/min. A DC bias of ~-67 V was recorded for the process conditions used on this ample. Such a low DC bias will probably generate a shallow ion angular distribution in the plasma that gives rise to the lateral resist erosion[16], as is evident in the corners of the vias.

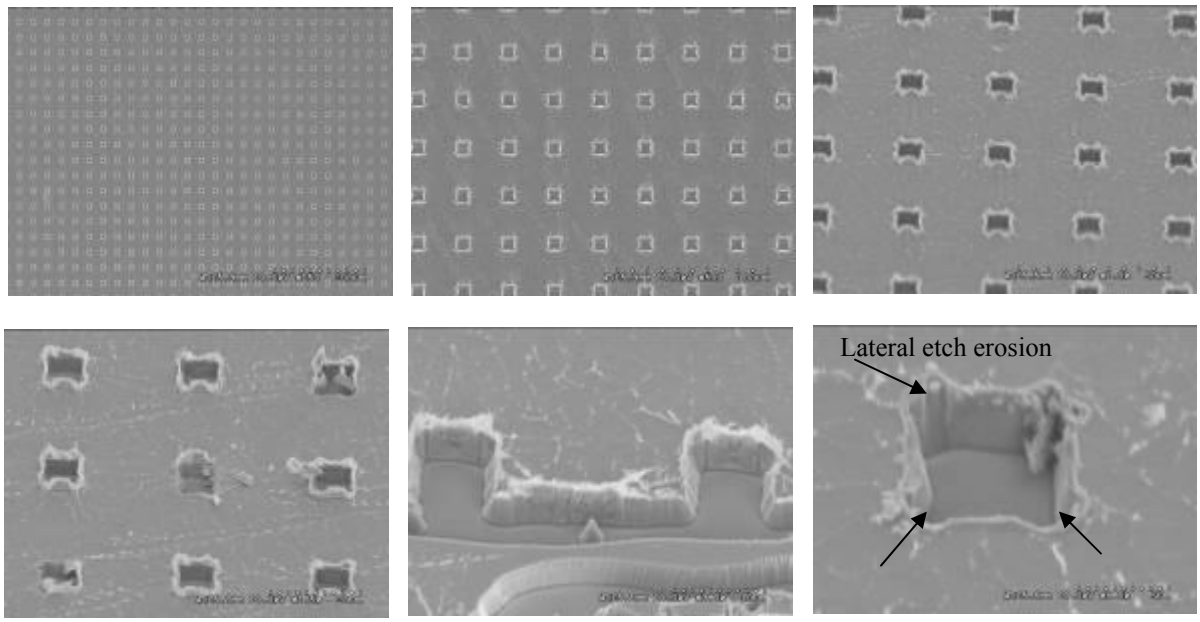


Figure 4: Plan view and angular view SEM images of array sample 1 etched 2.8 µm deep with ICP

[16] J.D. Benson, A.J. Stoltz, A.W. Kalaczyec, M. Martinka, L.A. Almeida, P.R. Boyd, and J.H. Dinan, J. Electron. Mater., 31, 822 (2002).

The angular view SEM images show smooth sidewalls and etched surfaces. Figure 5 shows plan view and angular view SEM images of array sample 2 etched with ICP conditions listed in Table 2. Photoresist residue on this sample is low compared to the array sample 1 after the oxygen plasma cleaning. This is due to the reduction of the Ar concentration in the etch process. Photoresist usually hardens with high energy Ar ion bombardment. Also, a reduction in the lateral resist erosion can be seen from the angular view SEM images. An etch depth of 2.167 μm is obtained on this sample at an etch rate of 0.197 μm/min.

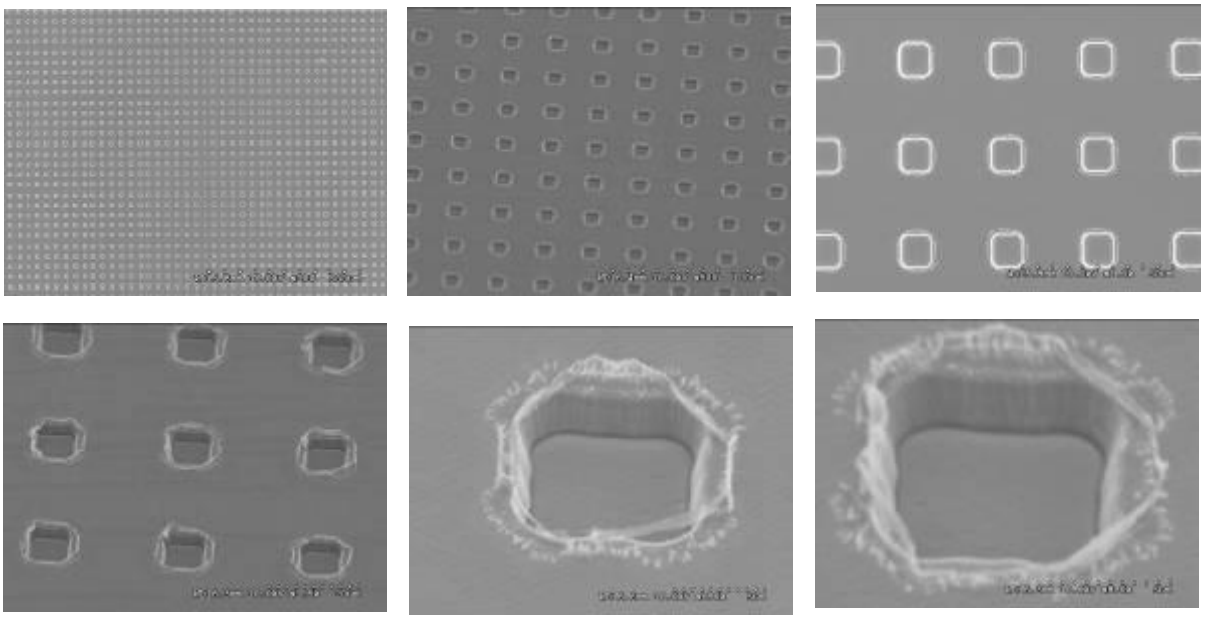


Figure 5: Plan view and angular view SEM images of array sample 2 etched 2.1 μm deep with ICP

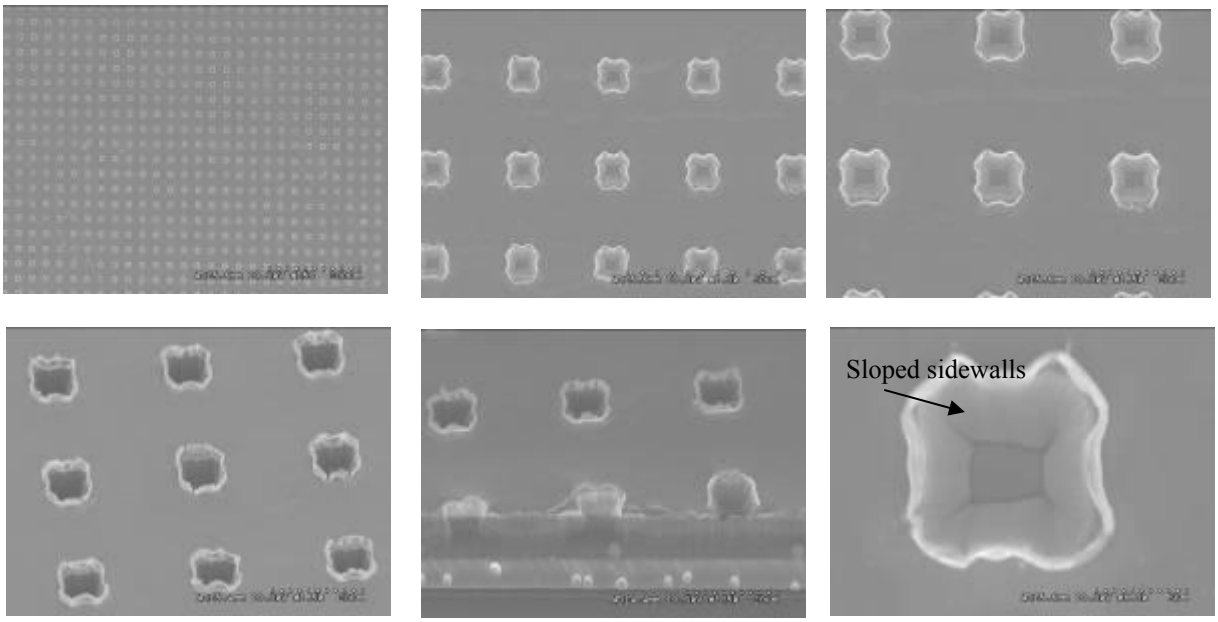


Figure 6: Plan view and angular view SEM images of array sample 3 etched 4 μm deep with ICP

Figure 6 shows plan view and angular view SEM images of array sample 3 etched with the ICP conditions listed in Table 2. Sloped sidewalls were obtained when the Ar flow, CH_4 and the RF power were increased for this sample. The ion angular distribution is higher in this case due to the large number of collisions in the plasma with the addition of CH_3 radicals and the Ar ions. An etch depth of ~4.04 μm was measured on this sample and the etch rate evaluated to 0.202 μm/min.

Figure 7 shows the SEM images of the array sample 4 etched with the ICP conditions listed in Table 2. We observed that the slope of the sidewalls is reduced by increasing the CH_4 gas flow. Photoresist residue on this sample is also reduced significantly due to the reduced Ar concentration. An etch depth of 5.51 μm was measured by the step profilometer and the etch rate calculated was 0.551 μm/min.

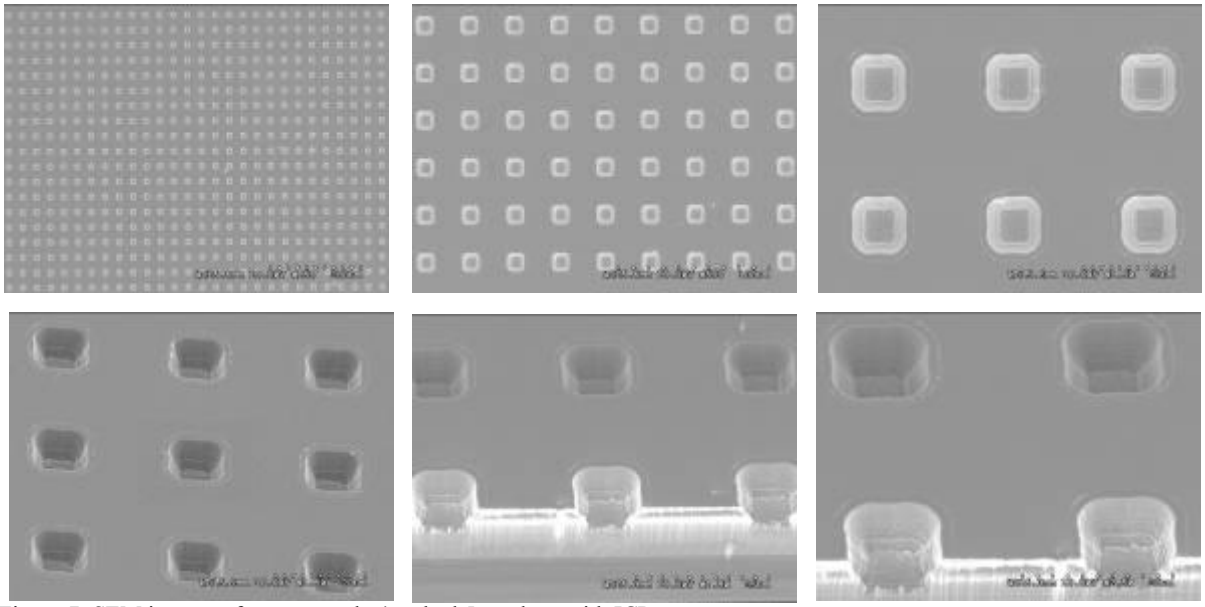


Figure 7: SEM images of array sample 4 etched 5μm deep with ICP

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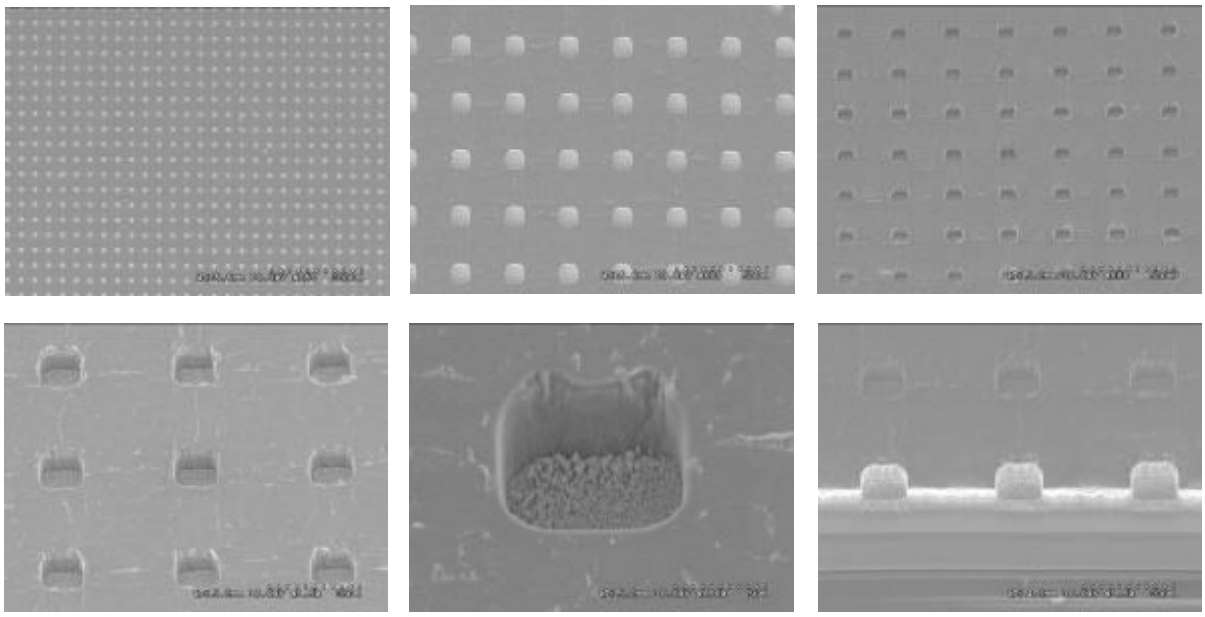


Figure 8: SEM images of array sample 5 etched 4.9μm deep with ICP.

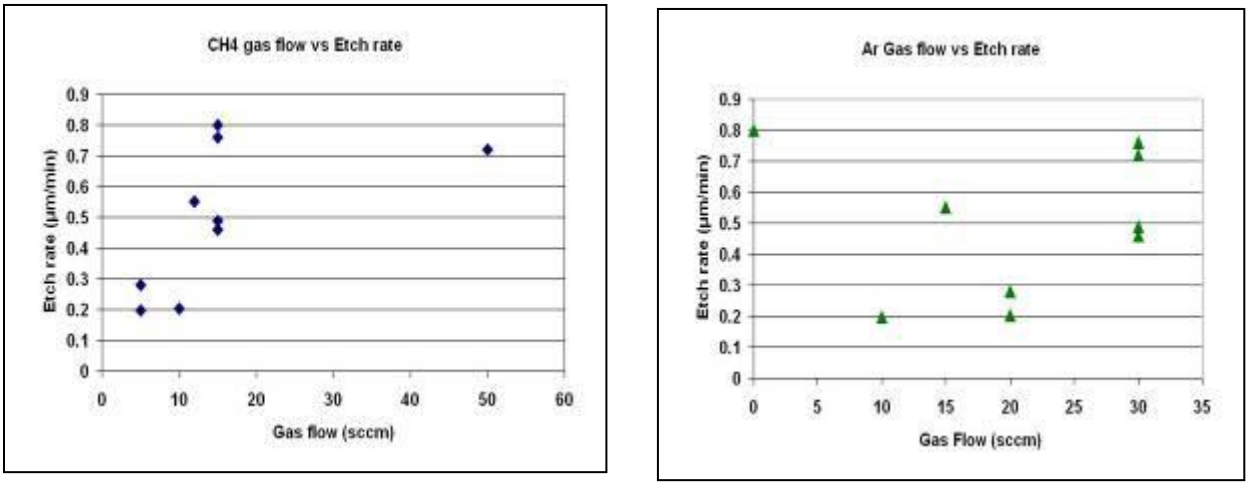
Further increase in CH_4 gas flow with constant RF power and higher Ar gas flow resulted in abrupt sidewalls on array sample 5. SEM images of this sample are shown in Figure 8. An etch depth of 4.9 μm was measured by the stylus profilometer and the etch rate was calculated to 0.491 μm/min.

A summary of the ICP etch results and the corresponding descriptive statistics of the array samples is given in Table 3.

	Etch depth	Etch rate	Standard deviation of etch depth over the sample	Sidewall profile
Array sample 1	2.8 μm	0.288 μm/min	0.0636 μm	Smooth/etch lag
Array sample 2	2.167 μm	0.197 μm/min	0.2406 μm	Smooth/etch lag
Array sample 3	4.04 μm	0.202 μm/min	0.1091 μm	Smooth/sloped
Array sample 4	5.51 μm	0.551 μm/min	0.0796 μm	Smooth/sloped
Array sample 5	4.9 μm	0.491 μm/min	0.0824 μm	Smooth/abrupt

Table 3: ICP etch process results on HgCdTe array samples

The uniformity of the etch process over the array samples was statistically evaluated from the etch depth over several vias on each sample. The standard deviation values listed in Table 3 illustrate a high degree of etch uniformity achieved over the 128 x 128 array format samples. Such a degree of uniformity cannot be achieved with the isotropic wet etching process. Precise control of etch rate, surface morphology and preservation of physical and electrical properties of HgCdTe material are of primary importance for transition to a device manufacturing technology. We have further analyzed the etch rate of HgCdTe with the various process parameters: CH_4 gas flow, Ar gas flow, RF power and chamber pressure.



a. b.

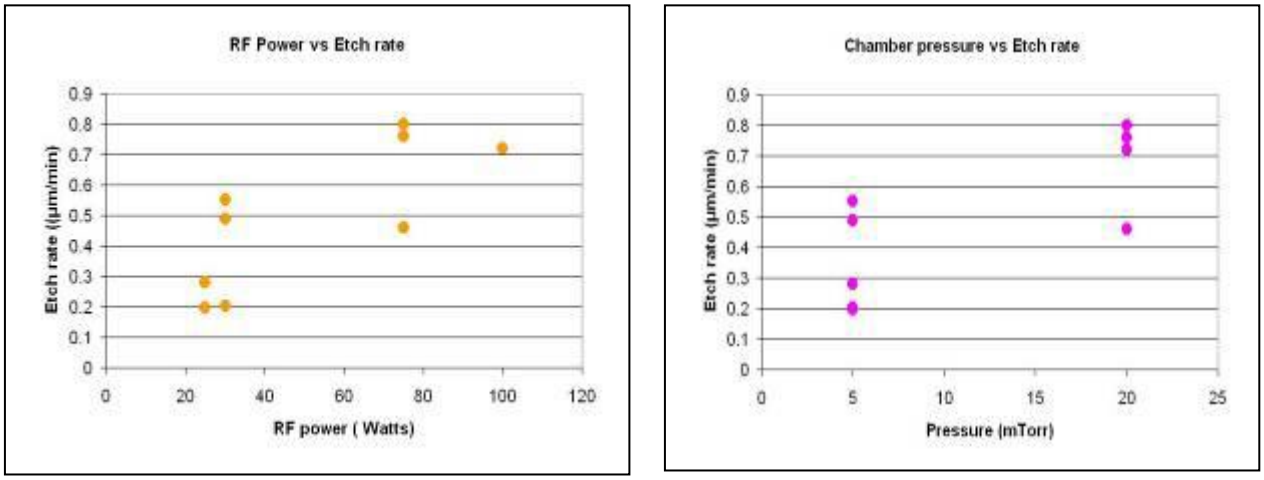
Figure 9: (a) Etch rate as a function of CH_4 gas flow; RF power ~25 -100 W; ICP power~750 -1000 W, chamber pressure 5-20 mT, (b) Etch rate as a function of Ar gas flow; RF power ~25-100 W; ICP power ~750-1000 W, chamber pressure 5-20 mT

Figure 9 (a) shows the etch rate of HgCdTe as a function of the CH_4 gas flow. It can be seen that the etch rate increases with the increase in the CH_4 flow rate. This is in agreement with the previously reported results [10] that conclude that an

increase in the CH_4 increases the etch radicals CH_3 that are critical for etching HgCdTe. However, a high etch rate of HgCdTe is observed to be a tradeoff with the surface roughness due to the low damage threshold of the material. The data presented in this report suggests that an etch rate below or close to ~0.5 μm/min would result in a good surface morphology and a precise control over the etch process to fabricate abrupt sidewalls.

The etch rate plotted as a function of Ar gas flow in Figure 9 (b) shows a similar trend of high etch rate at high gas flow rate with the exception that a high etch rate is also obtained with zero Ar flow. However, this does result in a rough etched surface, as observed in AFM data. An increase in the CH_4/Ar ratio from 50% to 80% resulted in sloped sidewalls (array sample 3) but the same 50% gas ratio with a higher RF power resulted in abrupt sidewalls (array sample 5). These process conditions can be optimized to fabricate high-density vias for eliminating cross talk between pixels and also for fabricating mesas with sloped sidewalls that facilitate a conformal sidewall passivation.

The etch rate of HgCdTe as a function of RF power and chamber pressure is analyzed from the plots shown in Figure 10 (a) and (b).



a. b.

Figure 10: (a) Etch rate as a function of RF power; CH_4 ~ 5-50 sccm, Ar ~0-30 sccm, ICP power ~750-1000 W, (b) Etch rate as a function of chamber pressure; CH_4 ~ 5-50 sccm, Ar ~0-30 sccm, ICP power ~750-1000 W

Increasing the RF power to the wafer electrode in the ICP chamber increases the DC bias in the plasma, which imparts higher kinetic energy to the ions. This translates into a higher etch rate for higher RF power, as shown in Figure 10 (a). Increasing the RF power also increases the selectivity of the etch process, resulting in abrupt sidewalls. However, very high RF power can lead to increased surface roughness of the sidewalls and the etched surface, which reduces the device carrier lifetimes due to high surface recombination at the rough surfaces.

Figure 10 (b) shows the etch rate as a function of chamber pressure. Increasing the chamber pressure increases the density of ionized species in the plasma and hence results in an increased etch rate. A higher density of ions in the plasma results in a larger number of collisions with the atoms and this reduces the directionality of the etch process and a loss of selectivity. A high degree of selectivity was achieved in etching vias 5 μm deep on array format samples.

4. SUMMARY AND CONCLUSIONS

ICP etching of HgCdTe was performed on types of samples: (a) variable area mesa device samples for delineating mesas for single element detectors, and (b) 128 x128 format arrays for fabricating deep vias to realize two color detectors and eliminate cross talk. CH_4/Ar/H_2 chemistry was used for the mesa device samples while purely CH_4/Ar-based chemistry was applied to the array format samples for the first time to our knowledge. Distinct etch rates and surface roughness values were obtained on the mesa device samples that suggest that the use of H_2 in the etch process may not be favorable

for etching smooth sidewalls in HgCdTe devices. Abrupt sidewalls with smooth surfaces were obtained with low etch rates on the vias etched in the array format samples. Etch depth variation with a standard deviation as low as 0.06 was achieved on the array samples, which indicates a high degree of uniformity with the ICP etch process. Etch conditions required to control the slope of the sidewalls have been suggested.

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