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CERAMIC VIA WAFER-LEVEL PACKAGING FOR MEMS

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ABSTRACT

We will present a novel approach to wafer level packaging for micro-electro-mechanical systems. Like most common MEMS packaging methods today, our approach utilizes a wafer bonding process between a cap wafer and a MEMS device wafer. However, unlike the common methods that use a silicon or glass cap wafer, our approach uses a ceramic wafer with built-in metal-filled vias, that has the same size and shape as a standard 150 mm silicon wafer. This ceramic via wafer packaging method is much less complex than existing methods, since it provides hermetic encapsulation and electrical interconnection of the MEMS devices, as well as a solderable interface on the outside of the package for board-level interconnection. We have demonstrated successful ceramic via wafer-level packaging of MEMS switches using eutectic gold-tin solder as well as tin-silver-copper solder combined with gold thermo-compression bonding. In this paper, we will present the ceramic via MEMS package architecture and discuss the associated bonding and assembly processes.

INTRODUCTION

Micro-electro-mechanical systems (MEMS) have become widespread in many industries, from micromirrors for video projectors to accelerometers and gyroscopes for automotive inertial sensing systems. However, despite much research and development in radio-frequency (RF) MEMS devices such as switches, filters, and variable capacitors, there is still a significant untapped opportunity for MEMS in the wireless communications market. With one noteable exception (the film bulk acoustic resonator (FBAR) duplexer) RF MEMS have yet to penetrate this highly cost-sensitive market. One of the key reasons for this is the high cost of MEMS packaging, which can account for up to 80% of the final product cost [1].

MEMS devices such as RF switches require wafer level packaging (WLP) for several reasons. First and foremost, the existence of microscopic moving parts on the wafer requires them to be encapsulated prior to dicing, because water and particles created during the sawing process would destroy the MEMS devices. Therefore packaging is best done at the wafer level, immediately after the moving components are "released" (i.e. made free to move by dissolving a sacrificial thin-film material). Second, cost is typically reduced compared to die-level packaging, where the die must be released and packaged individually. Third, cleanliness and yield are generally improved compared to die-level packaging, where the dice must be handled with the MEMS devices exposed. Fourth, MEMS WLP's are typically very small, since they are essentially a chip-scale package (CSP); this is especially important for the wireless communications market where small form factors are required.

MEMS packaging can be broken down into a hierarchy of levels. The *zero-level* typically refers to the initial encapsulation of the MEMS devices on the wafer or die. The zero-level package is typically assembled into a *first-level* package, which provides electrical and mechanical connections that are compatible with surface-mount technology (SMT). The *second-level* packaging refers to the actual surface-mounting or soldering of the first-level package to a PC board, and the *third-level* is the final packaging of the product [1].

The term "wafer-level packaging" is commonly used differently between to the MEMS industry and the IC industry. In the IC industry, a WLP technology typically provides interconnect and encapsulation functions at both the zero- and first-level. The resulting dice, by definition, can be soldered to a board using surface-mount technology. In contrast, the MEMS industry typically refers to any wafer-level encapsulation technology as a WLP, without regard for electrical interconnection or the first level of packaging. For example, if a MEMS device is capped using a silicon wafer bonding technique, it is referred to as wafer-level packaging, even if the resulting die must subsequently be assembled and wirebonded into an additional package at substantial cost. Ideally, a true MEMS WLP would provide not only the zero-level encapsulation, but also the electrical interconnect to make the device compatible with surface mount soldering technology. Simply put, the rationale behind the ceramic via wafer bonding technology is to provide a true surface-mountable wafer-level MEMS package in a single wafer-bonding step.

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NOMENCLATURE

MEMS Wafer-level packaging (WLP): any packaging method in which the MEMS are encapsulated prior to singulating the wafer.

MEMS Wafer-scale packaging (WSP): a subset of WLP in which all the MEMS devices on an entire MEMS wafer are packaged simultaneously, such as by wafer bonding.

Package interface layer (PIL): The material that serves as the bonding medium between the cap or lid and the MEMS wafer.

Surface mount technology (SMT): standard technology for soldering packaged dice to a board

BACKGROUND

There are many zero-level MEMS WLP architectures, which can be classified according to three aspects: the lid or cap wafer material, the bonding and sealing material (package interface layer, or PIL), and the feedthrough configuration.

Many options for the lid material can be considered for hermetic wafer-level MEMS packaging. Metal lids, while used extensively for die-level MEMS packages, present two main difficulties at the wafer-level: (1) high coefficient of thermal expansion (CTE) mismatch between the metal and the silicon (metals typically expand around 10-20 ppm/°C), and (2) limited applicability to the vertical feedthrough architecture, as this would require a method of making isolated vias in the lid or vertical feedthroughs through the MEMS wafer itself. Ceramics lids can be fabricated with well-established LTCC (low-temperature cofired ceramic) or HTCC (high-temperature cofired ceramic) technologies that enable integration of metal through-vias and redistribution layers. One challenge to applying ceramics for wafer-scale bonding is in reducing the CTE of the ceramic material such that it can be reliably bonded to silicon at the wafer scale. Typical CTE values of ceramics range from 7-9 ppm/°C for HTCC to 5-7 ppm/°C for LTCC, compared to 2.6 ppm/°C for silicon. In addition, there are significant although not insurmountable challenges in manufacturing 6" ceramic wafers with acceptable dimensional tolerance control. Certain borosilicate glasses, such as Pyrex 7740 (Corning) or Borofloat (Schott AG) are formulated to approach the thermal expansion rate of silicon, and thus are widely used for wafer-to-wafer bonding (often using anodic bonding). Unlike LTCC, Pyrex glass is readily available in 6" wafer form, has no dimensional control problems related to shrinkage, and has a relatively low CTE of only 3.2 ppm/°C. On the other hand, the main challenge is that there is no well-established inexpensive method for making metal-filled vias. For packages with very thin lids and stringent leak-rate requirements, gas permeation through the thin glass lid may be of concern. Polymers in general are highly permeable to gases, and therefore are not considered for hermetic packaging. However, liquid-crystalline polymers (LCP's) with moisture and oxygen permeability approaching that of glass are receiving increasing attention as near-hermetic alternatives [2].

There is a wide variety of sealing and bonding materials for WLP (also referred to the package interface layer, or PIL), which fall broadly into 3 families, as shown in Table 1. Surface bonding techniques, such as anodic bonding, fusion bonding, and activated-surface bonding generally form strong, hermetic seals, but they cannot bond metals, and they require wafers that are polished smooth. Metallic interlayer techniques include solder bonding, thermocompression bonding, and eutectic bonding. Solder bonding is very common in the MEMS industry, but only fluxless solders such as gold-tin (80%Au/20%Sn) can be used, since the presence of any liquid would typically destroy the MEMS device. Thermo-compression bonding (TCB), using thick electroplated gold, is also common. Au-Si eutectic bonding is common in the MEMS community, but it too also requires fairly smooth surfaces. Insulating interlayer bonding can be divided into glass frits and polymers. Glass frit is a common hermetic seal ring material that can achieve sealing by heating to around 350-450°C. However, since it is deposited by screen printing, it is challenging to achieve narrow line widths. There are also countless adhesives that can and have been used for wafer bonding, but they are generally not considered hermetic [3].

Table 1. Wafer bonding methods.

Bonding method		Advantages	Drawbacks
Surface-bonding	Anodic	Hermetic, strong	High voltage, very smooth surface req'd
	Fusion (direct)	Hermetic, strong	High temp (>800°C), smooth surface req'd
	Plasma-activated	Hermetic, low temperature	Very smooth surface required
Metallic bonding	Solder	Can seal to rough, high-topography surfaces; hermetic, low temperature	"Wicking" is possible
	Thermo-compression	Can seal to rough surfaces; hermetic, low temperature, small feature size	High force required
	Eutectic	Hermetic, strong	High temp (>363°C); smooth surface req'd
Insulator bonding	Glass frit	Can seal to rough, high-topography surfaces; hermetic, low temperature	Large feature size due to screen printing; organic content
	Polymers	Various	Less hermetic; organic content

For any wafer-level MEMS package, a feedthrough configuration for routing the signal from the device to the outside must be decided. There are essentially two types of feedthroughs: lateral and vertical, as shown in Fig. 1. Lateral feedthroughs are routed on the wafer surface beneath the seal ring from the MEMS device to the outside (Fig. 1a). MEMS packages utilizing such lateral feedthrough architectures are typically wirebonded to a first-level package. Many companies, including Analog Devices [4], Motorola [5], and Bosch [6] currently use this configuration with a glass frit seal ring material to package inertial sensors (accelerometers and gyroscopes). Vertical feedthroughs on the other hand, route the signal vertically through the lid to the outside (Fig. 1b). In such cases, it is logical to use a metal PIL material for both the electrical contacts and the seal ring. This approach is used by Agilent for the FBAR duplexer [7]. One advantage of vertical (rather than lateral) feedthroughs is that they generally reduce the die and package area, since large pads for wirebonding or soldering are made on the outside of the lid rather than on the silicon die itself. A second key advantage of vertical feedthroughs is that there is a potential for eliminating the first-level package, if the bondpads are made SMT-compatible.

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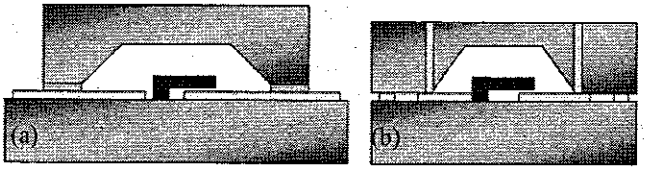

Figure 1. Feedthrough architectures for MEMS packages: (a) lateral feedthroughs (b) vertical feedthroughs (vias).

In order to make a wafer-scale package that is truly wafer scale at both the zero-level and the first-level, the lid material, PIL material, and feedthrough configuration must be chosen such that the final packaged device is surface mountable. Most commercially available MEMS are only truly "wafer-scale" at the zero-level—after singulation, they must be must be mechanically and electrically connected to a first-level package in order to make them compatible with surface mounting.

To achieve this end, a ceramic lid material with vertical feedthroughs was chosen, since ceramics with metal-filled vias and Ni-Au solder pads have long been used as surface-mountable package substrates. However, to our knowledge, ceramics have not been used in a large-format silicon wafer-bonding paradigm. The package interface layer, or PIL, must be hermetic, it must withstand the surface mount temperatures (up to 260°C), it must be electrically conductive to connect the MEMS devices to the metal-filled vias, and it must be fluxless to prevent contamination of the mechanical components. Gold-tin solder was therefore the primary choice for this application.

EXPERIMENTAL

Ceramic via lids

Significant ceramic technology development was required in order to make 150 mm ceramic via wafers with accurate dimensional control and sufficiently low CTE to be suitable for wafer bonding to silicon. Therefore, individual die-sized ceramic via "lids" were first used to validate the approach, and the concept was later scaled up to full 150 mm wafers. The ceramic via lids were made using an LTCC or HTCC material (NTK and Kyocera). The lids were 2.9×4.0 mm², with 300 μm thickness, a 150 μm wide seal ring, and metal-filled vias with 200 μm diameter bondpads. The PIL material was a lead-free, fluxless Sn/Ag (96.5/3.5%) solder, with a melting temperature of 223°C. On the MEMS wafer, the seal rings and bondpads were patterned with 6 μm of electroplated gold. The ceramic via lids used a "hybrid" structure in which solder was used for the seal rings and gold stud bumps were made on the MEMS wafer to form the electrical connection to the vias. A schematic of this configuration is shown in Fig. 2.

This hybrid configuration was used for several reasons. First, using solder for the bondpads as well as the seal ring was found to result in significant "wicking", or solder flow along the metal traces on the MEMS wafer, which will be discussed later (Fig. 10). Second, the gold bumps acted as a standoff to maintain the gap between the ceramic cap and the MEMS wafer. Third, and most importantly, this process permitted the final sealing of the lid to be done in a wafer bonder, separately from the initial attachment in the pick-and-place tool. Sealing the MEMS devices in an enclosed chamber was necessary to allow stringent control over the composition and pressure of the environment inside the package.

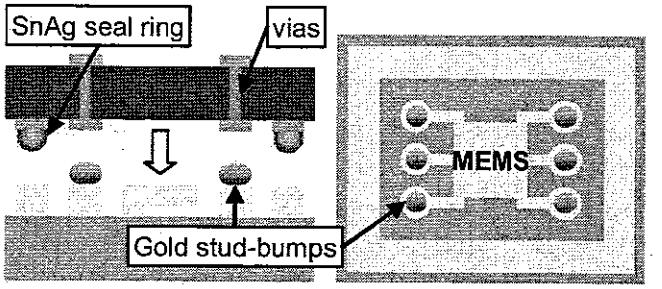

Figure 2. Schematic of a ceramic via lid with a solder seal ring and vertical feedthroughs. In this "hybrid" configuration, gold stud bumps were used for the bondpad interconnection instead of solder.

The process for assembling the hybrid ceramic via packages was as follows. First, gold stud bumps were made on the MEMS wafer, with a height slightly larger than the thickness of the solder seal ring (Palomar Technologies, Vista, CA). The ceramic via lids were then thermosonically bonded to the gold stud bumps using a pick-and-place tool (Palomar Technologies). This was done at a low temperature to prevent the solder from reflowing, which would seal an unsuitable environment inside the package. With the lids attached but not reflowed, the wafers were then placed in a wafer bonder (Suss MicroTec SB6e), which was evacuated and pressurized with dry nitrogen. The lids were then sealed to the MEMS wafer by applying a force of 1 kg per lid and heating to 230°C to reflow the solder seal ring.

Ceramic via wafers

For this approach, 150 mm LTCC wafers with silver-filled vias were obtained (Nikko Co., Hakusan city, Japan). These ceramic via wafers were 300-500 μm thick, and had coefficients of thermal expansion (CTE) ranging from 5.5 ppm/°C to as low as 3.4 ppm/°C. A stencil-printed eutectic Au/Sn (80%/20%) solder PIL material was deposited on both the bondpads and the seal rings. The hybrid PIL used for the ceramic via lids was found to be unnecessary for the ceramic via wafer approach, because the solder was less prone to wicking. A schematic of the ceramic via wafers is shown in Fig. 3. Figure 4 contains a cross-sectional SEM image of the ceramic via wafer, showing the Ag via and the Au/Sn solder. During the manufacture of the ceramic wafers, the AuSn was reflowed and planarized by a grinding process.

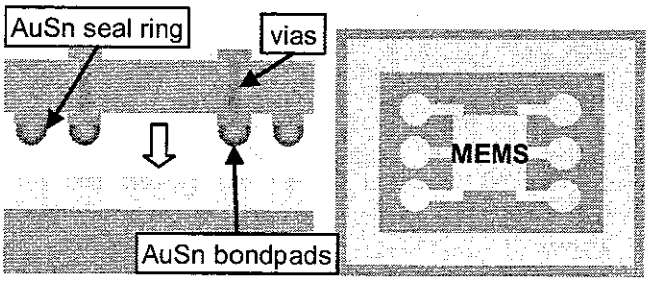

Figure 3. Schematic of the ceramic via wafer package.

Bonding of the ceramic via wafers to the MEMS wafers was carried out in a single step using the wafer bonder (Suss MicroTec SB6e). There are multiple challenges involved with this step, including thermal-expansion-induced misalignment

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and stress. The methods used to address these issues are discussed elsewhere [8]. The bonding process used a temperature of 300°C and a pressure of 400 kPa.

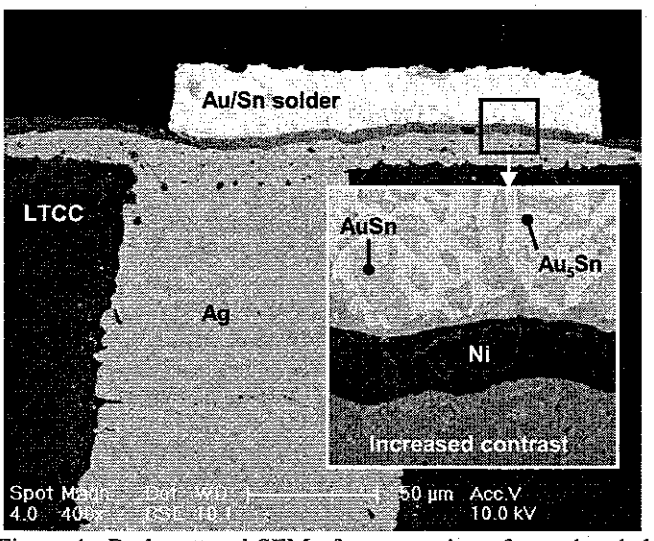

Figure 4. Backscattered SEM of cross section of an unbonded ceramic via wafer with Au/Sn solder. The inset represents a magnification of solder/pad interface with major phase compositions labeled (as interpreted from EDX data).

Assembly

Singulation of the ceramic via wafer level package was done using a wafer saw (Disco DFD 641). Board mounting was done by reflowing Sn(63%)/Pb(37%) ball grid array (BGA) solder spheres (Amtech Inc., Branford CT) directly to the bondpads on the ceramic via wafer. The package was then mounted directly onto an FR-4 board and reflowed.

RESULTS

Ceramic Via Lids

The ceramic via lids were bonded to MEMS switch wafers, as shown in Fig. 5. Figure 6 shows cross-sectional images of the joints formed between the ceramic via "hybrid" lid and the 6 µm gold features on the MEMS wafer. The seal ring joint between Sn/Ag solder and the MEMS Au is shown in Fig. 6a, and the bondpad joint between the Au stud bump and the bare bondpad is shown in Fig. 6b. It is interesting to note that the joint formed by the Sn/Ag solder consists primarily of two phases of Au/Sn, namely AuSn and $AuSn_2$. The silver precipitates out of solution to form distinct Ag crystals within the $AuSn_2$. The Au from the 6-µm gold pad is quickly absorbed by the solder during the bonding process. The presence of the Ag crystals is expected to be a reliability concern, as the crystal edges could serve as areas of stress concentration during reliability cycling. For higher reliability joints, a much thinner gold layer, preferably over a wettable yet low-diffusivity material (such as nickel) would be preferred.

The ultimate measure of package hermeticity for MEMS switches is the contact resistance, because the presence of any moisture or organics inside the package leads to significant contact degradation. The switches packaged using this approach exhibited a contact lifetime that was two orders of magnitude longer than that of unpackaged switches.

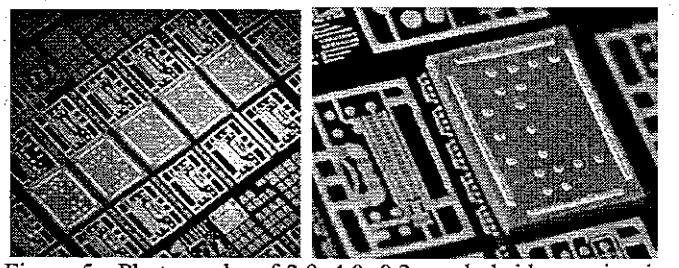

Figure 5. Photographs of 2.9×4.0×0.3 mm hybrid ceramic via lids bonded to a MEMS switch wafer, viewed from an angle. The bonding was done using a combination of gold stud bumps for the bondpads and Sn/Ag solder for the seal ring. Five packaged units are visible in the left photo, and the right photo shows one packaged die next to an unpackaged die.

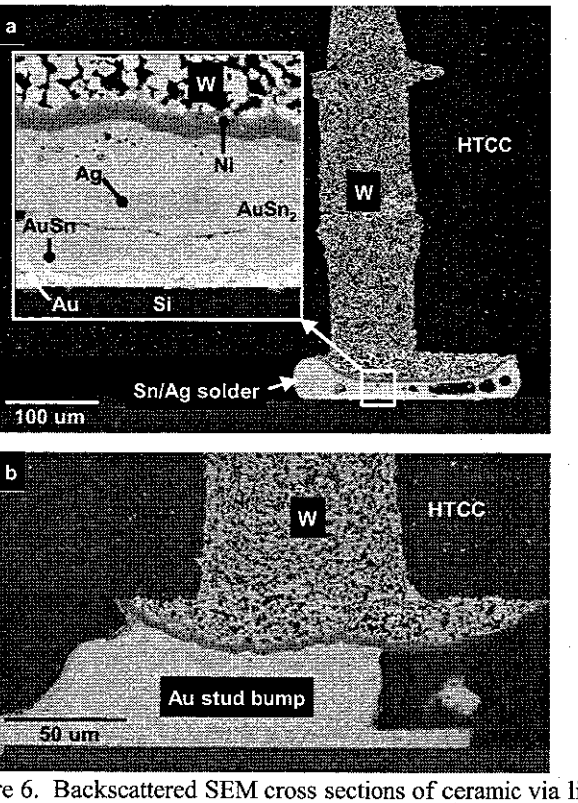

Figure 6. Backscattered SEM cross sections of ceramic via lids bonded to 6 µm thick gold pads on the MEMS wafer, showing the vias and bondpad joints. (a) The Sn/Ag seal ring; the inset shows a magnification of the joint with majority phase compositions labeled (as interpreted from EDX data). (b) The gold stud bump joint formed by thermosonic bonding followed by thermocompression bonding.

Ceramic via wafers

Successful wafer-scale bonding of ceramic via wafers to MEMS wafers was demonstrated, as shown in Fig. 7. Good results were obtained for ceramics with CTE's of up to 5.5 ppm/°C, although 4.0 and 3.4 ppm/°C ceramic wafers were more successful. The details of these bonding processes are discussed elsewhere [8]. As with the ceramic via lid package, the MEMS switches packaged by ceramic via wafer bonding exhibited a typical contact lifetime two orders of magnitude better than the unpackaged devices.

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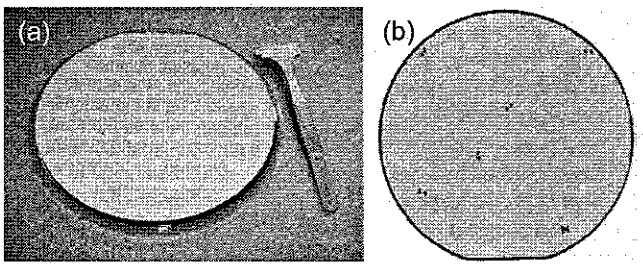

Figure 7. Photographs of MEMS wafers packaged by ceramic via wafer bonding: (a) 5.5 ppm/°C LTCC, and (b) 4.0 ppm/°C LTCC (the marks visible in the figure were for identification purposes only).

Assembly

Thermally-induced stresses can cause some curvature of the ceramic-silicon stack after bonding. This curvature can make the subsequent dicing process challenging. However, successful dicing of ceramic via wafer packages using 5.5 ppm/°C ceramic was demonstrated (Fig. 8), despite the presence of a small degree of curvature. Ceramic via packages with lower-CTE ceramic exhibited significantly less curvature, so singulating these wafers is not an issue.

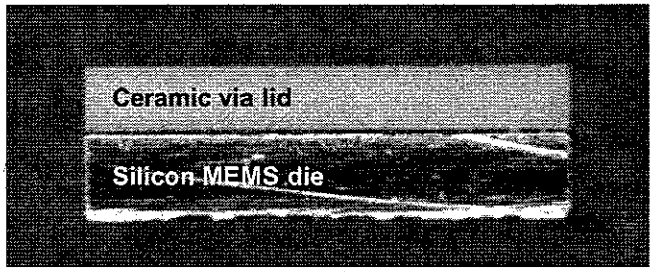

Figure 8. A side view of a ceramic via wafer packaged die, singulated using a wafer saw.

Once singulated, ceramic via wafer packages are very similar to standard surface-mountable devices. We have demonstrated successful surface-mounting of ceramic via packages to test boards using reflow of standard BGA balls. Figure 9 shows a ceramic via lid package with solder balls reflowed onto its external bondpads, prior to surface mounting to a board.

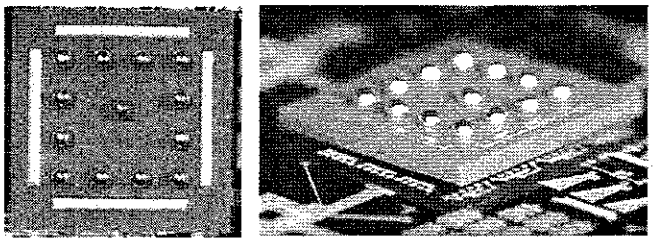
Figure 9. Straight and angled photographs of a ceramic via lid package with solder balls, taken prior to surface-mounting. 12-mil, Sn/Pb (63%/37%) solder balls were mounted onto 0.3 mm diameter pads coated with electroless Ni-Au.

DISCUSSION

For RF MEMS switches, ceramic via wafer packaging technology was pursued for various reasons, including cost, process complexity, hermeticity, size, and signal routing. The fundamental requirements were a vertical feedthrough configuration (using vias), wafer-scale packaging (*i.e.* wafer bonding), and a metallic PIL material. For MEMS switches in particular, excellent hermeticity is also a critical factor for contact lifetime.

A vertical feedthrough (via) configuration is preferable to a lateral feedthrough approach for most RF MEMS devices. Typically, these devices have very small die sizes (2×2 mm) and are targeted towards extremely cost-sensitive markets. A significant reduction in die size, and hence cost, can be achieved by using vias instead of lateral feedthroughs. This is based on the simple argument that vias allow the bondpads to be made on the lid instead of taking up additional area on the die. Furthermore, the via configuration also has a significant advantage with regard to the cost of assembly. In general, a MEMS package with lateral feedthroughs requires wirebonding to an intermediate substrate so it can be surface mounted to a board. This is because the bondpads are recessed below the level of the lid. In contrast, the vertical feedthrough packages shown here have Ni-Au bondpads on the top of the lid, and are fully compatible with surface mount assembly, without the need for an intermediate substrate.

For the ultimate in miniaturizability of the RF switch package, a metallic PIL is appropriate. Metals, unlike polymers and many glasses, offer the extremely low gas permeability that is required. Furthermore, metals are most compatible with the vertical feedthrough architecture. The Sn/Ag solder was implemented successfully as a PIL, but only when combined with gold stud bumping and thermosonic bonding to limit solder squeeze-out. Au/Sn was implemented successfully, although some degree of wicking and voiding was still observed with this material. Figure 10 compares the wicking and squeeze-out observed with Sn/Ag and Au/Sn solders. For the final packaged MEMS device to be entirely lead-free, the PIL material must also be able to withstand the lead-free surface-mounting temperature, which is in the range of 240-260°C. Au/Sn solder meets this requirement.

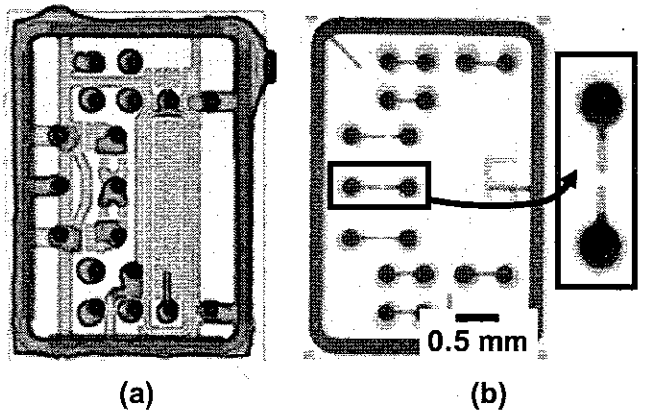

Figure 10. X-ray micrographs of bonds formed with (a) Sn/Ag/Cu solder and (b) Au/Sn solder. The solder is deposited on both the pads and the interconnect. The Sn/Ag/Cu squeezed out significantly more than the Au/Sn solder.

CONCLUSIONS & FUTURE DIRECTIONS

Packaging is one of the most critical factors in enabling high-volume commercialization of RF MEMS. In addition to

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the extremely cost-sensitive nature of the wireless market, RF MEMS switches also place very stringent requirements on the packaging, particularly with regard to hermeticity.

The ceramic via wafer packaging technology represents an attempt to significantly reduce the cost of MEMS wafer-level packaging. A through-via architecture was chosen because it enabled superior miniaturization of the die and package. A AuSn sealing material was chosen for several reasons, including hermeticity, electrical conductivity, and reflow temperature. Most importantly, the ceramic via wafer offers the ability to combine the zero-level and first-level packaging into a single wafer-bonding step, thus significantly reducing the complexity and cost of the assembled product.

We have demonstrated successful implementation of a ceramic via wafer-level packaging process, with the capability to package RF MEMS switches. In addition, we have shown that the package can be successfully diced and mounted onto a printed circuit board without the need for an additional level of packaging.

In the future, ceramic via wafer technology will benefit from continued reduction in CTE and dimensional control of the ceramic. The development of AuSn solder deposition techniques such as electroplating to allow very fine linewidths will be beneficial. In addition, extensive reliability testing must be done.

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