Applications of Plasma Enhanced Chemical Vapor Deposition in VLSI

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Applications of plasma enhanced chemical vapor deposition in microelectronics fabrication are discussed. Some of these applications are for the deposition of materials which have properties as good as or better than those of films deposited at higher temperatures by strictly thermal processes. Other applications described are those which serve as aids to lithography, etching, and other unit steps where films remaining on the processed wafers are removed. Relatively recent PECVD processes for the formation of new films with interesting potential applications are also reviewed.

CHEMICALLY REACTIVE, low-pressure glow discharge plasmas have been used to form a number of coating materials employed in the fabrication of microelectronic circuits. The key advantage of plasma-assisted reactions is that they can occur at temperatures that are usually considerably lower than are possible with thermal reactions alone. As a result it is possible to deposit or to grow films on substrates that do not have the thermal stability to accept such coatings at the higher temperatures required. This feature is important not only from the viewpoint of the deposition of passivating coatings over metal interconnects, but also because of the desire to limit such factors as diffusion or grain growth in devices having small feature sizes and shallow junctions. Where thermal reactions are allowed, additional advantages of plasma activation are that it can increase reaction rates substantially and produce films having unique compositions. The latter, of course, can also be a disadvantage since it may result in film contamination.

A number of in-depth reviews of the fundamental aspects of Plasma Enhanced Chemical Vapor Deposition (PECVD) are available [1-6]. Therefore, the emphasis here will be on a review of the application of PECVD materials in microelectronics fabrication processes.

Inorganic Dielectrics for Passivation

PECVD Silicon Nitride

Passivation of IC chips has undoubtedly been the most significant application for PECVD materials, and silicon nitride has been the film of choice. Its coverage of the underlying metal is conformal, it is acceptably low in pinholes for thicknesses greater than about 1000 Å, and it is a good barrier to moisture and sodium. The films are usually in compression and are thus less prone to delamination or cracking. Some typical properties of PECVD nitride compared to those of high temperature LPCVD nitride are listed in Table I.

SiN films of various compositions are deposited in plasma reactors of the parallel plate, radial gas flow type [8], shown in Fig. 1 or of the longitudinal, hot wall type [9] shown in Fig. 2. The range of deposition temperatures is from 200 to 400 °C, with pressures in the 1 to 3 torr range. Typical reactants are silane (SiH_4) and either ammonia (NH_3) or nitrogen (N_2). Some of the properties shown in Table I, including film composition, are strong functions of gas composition as well as deposition temperature, pressure, discharge frequency, power, and electrode geometry. For example, compressive stress is favored by lower frequency, and by the use of N_2, rather than NH_3.

Table I—Properties of PECVD Silicon Nitride Compared to Those of High-Temperature CVD Nitride*

Property	HT-CVD-LP 900°C	PE-CVD-LP 300°C
Composition	Si_3N_4	$Si_xN_yH_z$
Si/N Ratio	0.75	0.8–1.0
Density	2.8–3.1 g/cm³	2.5–2.8 g/cm³
Refractive Index	2.0–2.1	2.0–2.1
Dielectric Constant	6–7	6–9
Dielectric Strength	1 × 10⁷ V/cm	6 × 10⁶ V/cm
Bulk Resistivity	10^{15} – 10^{17} ohm-cm	10^{15} ohm-cm
Surface Resistivity	> 10^{13} ohms/sq.	1 × 10^{14} ohms/sq.
Stress at 23°C on Si	1.2–1.8 × 10^{10} dyne/cm² (T)	1–8 × 10^{9} dyne/cm² (C)
Thermal Expansion	4 × 10^{-6}/°C	4–7 × 10^{-6}/°C
Color, Transmitted	None	Yellow
Step Coverage	Fair	Conformal
H_2O Permeability	Zero	Low–none
Thermal Stability	Excellent	Variable > 400°C
Solution Etch Rate		
BHF 20–25°C	10–15 Å/min	200–300 Å/min
49% HF 23°C	80 Å/min	1500–3000 Å/min
85% H_3PO_4 155°C	15 Å/min	100–200 Å/min
85% H_3PO_4 180°C	120 Å/min	600–1000 Å/min
Plasma Etch Rate 70% CF_4/30% O_2, 150 W, 100°C	200 Å/min	500 Å/min
Na^+ Penetration	< 100 Å	< 100 Å
Na^+ Retained in top 100 Å	> 99%	> 99%
IR Absorption		
Si–N max	~870 cm⁻¹	~830 cm⁻¹
Si–H minor	———	2180 cm⁻¹

*After Kern and Rosler [7].

From a theoretical viewpoint, NH_3 is typically preferred due to the relatively low dissociation energy required to produce nitrogen atoms. However, with NH_3, hydrogen, in the form of Si-H and N-H, is found in the films to the extent of 18-30 at.% even at the highest end of the range of deposition temperatures used. Loss of this hydrogen during subsequent processing may prove detrimental to the underlying circuitry.

Significant threshold shifts have been observed in nitride encapsulated poly-silicon gate MOSFETs subjected to dc stress voltages. When N_2 was used instead of NH_3, the hydrogen content was reduced by as much as 75% and the threshold voltage shift decreased by as much as 90% [10]. Bound hydrogen can also affect the wet chemical or dry etch rates of the nitrides. For example, BHF etch rates of 10-1200 Å/min were measured for films with H contents of 12 to 30 at.%. The effects of deposition temperatures on BHF and plasma etch rates are shown in Figs. 3 and 4. While the effect on plasma etch rate is not of the same order of magnitude as that for BHF etch, it is significant and can have important processing implications in terms of etch selectivity with respect to adjacent films.

Dielectric Interlayers

PECVD Oxide and Oxynitrides

Dielectric interlayers represent another major application for PECVD oxides of the undoped and doped variety. Undoped oxide films are deposited by the reaction of silane and nitrous oxide (N_2O) and/or oxygen (O_2) at temperatures from 200 to 400 °C and frequencies of 400 kHz and 23.6 MHz in hot wall and cold wall reactors, respectively. Figure 5 shows the effect of deposition temperature on deposition rate, refractive index and BHF etch rates on oxide deposited in the hot wall type.

Films, typically 0.5 to 1.0 μm thick, exhibited pinhole densities of less than 0.5 per sq. cm and compressive stress of $\sim 10^9$ dynes cm^{-2}. The conformal nature of the films is demonstrated in Fig. 6. Interlevel capacitance can be controlled by varying the Si/O ratio or by adding N to the film composition to produce properties between those of an oxide and those of a nitride. With silicon oxynitride [$SiO_xN_y(H_z)$] films, formed by the combination of SiH_4, NH_3, and N_2O, improved thermal stability, cracking resistance, and decreased stress have been observed [11]. The oxynitrides are also less permeable to moisture and other contaminants than are silicon oxides. Another means of altering the interlayer capacitance is to combine the oxides in a layered structure with other thermal CVD or PECVD films. This also provides opportunities to make other advantageous use of the desirable properties of both materials. This will be discussed later.

PSG and BPSG Plasma Deposition

Phosphosilicate glass (PSG) is frequently used as a barrier layer and as a getter for sodium (Na) ions. Plasma PSG has been deposited at from 340 to 380 °C in parallel plate, cold wall systems and longitudinal, hot wall reactors at 13.6 MHz and 410 kHz, respectively [12-14]. The reactants typically have been SiH_4, N_2, O_2, and phospine (PH_3), with argon as a diluent. The films were generally more conformal, more crack resistant and had fewer pinholes than when atmospheric pressure, thermally deposited PSG (AP-PSG) was used. The phosphorous content of the films was as high as 8 wt.% and was primarily a function of the PH_3/SiH_4 ratio. Measurements of flat band shifts indicated that the plasma PSG was as effective in gettering alkali ions as was AP-PSG [14].

The step coverage of AP-PSG films can be improved by flowing them at temperatures as high as 1100 °C and by increasing the phosphorous content. Lower temperatures are desirable from the viewpoint of minimizing diffusion in MOS circuits, but excessive

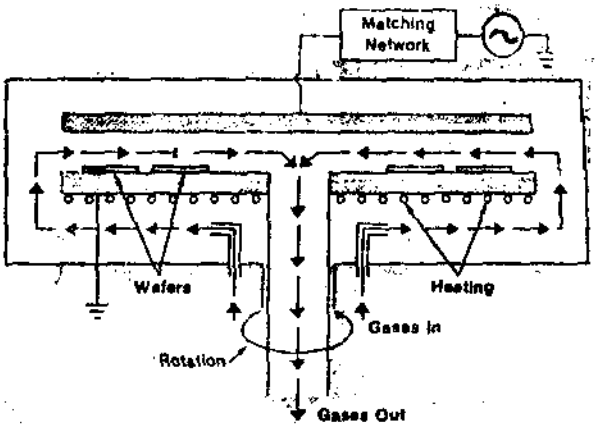

Fig. 1—Parallel plate, cold wall PECVD reactor.

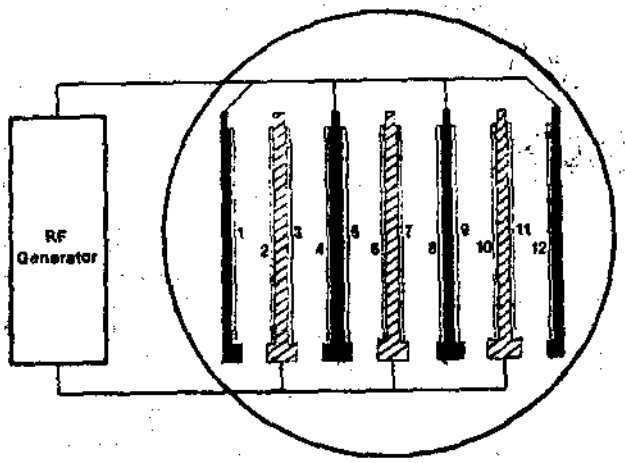

Fig. 2—Cross section of longitudinal, hot wall reactor.

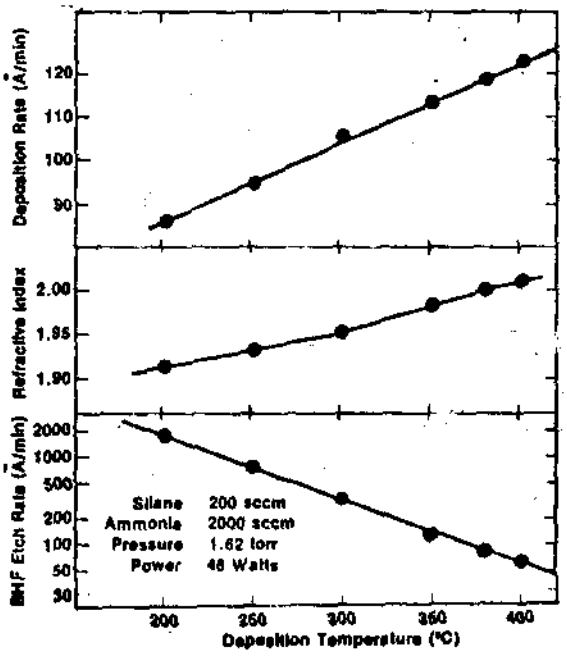

Fig. 3—Effect of deposition temperature on PECVD nitride parameters.

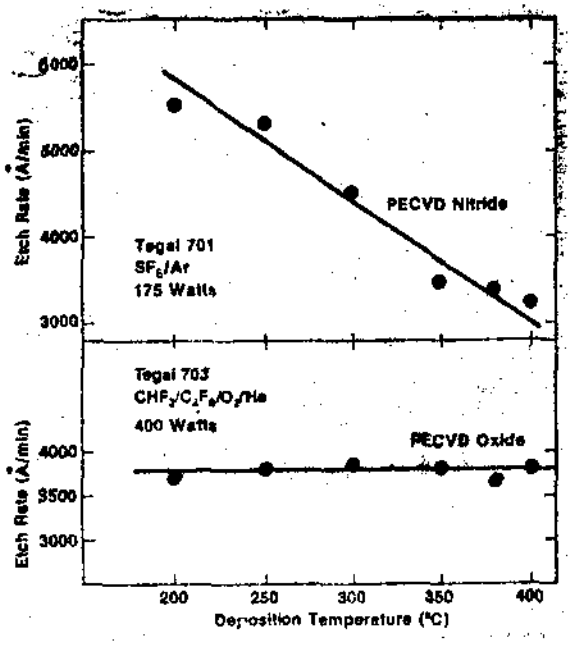

Fig. 4—Effect of deposition temperature on PECVD film plasma etch rates.

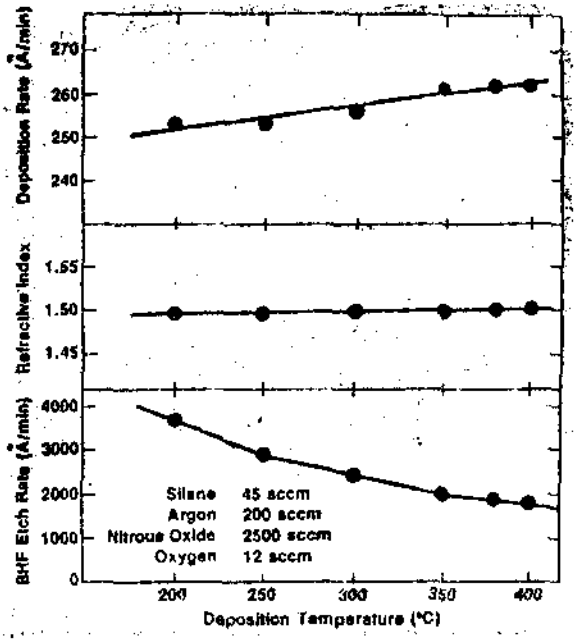

Fig. 5—Effect of deposition temperature on PECVD oxide parameters.

phosphorous can result in film compositions that are not thermally stable. Plasma PSG can also be flowed in order to partially planarize a topography that has already been conformally coated. However, the temperature for flow is about the same as for AP-PSG. This can be reduced by as much as 300 °C with the addition of boron (B) to the film.

Borophosphosilicate glass (BPSG) is deposited by adding diborane (B_2H_6) diluted in argon, to $SiH_4 + N_2O + O_2 + PH_3$ mixtures [12, 13]. A final boron content ranging from 3 to 5 wt.% is most frequently used. In the PECVD-BPSG films, the contents of phosphorous and boron are dependent on the PH_3/SiH_4 and B_2H_6/SiH_4 flow ratios, respectively, and are independent of each other [12].

For purposes of reflow after an initial densification in a nitrogen or steam ambient at 800 °C, it was found that an increase in the boron level of 1 wt.% results in a reduction of 40 °C in the temperature needed for reflow, while a 1 wt.% increase in phosphorous results in a 20 °C lowering of the softening point of the glass [12]. Maximum doping is limited by such factors as film thermal stability, interactions with adjacent layers, and marginal dopant solubility which may lead to segregation.

Planarization

Where adequate step coverage over high aspect ratio topographies cannot be accomplished by PSG or BPSG deposition and reflow, other means of surface planarization are employed. One technique involves the coverage of the interlevel dielectric by a layer of organic material, typically photoresist, followed by reflow of the resist and dry etching at equal etch rates of resist and oxide [15]. The latter is most critical since a difference in etch rates could undo the effects of the planarizing medium. In this respect, it has been noted that the dry etch rate of undoped PECVD oxide may be as much as 20-40% higher than that thermally grown or CVD oxides, and that doped PECVD oxides may etch twice as fast as these types. This must also be taken into account when etching a multilayer dielectric. In some cases this difference can be used advantageously. For example, the superior dielectric properties of PECVD silicon oxynitride have been used in forming the lower layer of a two layer planarizing film where the upper layer is a sacrificial layer of PECVD nitride [16]. During the planarization etch of the nitride/resist layer, the etch rate ratio of 1:5 for oxynitride to nitride and resist provides an etch stop in critical areas [16]. A photomicrograph of a planarized PECVD oxide dielectric interlayer over metal interconnects is shown in Fig. 7. This can be compared to the unplanarized topography shown in Fig. 8.

Special Structures

Trilayer Etch Masks

The planarizing properties of thick organic materials which are sometimes used to improve the step coverage of multilevel metallization, have also been used for improving the ability of virtually

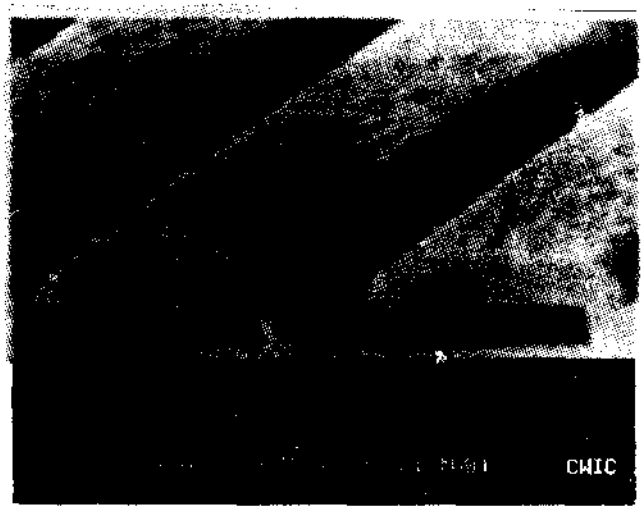

Fig. 6—SEM of PECVD oxide over polysilicon lines. Poly has been removed by wet etch to show detail.

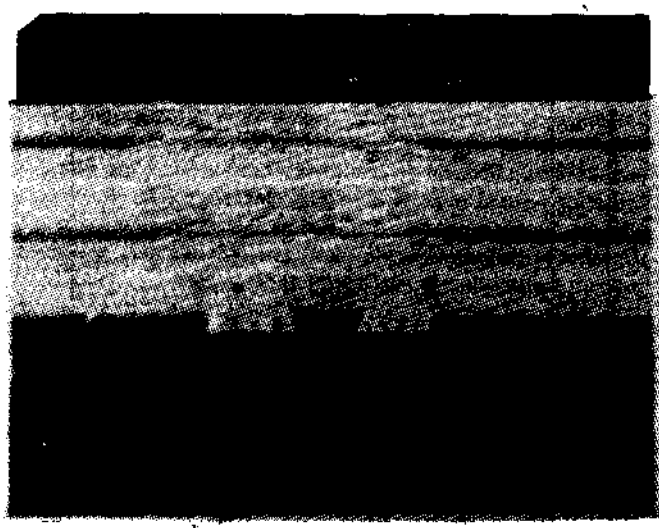

Fig. 7—SEM of PECVD oxide planarized over poly and metal lines by RIE of oxide and resist at the same etch rate.

Fig. 8—SEM of poly and metal lines covered with photoresist before planarization by RIE.

all forms of lithography to resolve small geometries over complex topographies. Trilayer resists typically consist of: (1) a lower layer of 1-3 μm of a novolac type resist, polyimide, polysulfone, or PMMA (polymethylmethacrylate); (2) a "hard" pattern transfer layer of 500 to 1000 Å of inorganic material; and (3) an upper, imaging layer of resist suitable for optical, e-beam, x-ray, or ion beam lithography [17].

PECVD nitride and oxide have been found to be suitable for the pattern transfer layer which serves as a relatively inert mask for oxygen RIE of the lower layer and final etch mask. The films are deposited over photoresist at a temperature of ~ 200 °C, and patterned using optical lithography. Oxygen RIE was then used to pattern the planarizing layer. After final RIE of the exposed material, the mask could be removed by wet chemical stripping and/or plasma etching, depending on the nature of the patterned film or the substrate.

Lift-Off Masks

If the process described above is altered during the O_2 RIE of the planarizing layer, resulting in isotropic rather than anisotropic etching of the resist, an undercut structure will be formed. This is accomplished typically by raising the O_2 pressure in the RIE chamber to increase the oxygen radical population which is largely responsible for lateral etching. Evaporation or sputtering of aluminum or other materials into this structure results in deposition on the substrate and top surfaces, with virtually no deposition on the sidewalls due to shadowing by the overhang. The mask and its overlying material are then removed (lifted off) by dissolving the organic layer and undermining the undesired portion of the metallization [17]. Metallizations with submicron linewidths have been produced by this technique without the need for critical RIE of the metal.

Two-level Etch Masks

In some applications, where planarization is not required, it is possible to deposit and pattern an inorganic mask directly over the material to be etched. A PECVD nitride mask of 500 to 1000 Å has been used to etch Mo and other metal geometries in the 1 to 1.5 μm linewidth range. The mask served not only to pattern the substrate, but was also used to study the sources of etched linewidth loss with different photoresists and/or etching chemistries, (Fig. 9). In Fig. 10, which can be compared to Fig. 9, undercutting is the prevailing

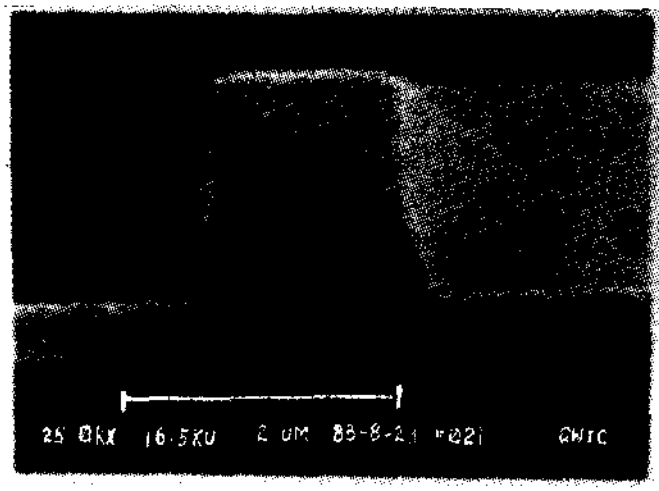

Fig. 9—SEM of cross section of patterned PECVD nitride mask over metal film to be etched. Photoresist is on top of nitride.

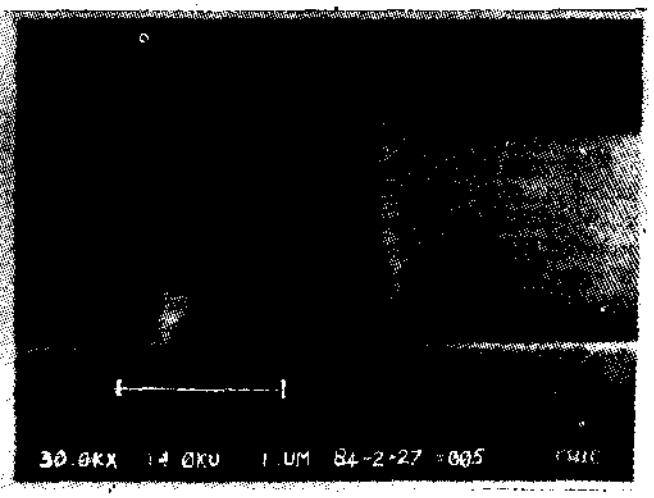

Fig. 10—SEM of cross section of etched metal line showing undercutting.

mechanism, while in Fig. 11, lateral erosion and undercutting are both sources of linewidth loss. The nitride mask was subsequently removed by a plasma etch which was sufficiently selective to avoid excessive loss of the substrate and the metal.

Spacers

Lightly Doped Drain structures (LDD) have been effective in reducing junction leakage and hot electron induced degradation in short channel MOS-FETs [18]. Such structures typically consist of oxide spacers formed on etched polysilicon sidewalls after an initial phosphorous-ion implant to form lightly doped n^- regions. The spacers then serve as masks for the heavy source-drain arsenic-ion implant.

Such spacers range in width from 1000 to 4000 Å. Using the conformal coverage provided by PECVD oxide and the vertical etching of RIE, the spacer width will generally be within a few hundred angstroms of the thickness of the deposited film. An SEM of a spacer configuration in the LDD application is shown in Fig. 12. Note than the spacers also serve to enhance film coverage over the vertical sidewall poly line.

Spacers have also been used during the silicidation of titanium over doped polysilicon gates and interconnects in order to increase their conductivity and circuit speed. During the process of heating the titanium, the metal over the oxide spacers is unreacted and can be removed easily leaving a self aligned silicide [19]. Other metals are also useful for this application.

The sloping of originally straight vias in order to provide for improved step coverage by the metallization has been yet another potential application for PECVD spacers [20]. PECVD oxide is first deposited over vias which have been formed by patterning and RIE. The oxide is then etched by RIE down to the original surface leaving sloped sidewalls in the interior of the vias which are well suited for metallization (Fig. 13).

PECVD oxide or nitride spacers on the vertical-walled first level metal of a two level metal structure have also been used to improve step coverage. In many cases the need for interlevel dielectric planarization, as described above, can be eliminated.

Refractory Metal Silicides

Titanium Silicide

Refractory metal silicides have resistivities typically an order of magnitude lower than that of doped polysilicon. For features lower than about 2 μm, this offers the opportunity to achieve higher device speeds than are characteristic of those based on polysilicon gates or gate level interconnects of the same dimensions. Sputtered silicides or metals (which can be subsequently silicided) are being widely investigated for this application [21], and the potential for excellent step coverage and high wafer throughput offered by the use of CVD films has stimulated interest in their development.

Plasma assisted CVD of titanium silicide has been reported [22] and is now available in commercial equipment. The process employs a longitudinal reactor similar in design to that used for dielectrics, polysilicon, and amorphous silicon. However, the graphite boat/electrode structure is modified to prevent the potential for arcing due to the deposition of the more conducting films on the insulating structures. The reactants are $TiCl_4$ (titanium tetrachloride) and SiH_4, with argon as a diluent. For the temperature range 300 to 450°C, thermal reaction alone is negligible, but in a glow discharge with rf power of 100 W at 50 kHz, the deposition rate of TiSi is 60 to 80 Å/min.

The amorphous film is deposited as the inner layer of a trilayer structure where the lower and upper layers are plasma-deposited amorphous silicon. Overall thickness is from 1500 to 2500 Å, and

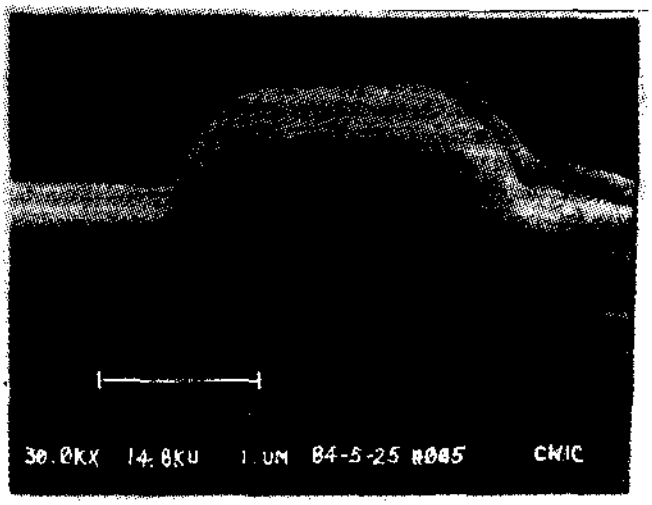

Fig. 12—PECVD oxide spacers on poly gate. Poly and implanted silicon have been etched to show detail.

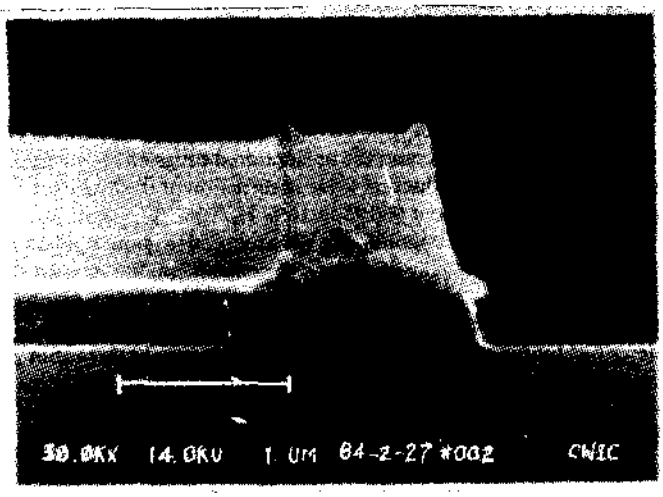

Fig. 11—SEM of cross section of etched metal line showing undercutting and lateral etching of the resist.

Fig. 13—Oxide spacer on sidewall of contact hole to improve step coverage.

the as-deposited sheet resistance ranges from 4 to 18 ohms/sq., depending on the $SiH_4/TiCl_4$ ratio (Fig. 14). Over approximately the same range of ratios shown in Fig. 14, the Si/Ti ratios increase from about 1 to 1.8. On annealing at 650°C for about 15 min., the sheet resistance is reduced by almost an order of magnitude to 0.8 to 1.5 ohms/sq. (20 to 37.5 μohm-cm resistivity). This lower and narrower range is due largely to interactions with silicon from the adjacent layer, resulting in Si/Ti ratios that are almost constant at 2.0 ($TiSi_2$) over a wide range of $SiH_4/TiCl_4$ ratios. The advantages of the low temperature deposition and low temperature anneal are obvious in view of the desire to limit diffusion and grain growth in small devices with shallow junctions.

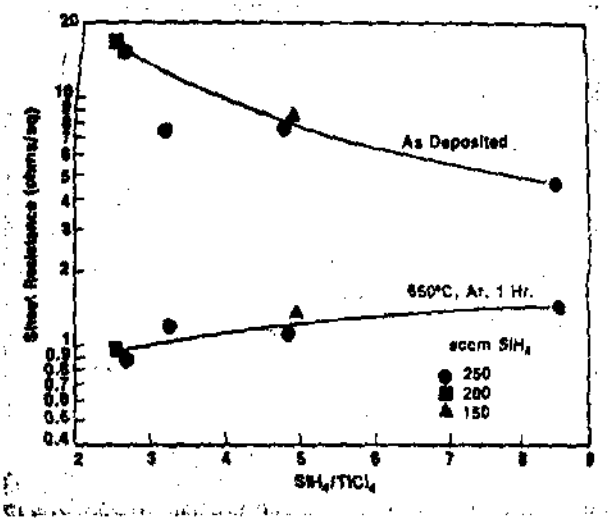

Fig. 14—Sheet resistance of TiSi as a function of $SiH_4/TiCl_4$ ratio (from Reference 22).

Other Silicides Formed by PECVD

Tungsten silicide can be deposited by plasma enhanced reaction between SiH_4 and WF_6 (tungsten hexafluoride), while molybdenum silicide is formed by the reaction of SiH_4 with $MoCl_5$ (molybdenum pentachloride) in the presence of additional hydrogen. The choice of refractory metal containing source gas is based, in part, on the ease of handling (i.e., volatility of the source); on the potential for contamination of the deposited films by elements present in the source; and on the etching characteristics of the reactants or products. The use of WF_6 is indicated by its low boiling point; and the successful deposition of WSi films in a range of reactant ratio dependent compositions has been reported [22]. The depositions were carried out in a parallel plate reactor at 230°C, 0.5-0.7 torr and an excitation frequency of 13.56 MHz. Deposition rates were on the order of 500 Å/min. The as deposited resistivities ranged from 40 to 4000 μohm-cm, for W contents of 90 to 15% respectively. On anneal at 700°C, in N_2 for 60 min., the resistivity range decreased to 35 to 400 μohm-cm. This decrease was attributed primarily to the loss of trapped fluorine and hydrogen from the as-deposited films.

For molybdenum silicide, MoF_6 with a boiling point of 18°C would appear to be the source of choice, but films deposited from the fluoride have been found to be high in fluorine content and with higher resistivity, apparently due to the formation of non-volatile MoF_3 [24]. $MoCl_5$ suffers from the inconvenience of heated gas supply lines and other precautions against condensation of the vapor, but the byproducts of reaction are more volatile. $MoSi_2$ films have been deposited at 400°C in a parallel plate reactor [25]. Hydrogen is added to the reactant gas mixture, apparently in order to scavenge chlorine atoms, but the resistivity of the as-deposited films is increased with increasing H_2 flow rates as well as with increasing SiH_4 rates. This is presumably due to decreasing Mo/Si ratios in the films. CVD refractory metals such as tungsten or molybdenum can also be used as gates or interconnects, either by themselves or if they are silicided by annealing after their deposition on polysilicon [21]. At the present time, the latter is the preferred mode, since there are some concerns regarding the oxidative stability of the metals or their reaction with silicon at elevated temperatures. However, the trend to smaller feature sizes will stimulate ways to utilize the even lower resistivities offered by these materials.

Tungsten and Molybdenum

Additional applications for CVD metals include metallizations in the first and subsequent levels of MOS devices since they do not exhibit the spiking, electromigration or hillocking, and large grain growth problems of aluminum. They also have higher melting points than those of aluminum and its alloys. Furthermore, the excellent step coverage demonstrated by CVD tungsten, for example, has greatly exceeded that generally obtained by sputtering, particularly over closely spaced, thick vertical walled lines or vias of small diameter and high aspect ratio. One scheme for which CVD of metals is particularly useful is the complete filling of such holes and the formation of "plugs" which represent the best opportunity for contact reliability and densely packed contact arrays. In the case of tungsten, another demonstrated advantage of CVD has been the ability to be formed selectively over Si and other materials in preference to SiO_2, thereby offering not only an opportunity for plugs but for self-aligned structures such as gates and active areas [26]. There have been no indications that PECVD tungsten can be selectively placed, and the prospects for doing so are slim due to potential ion bombardment damage of the oxide and the formation of nucleation sites for tungsten growth. On the other hand, where non-selective tungsten is desired, adhesion of the metal to SiO_2 is typically poor and has required the insertion of a "primer" layer such as tungsten silicide, polysilicon or another metal. PECVD may offer an opportunity for better adhesion due to some of the same mechanisms that adversely affect selectivity, or to differences in film stress. However, this has not been reported.

Tungsten has been deposited at rates of up to 40 Å/min. in a parallel plate reactor at temperatures from 200 to 400°C, pressure of 200 mTorr and a frequency of 4.5 MHz, using WF_6 and H_2 [27]. Without the addition of hydrogen, fluorine atoms formed by electron impact ionization of WF_6, are free to attack Si and SiO_2 until these layers are covered by a few monolayers of W. During a typical PECVD cycle as much as 700 Å of SiO_2 have been etched. Hydrogen atoms as well as molecular hydrogen can react with fluorine atoms to limit the etching reaction. Increasing the hydrogen flow also decreases the as-deposited tungsten resistivity, presumably due to the fluorine scavenging action of the hydrogen. After the anneal at about 950°C in 10% H_2/90% N_2, resistivities which were as high as 100 μohm-cm, were reduced to about 8 μohm-cm, regardless of virtually any of the deposition conditions used.

Molybdenum has also been deposited by PECVD processes using MoF_6 and H_2 mixtures under about the same conditions as described for tungsten. However, resistivity was over 10,000 μohm-cm, apparently due to fluorine incorporation [27]. $MoCl_5/H_2$ mixtures, reacting at a pressure of 1 torr and 170 to 430°C electrode temperatures, produced films with a resistivity of about 300 μohm-cm. On anneal in N_2 at 900°C, this was decreased to about 10 μohm-cm [25]. DC glow discharges in molybdenum hexacarbonyl, $Mo(CO)_6$ also have produced Mo films, although these were excessively high in carbon content due to the source gas [28].

Polysilicon and Silicon Epitaxial Films

Doped and undoped polycrystalline silicon films have been deposited in various plasma reactor geometries [29, 30] including the longitudinal type used for TiSi. The depositions were performed at about 600°C using gas mixtures of dichlorosilane/argon or silane/hydrogen. At temperatures below about 450°C, the films tend to be primarily amorphous. The ease of introducing dopants such as phosphorus during the deposition, without the need for auxiliary steps (e.g., $POCl_3$ doping) and accompanying potential problems of excessive grain growth and nonuniformity of distribution, appears to be the greatest driving force for the development of these processes for MOS applications.

Also promising is the ability to deposit silicon epitaxial layers at temperatures as low as 775°C using SiH_4 in PECVD reactor [31]. Compare this to conventional APCVD and LPCVD deposition at 1050 to 1200°C, which can lead to significant dopant redistribution. The need for in situ removal of native silicon oxide from the substrate surface to achieve epitaxial growth was conveniently provided by an argon glow discharge in the PECVD reactor.

Summary

PECVD has been demonstrated to be useful for the formation of high quality dielectric films at low temperatures and it is currently being applied in a number of steps in the fabrication of CMOS and other microelectronic circuits. Other potential PECVD applications of polycrystalline and amorphous silicon, refractory metal silicides, and metals are not yet at the same stages of development. However, the desire to limit the thermal treatment of the underlying films and diffusions will continue to be a driving force for further work aimed at commercialization of appropriate processes.

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