Material and optical properties of GaAs grown on (001) Ge/Si pseudo-substrate

Yves Chriqui[1], Ludovic Largeau[1], Gilles Patriarche[1], Guillaume Saint-Girons[1], Sophie Bouchoule[1], Daniel Bensahel[2], Yves Campidelli[2], Olivier Kermarrec[2], Isabelle Sagnes[1]
[1] Laboratoire de Photonique et Nanostructures, LPN-CNRS / UPR 20,
Route de Nozay, F-91460 Marcoussis FRANCE
[2] STMicroelectronics,
850 Rue Jean Monnet, F-38926 Crolles Cedex FRANCE

ABSTRACT

One of the major challenges during recent years was to achieve the compatibility of III-V semiconductor epitaxy on silicon substrates to combine opto-electronics with high speed circuit technology. However, the growth of high quality epitaxial GaAs on Si is not straightforward due to the intrinsic differences in lattice parameters and thermal expansion coefficients of the two materials. Moreover, antiphase boundaries (APBs) appear that are disadvantageous for the fabrication of light emitting devices. Recently the successful fabrication of high quality germanium layers on exact (001) Si by chemical vapor deposition (CVD) was reported. Due to the germanium seed layer the lattice parameter is matched to the one of GaAs providing for excellent conditions for the subsequent GaAs growth. We have studied the material morphology of GaAs grown on Ge/Si PS using atomic layer epitaxy (ALE) at the interface between Ge and GaAs. We present results on the reduction of APBs and dislocation density on (001) Ge/Si PS when ALE is applied. The ALE allows the reduction of the residual dislocation density in the GaAs layers to 10^5 cm^{-2} (one order of magnitude as compared to the dislocation density of the Ge/Si PS). The optical properties are improved (ie. increased photoluminescence intensity). Using ALE, light emitting diodes based on strained InGaAs/GaAs quantum well as well as of In(Ga)As quantum dots on an exactly oriented (001) Ge/Si pseudo-substrate were fabricated and characterized.

INTRODUCTION

For the past twenty years, many research groups [1] worked on the integration of III-V semiconductors with silicon-based integrated circuits. The wide range of applications, from low cost solar cells to fast clock signal distribution and optical interconnects, is very attractive. However, the lattice mismatch and difference in thermal expansion coefficients between GaAs and Si lead to high dislocation densities (>10^8 cm^{-2}) [2] and cracks in the epitaxial layer, resulting in low quality materials. Recently, an approach using relaxed Ge/$Si_{1-x}Ge_x$ graded buffer layers has been proposed for the successful monolithic growth of GaAs on Si. The reduced lattice mismatch (0.07% at 300K) due to the Ge layer enabled the realisation of GaAs/AlGaAs and InGaAs/GaAs quantum well laser diodes grown on 6° offcut Ge/$Si_{1-x}Ge_x$/Si pseudo-substrates (PS) [3,4]. The PS was misoriented to overcome the additional problem of antiphase boundary (APB) formation when growing polar (GaAs) on non-polar (Ge) material [5]. However, the compatibility with Si-CMOS microlectronics systems requires the use of exactly (001) oriented substrates. We present results on GaAs growth on exact (001) Ge/Si PS based on the atomic layer epitaxy (ALE) at the GaAs/Ge interface. We demonstrate that ALE combined with a low temperature buffer layer leads to a drastic reduction of the APB density, a low

dislocation density (< $5x10^5 cm^{-2}$), a smooth surface, and an increase of the photoluminescence (PL) yield of InGaAs/GaAs quantum well (QW) based structures. InGaAs/GaAs QW based light emitting diodes (LEDs) and In(Ga)As/GaAs quantum dot (QD) based LEDs were realised on (001) Ge/Si PS. First results gave wavelength emission at 1 µm, which can be increased to 1.2 µm for the QD based LEDs.

EXPERIMENTAL DETAILS

The Ge/Si PS were grown in an industrial lamp-heated single wafer chemical vapour deposition reactor on 200 mm diameter (001)-oriented silicon substrates [6]. The root mean square (rms) roughness after a chemical mechanical polishing step is less than 0.5 nm, providing an epi-ready surface for the subsequent III-V epitaxy. All III-V layers were grown in an EMCORE D125 MOVPE system at a working pressure of 60 Torr. Trimethylaluminium, trimethylgallium, trimethylindium, diethylzinc, silane, and arsine were used as precursors. The growth temperature was either fixed at 650°C for standard GaAs growth, or varied between 450 and 650°C for the ALE and the GaAs buffer layer. During the ALE step, Ga and As precursors are provided alternately [7], whereas for conventional GaAs growth sequences, Ga and As precursors are provided at the same time.

For this study, three samples were grown. First sample, Ge5, consists of a 1 µm thick GaAs layer directly grown on the PS at 650°C, after annealing the PS at 700°C under arsine in order to remove the native oxide and to passivate the surface by arsenic atoms. This sample was grown without using the ALE technique and without low-temperature grown GaAs buffer layer. The second sample, Ge183, consists of a 60 nm thick GaAs layer grown at 450°C after an annealing at 700°C under arsine flux, and without using ALE.
Then the third sample, Ge122b, was grown with ALE. The growth sequence was as follows : after the annealing step at 700°C under arsine flux, the growth temperature was ramped down to 450°C, and we proceeded to 20 ALE cycles, an ALE cycle consisting in providing 2.4 s of trimethylgallium followed by 6 s of arsine in the reactor. Subsequently, a 60 nm thick GaAs layer was grown at 450°C with the conventional sequence.
For PL measurements, two samples containing an InGaAs QW were grown : the re-growth procedure of Ge109 is similar to that of sample Ge5. For Ge110, we used a re-growth procedure similar to that of sample Ge122b. For both samples, the temperature was then ramped up to 650°C, and the InGaAs/GaAs QW was grown after a 500 nm high temperature GaAs layer.

Structural characterisations of these samples were performed using atomic force microscopy (AFM) and scanning electron microscopy (SEM). Before SEM observation, different chemical etching procedures were used to reveal the presence of APBs and dislocations. For the APBs, we dipped the samples during 20s in a "stain etching" solution consisting of HF(40%)-HNO_3(69%)-H_2O, with a volume ratio of 20:1:2 [8]. The total etched thickness was less than 20 nm. In the following, we will designate as APB density the length of APBs per unit area. In order to reveal dislocations in the PS, and thus estimate the etch pit density (EPD), we used a 2s dip in an iodine solution consisting of HF(40%)-HNO_3(69%)-CH_3COOH with a volume ratio of 5:10:11 with 30 mg iodine dissolved per 26 ml solution [9]. For the GaAs layers grown on the PS, the dislocations were revealed using either a Br-CH_3OH solution, or a modified stain etching solution (volume ratio 20:1:10).

Room-temperature photoluminescence measurements were carried out on samples Ge109 and Ge110. PL was excited using the 532 nm emission line of a doubled Nd-YVO_4 laser, and the PL signal was collected using a Ge detector cooled at liquid nitrogen temperature.

DISCUSSION

With conventional high temperature (HT) GaAs growth sequence, the Ge5 sample surface shows pits of average depth of more than 400 nm and antiphase boundaries are present (figure 1a, b)). We attribute the pits to a not completely removed oxide layer on the surface. After the step at HT prior to growth, the oxide layer on the surface might not be completely removed, and when the growth starts, selective epitaxy occurs because the atoms would not stick to the surface covered by oxide.

When the growth starts at low temperature (LT), as in sample Ge183, the pits have disappeared. Indeed, due to the lower temperature, the atoms are more likely to stick to the surface, even when oxide is still present. The surface morphology is improved, but the APB density has dramatically increased (D_{APB} = 18.4 μm^{-1}) as shown in figure 2 a. This increase is attributed to the lower diffusion length of the precursor atoms at LT, leading to smaller antiphase domains and thus to higher APB density. Figure 2 b shows the surface of sample Ge122b, where ALE was applied. Due to the alternate exposure to the precursor atoms, as opposed to conventional expitaxy, the diffusion length on the surface is increased, and the APB density decreased from 18.4 μm^{-1} to 5.8 μm^{-1}.

The effect of the ALE growth start on the dislocation density was evaluated by comparing the etch pit density after revelation of the threading dislocations on the Ge/Si PS and on the Ge122b sample. The ALE leads to a reduction of a factor 10 of the EPD between the PS (6 10^6 cm^{-2}) and the GaAs layer (~ 5 10^5 cm^{-2}).

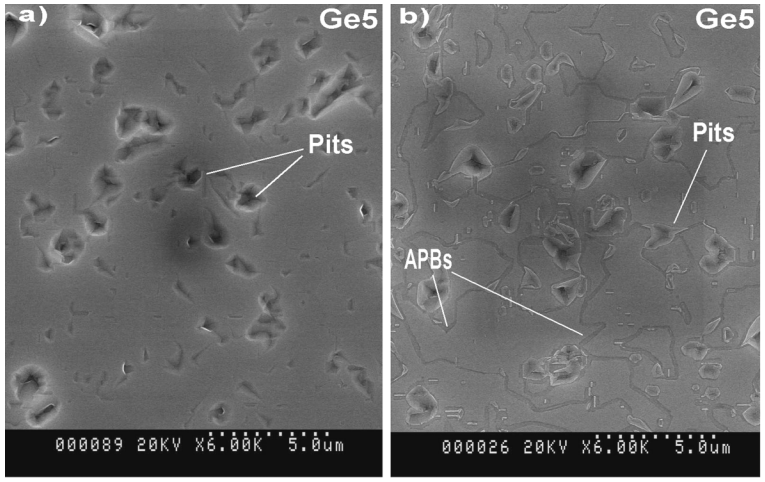

Figure 1. Sample with conventional HT GaAs growth sequence : a) as-grown, b) after APB revelation by stain etching (SEM micrograph).

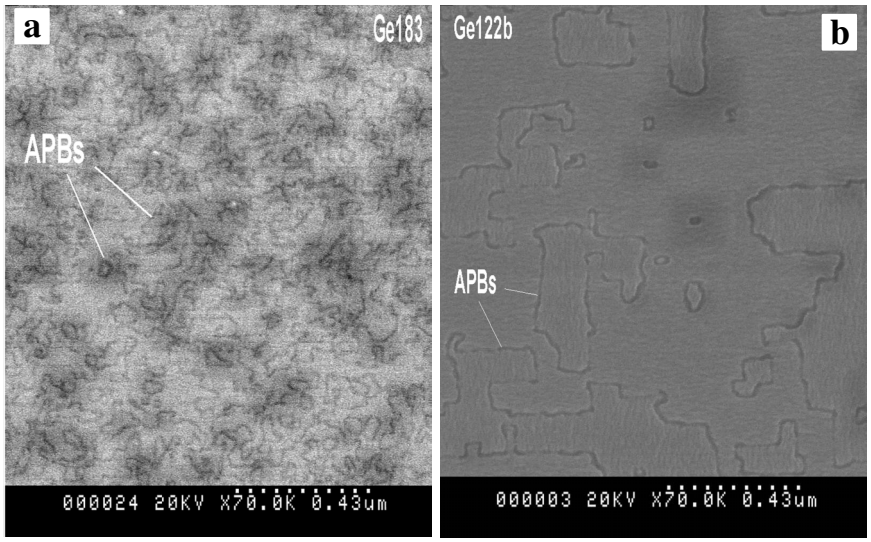

Figure 2. a) Sample with conventional LT GaAs growth sequence after APB revelation, b) sample with ALE + LT GaAs after APB revelation (SEM micrograph).

When the growth starts with ALE and LT GaAs, the GaAs layer presents a smooth surface, a low APB density, and a dislocation density one order of magnitude lower than that of the Ge/Si PS. All these lead to a better quality material as shown in figure 3. Two samples containing InGaAs/GaAs QW (8 nm thick with [In] ~ 20%) structures were grown on exact (001) Ge/Si PS, with conventional epitaxy (Ge109) and ALE +LT GaAs for the growth start followed by HT GaAs (Ge110). The spectrum of Ge109 exhibits two large peaks. One centred at 1.20 eV corresponds to the PL of the InGaAs QW. The second peak around 0.97 eV is attributed to the photoluminescence of defects in the layer. The Ge110 spectrum present a single peak around 1.16 eV attibuted to the PL of the InGAAs QW. We see that the PL intensity for Ge110 is 3 times higher than for Ge109. The full width at half maximum is also narrower for the sample with the ALE +LT GaAs growth start, showing the better quality of the material. The shift in PL wavelength between Ge109 and Ge110 may result from a difference in indium incorporation in the QW due to the different surface morphologies.

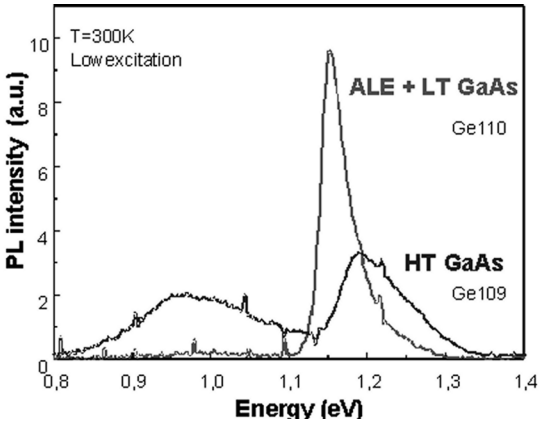

Figure 3. Photoluminescence spectra of sample Ge109 and Ge110 (room temperature).

To demonstrate the potential of exactly oriented (001) Ge/Si PS combined with the ALE technique, we grew and processed LEDs based on strained InGaAs/GaAs QW (8 nm thick with [In] ~ 20%) and In(Ga)As/GaAs QDs. The structure of the QW based LED is as follows : growth start as Ge122b (LT = 490°C), and after ramping up to 650°C a 0.5 µm thick of undoped GaAs was grown, followed by 1 µm thick n^+-doped GaAs bottom contact layer, 2µm n-doped $Al_{0.35}GaAs$ cladding layer. The InGaAs QW was embedded in 290 nm thick undoped GaAs waveguide. A 200 nm thick non intentionally doped AlGaAs layer and 1.8 µm p-doped $Al_{0,35}GaAs$ layer were grown forming the top cladding. Finally, the structure was finished with a heavily p^+-doped GaAs contact layer (200 nm). 50 µm broad stripes were defined on the p^+-doped GaAs contact layer.

Electroluminescence at room temperature (RT) under continuous wave injection was obtained at 1 µm (1.24eV) (figure 4). The maximum output power is 20 pW and the full width at half maximum (FWHM) is 72 meV. The limited output power may be due to the APBs. Indeed, with the ALE, the density is drastically reduced, but the APBs are not completely suppressed. This is why we used QDs as active material instead of QW. QDs are less sensitive to defects (APBs, dislocations) and enable to obtain longer wavelengths than QWs. The very promising result is the observation of RT electroluminescence of the QD-based LED at 1.2 µm (1.03eV), a wavelength not absorbed by silicon.

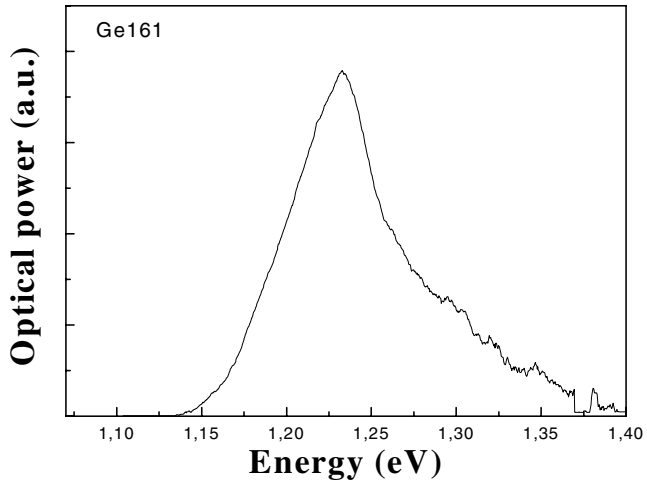

Figure 4. Electroluminescence spectra of InGaAs/GaAs QW LED.

CONCLUSIONS

We studied the effect of the atomic layer epitaxy and low temperature GaAs growth start as compared to conventional high temperature GaAs. The LT GaAs suppressed the formation of pits observed with the HT growth start, but increased the APB density. The use of ALE combined with LT GaAs at the beginning of the growth, lead to a smooth surface and a lower APB density and a dislocation density one order of magnitude lower than the Ge/Si PS. The so-grown material presented a higher PL intensity and a narrower FWHM. We were able to observe electroluminescence from InGaAs/GaAs QW based structures and In(Ga)As/GaAs QD LEDs, showing the potential of our approach for the monolithic integration of III-V on silicon.

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REFERENCES

1. S.F. Fang, K. Adomi, S. Iyer, H. Morkoç, H. Zabel, C. Choi, N. Otsuka, J. Appl. Phys. **68** (7), R31, (1990) and references therein.
2. A. Georgakilas, P. Panayotatos, J. Stoemenos, J.-L. Mourrain, A. Christou, J. Appl. Phys. **71** (6), 2679 (1992).
3. M.E. Groenert, C. L. Leitz, A.J. Pitera, V. Yang, H. Lee, R.J. Ram, E.A. Fitzgerald, J. Appl. Phys. **93** (1), 362 (2003).
4. Y.Chriqui, G. Saint Girons, S. Bouchoule, J-M. Moison, G. Isella, H. von Kaenel, I. Sagnes, Electron Letters **39** (23), 1658 (2003).
5. S. M. Ting, E.A. Fitzgerald, J. Appl. Phys. **87** (5), 2618 (2000).
6. C. Hernandez, Y. Campidelli, D. Simon, D. Bensahel, I. Sagnes, G. Patriarche, P. Boucaud, S. Sauvage, J. Appl. Phys. **86,** 1145 (1999).
7. T. Suntola, Handbook of crystal growth vol. 3, edited by Hurle (Elsevier Science Publisher 1994) p.602
8. A. Georgakilas, J. Stoemenos, K. Tsagaraki, Ph. Komninou, N. Flevaris, P. Panayotatos, A. Christou, J. Mater. Res. **8** (8), 1908 (1993).
9. D.P. Malta, J.B. Posthill, R.J. Markunas, T.P. Humphreys, Appl. Phys. Lett. **60** (7), 844 (1992).