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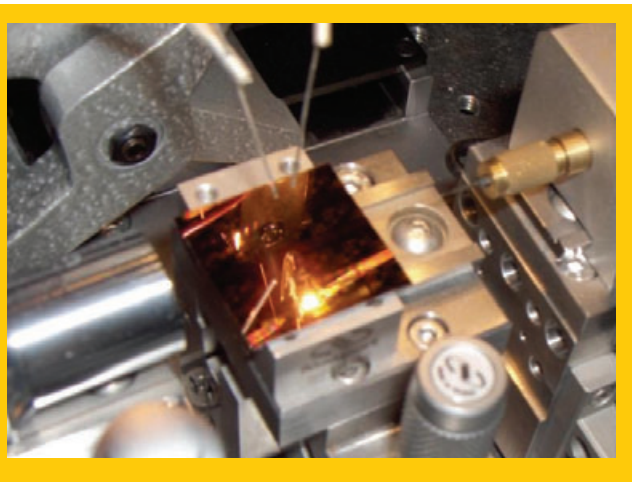
Abstract Silicon photonics defines a significant advancement in the development of highly integrated devices on a single semiconductor substrate. As a revolutionizing technology it benefits from the vast infrastructure accumulated over the previous six decades to service the burgeoning microelectronics industry and has found application in a range of areas such as telecommunications, sensing and optical interconnects. It is this latter application which is addressed primarily in this review. The potential for silicon photonics as a solution to high data rate transmission through the description of the devices and processes which have emerged in the last decade is discussed. An attempt is thus made to demonstrate that the integration of photonic and electronic functionality on a silicon substrate has the potential to propel communication beyond the Terabit per second threshold in a widely deployable paradigm.



The evolution of silicon photonics as an enabling technology for optical interconnection

Jonathan K. Doylend and Andrew P. Knights*

1. Introduction

The integration of electronic and photonic functionality in a manner compatible with processing protocols currently used in the microelectronics industry has begun to dominate the integrated optics arena [1]. Following the early progress of pioneers such as Richard Soref [2] in the 1980's, the volume of work on so-called silicon photonics has expanded rapidly and is now the subject of specific texts [3–5] and established international conferences [6,7]. In an effort to visually quantify the growth of the field, Fig. 1 plots the number of 'hits' from a search for papers and citations using the *ISI Web of Knowledge*^{SM} database using the keywords 'silicon' and 'waveguide' (certainly not a search which encompasses all silicon photonics papers, but surely one which may be deemed representative). From a modest number published in 1992 of less than fifty, the field had exploded to include over five hundred papers in 2008. A similar expansion of citations has realised over six thousand references to work in this field in 2010. Interestingly, the number of papers published in 2010 had fallen to less than five hundred which is perhaps an indication of maturity and consolidation as a number of large research groups based in both academia and industry begin to dominate.

This phenomenal activity has been in response, in the main, to the continued drive to maintain pace with Moore's Law and the subsequent difficulties associated with information transfer between devices. Moore's Law requires the doubling of electronic device density every two years [8] (thus increasing the processing speed in a concomitant manner).

Traditional interconnections are achieved using a copper/dielectric paradigm. The maximum frequency manageable by such an interconnect is dictated by its *RC* time constant which degrades quadratically with interconnect length [9]. Reductions in interconnect width with increasing device density exacerbate the problem by increasing electrical resistance. For interconnections between neighbouring regions of a processor, the length of the interconnect does decrease proportionality with device density, but for global interconnects which extend across the length of the chip the problem persists. Some mitigation is possible [10], but only at the cost of on-chip area, increased power density, and added delay. There also exist challenges in the metal/dielectric design with regard to power dissipation which is inversely proportional to impedance, and hence directly proportional to increases in signal frequency. Dielectrics have poor thermal conduction and thus the metallic transmission lines are heated significantly inducing electromigration and open-circuit failures. Finally, the increase in transmission speeds into the GHz regime induces significant loss in metal interconnects due to signal radiation, while antennae effects produce crosstalk between adjacent devices. These problems may be addressed only through the use of higher signal power.

It is clear that a radical development in interconnection technology is required to combat the limitations associated with the use of the metal/dielectric stack. The most promising solution is the use of optical interconnection whereby

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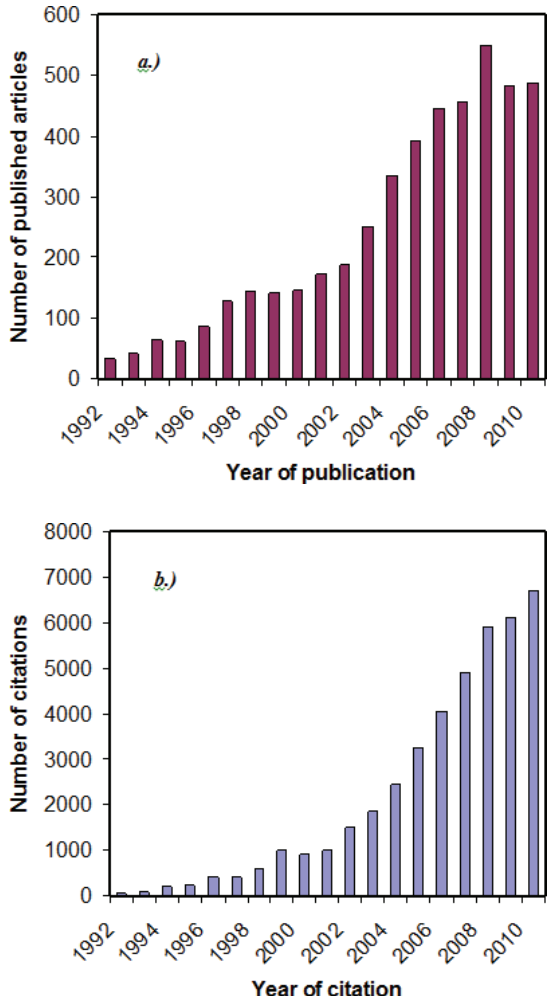

Figure 1 (online color at: www.lpr-journal.org) Number of 'hits' using a search of the database *ISW Web of Knowledge*^{SM}, using the keywords 'silicon' and 'waveguide': a) published articles; b) citations.

data is encoded onto an optical wave either by means of a directly modulated laser or (more likely) by an external modulator. The Nyquist frequency rather than the *RC* time constant becomes the limiting bandwidth factor, but as the optical frequency is of the order of several hundred terahertz, the Nyquist limit is of no concern for the foreseeable future. For optical wavelengths > 1100 nm, both silicon and SiO_2 are transparent, thus optical loss and power dissipation is negligible. Importantly, this wavelength cut-off excludes the important telecommunication bands *O*, *C* and *L*, and thus silicon photonics may make use of the vast knowledge and infrastructure associated with the fiber optics industry, and the devices developed to support the same. Indeed, the early development of silicon photonics was driven by the telecom industry and the goal to produce integrated optical solutions for fiber-to-the-home using the infrastructure originally dedicated to microelectronic processing [11]. A further important property of optical communication (and again one employed in telecommunications) is the potential for Wavelength Division Multiplexing (WDM) [12]. This technology is used to increase the aggregate bandwidth of a system by exploiting the fact that signals at different wavelengths may be used to carry information in parallel without interference. Thus, a data link which may be limited to a few tens of GHz, may be used in a WDM scheme to provide scaled data transfer of hundreds of GHz or higher.

There is then a steady increase in the move from electrical to optical technologies with regard to interconnects. Longer data links which have bundled tributary signals (thus with large bandwidth requirements) are already subject to the use of active optical cables. It is likely that optical technology will spread to the very shortest intra-chip distances (eventually) in response to the demands posed by increases in data rates.

The case for silicon photonics as the dominant platform for optical interconnection is based upon the well-developed infrastructure of the microelectronics industry and the compatibility for integration of photonic and electronic functionality in a cost-effective and monolithic manner. The wide availability of Silicon-On-Insulator (SOI) wafers [13] (developed initially to reduce electrical parasitic capacitance) provides a natural waveguide for optical transmission at wavelengths greater than 1100 nm. The development of silicon photonics has thus been driven by the need for the fundamental building-block devices of an optical transmission link – i. e. signal generation, detection and modulation. It is the remarkable recent progress made in the realization of these devices which forms the subject of this review.

2. Building block waveguide structures

In this section the basic physical building blocks of modern silicon photonics are reviewed and the physical properties which determine their effect on optical signals are described.

2.1. The Silicon-On-Insulator (SOI) waveguide

A guided optical signal in a planar chip requires a lower cladding layer to confine the beam near the surface. A planar layer of silicon dioxide situated below the silicon surface is well suited to this purpose. Such a material – Silicon-On-Insulator (SOI) – is in widespread use in the microelectronics industry. There have been several methods developed to fabricate SOI such as SIMOX, ELTRAN and BESOI; however the SmartCut® process has been established as the dominant technology. All four processes have been reviewed elsewhere [14].

The SmartCut® process was first proposed over twenty years ago [13]. In it, an oxidised silicon wafer is implanted with hydrogen/helium and bonded to a second 'handle' wafer. Upon thermal annealing the hydrogen/helium coalesces and creates large, buried microvoids, eventually causing the implanted wafer to cleave at a depth commensurate with the range of implantation. The result is a thin layer of crystalline silicon (the thickness of which is dictated by

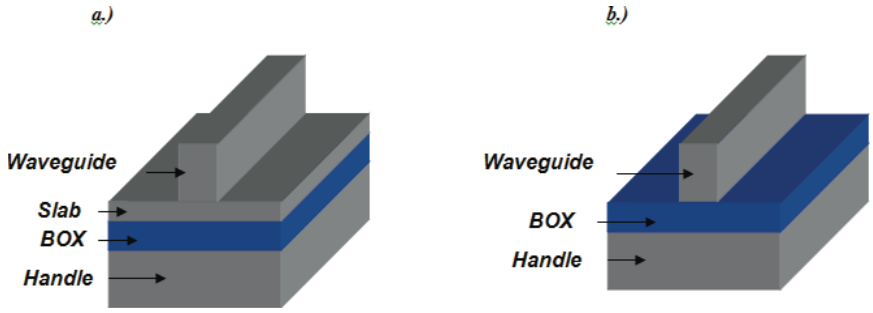

Figure 2 (online color at: www.lpr-journal.org) A schematic representation of an SOI optical waveguide: a) the ridge waveguide (electrical access to the propagating mode is provided by the silicon slab); b) the wire waveguide.

the implantation range) on top of a thermal oxide. The variation in dimensions across a wafer is determined by the variation in implanted depth and thermal oxide thickness-properties of two processes which are ubiquitous in silicon device processing.

The SOI structure thus provides a natural planar waveguide with a refractive index at 1550 nm of approximately 3.5 and 1.46 for silicon and SiO_2. In order to provide lateral confinement a ridge structure may be etched in the silicon thin film, with the ridge possessing an effective index greater than the adjacent slab regions. If the silicon is etched to the buried oxide a silicon wire is formed. In Fig. 2, we show a schematic representation of a silicon ridge waveguide (which includes a thin slab region suitable for electrical integration) and a silicon wire (where etching has removed the slab completely).

The calculation of propagation modes in such structures has been dealt with by many authors and is summarized by Reed and Knights [3]. The relatively large refractive index of the silicon thin film would imply the necessity for a small thickness to ensure single mode propagation. For a planar waveguide structure the number of guided modes is related to silicon film thickness (h) by:

$$\text{Number of modes} = \frac{k_0 nh \cos\theta_c}{\pi} \qquad (1)$$

where θ_c is the critical angle for total internal reflection, n is the refractive index and $\boldsymbol{k}_0$ the wavevector. For a silicon waveguide with thickness 5 µm, the number of supported modes is therefore >20. However, even in the case of films of thickness of several microns, design criteria exists which allow the formation of ridge waveguides such that higher-order modes are subject to significantly higher propagation losses and which therefore support only the lowest order mode for practical purposes, an important criterion for the use of such structures in integrated optical circuits [15].

The majority of recent work has taken place using silicon film thicknesses of around 220 nm. The propagation of light in waveguides of such thickness is unconditionally single mode in nature. The evolution in the thickness of the silicon waveguide has thus provided a reduction from several microns when development was dictated by the telecommunications applications in the 1990's, to a thickness of 200–300 nm as the requirement for small device structures has become important. Sub-micron waveguide dimensions provide strong optical confinement and thus permit waveguides with small bend radii. This has obvious benefits with regard to a reduction in device footprint. Another benefit of the use of waveguides with relatively low dimension is that they allow for the fabrication of modulators with high bandwidth, a subject to be dealt with later in this review. This is a direct result of the ability to deplete small waveguides of charge [16], whereas modulation in large volumes requires an approach reliant on carrier injection [17]. Strong confinement of light in such small waveguides has also presented the possibility of the exploitation of non-linear effects which are not described further in this review, although the interested reader is directed to several papers on this subject [18–20].

The fabrication of submicron waveguides does pose significant challenges with regard to propagation loss and device uniformity. This subject has been dealt with in detail by Bogaerts et al. [21]. The formation of either a ridge or a photonic wire requires definition of the waveguide edge in photoresist (via deep UV or electron beam lithography) and subsequent dry etch. These combined processes induce roughness along the sidewall edge, as shown in Fig. 3 which is reproduced from Tsuchizawa et al. [22]. The large modal overlap with the surface of the waveguide results in significant scattering of the light, which manifests in propagation losses far in excess of the large cross section waveguides of the 1990's which were reported as inducing loss of less than 0.1dB/cm [11]. Significant reduction in roughness and thus propagation loss may be achieved through thermal oxidation

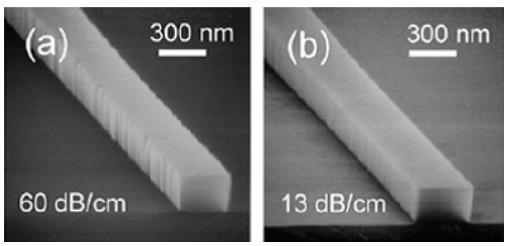

Figure 3 Side wall roughness in silicon waveguides induced by dry etching. The propagation loss reduction is associated with the observed reduction in sidewall roughness. © IEEE. Reprinted with permission from [22].

of the etched waveguide. This technique was reported by Lee et al. in relation to the formation of photonic wires [23]. In that case, for a waveguide width of 500 nm and height of 50 nm, propagation loss was reduced from 32 dB cm^{-1} to 0.8 dB cm^{-1} after a post-etch oxidation. The benefits of even a thin (few nanometers) dry thermal oxidation with regard to smoothing have been reported [21]. Others have extended the concept of oxidation smoothing in order to form waveguides in an etchless process, similar to the LOCal Oxidation of Silicon (LOCOS) technique [24]. Cardenas *et al*. have formed waveguides in this way with a height of only 70 nm and 1 μm width with a resulting propagation loss of 0.3 dB cm^{-1}. An example of a waveguide from this work is shown in Fig. 4 [25].

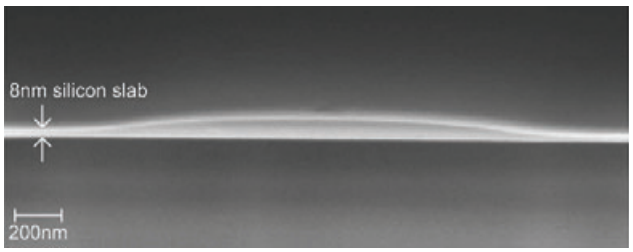

Figure 4 Low-loss etchless silicon waveguide formed via an oxidation process. Reproduced from [25].

A fabrication process which does not require a post-etch oxidation remains desirable and recent progress towards low-loss waveguides may render the use of oxidation smoothing redundant. For example, Gnan et al. [26] have reported waveguides (photonic wires) formed via electron-beam lithography which have loss of only 0.92 dB cm^{-1}. For high volume fabrication however, photolithography is required. An ingenious approach to low-loss waveguides formed using a optical stepper and dry etch (with no recourse to oxidation) was recently proposed by Bogaerts and Selvaraja [27]. They fabricated hybrid waveguides which were of the ridge design for propagation in a straight, and of wire design for sections requiring tight bends. The propagation loss was reported to be 0.27 dB cm^{-1}.

Standard waveguide-based devices such as directional couplers, multi-mode interferometers (MMI's), Mach-Zehnder interferometers (MZI's), and arrayed waveguide gratings (AWG's) have been well established building blocks in SOI for over a decade and will not be discussed in this review. The operating principles of MMI's are described elsewhere [28] as is their implementation in SOI [29]. The reader is also referred to excellent texts on the subject of the theory and implementation of directional couplers, MZI's, and AWG's [3–5].

2.2. Integrated optical gratings

Gratings provide a means of coupling between waveguides and optical modes, reflection, wavelength filtering, and input/output coupling. Coupling to a waveguide layer from a beam in free space was first proposed by Dakss et al. [30] and has since been demonstrated in silicon for fiber-chip couplers, distributed feedback and distributed Bragg lasers, and wavelength filters. Within silicon photonic devices, gratings are typically implemented by etching a periodic pattern into the waveguide layer as shown in Fig. 5. An alternate approach uses ion implantation rather than etch steps to introduce periodic refractive index variation into the waveguide [31–33].

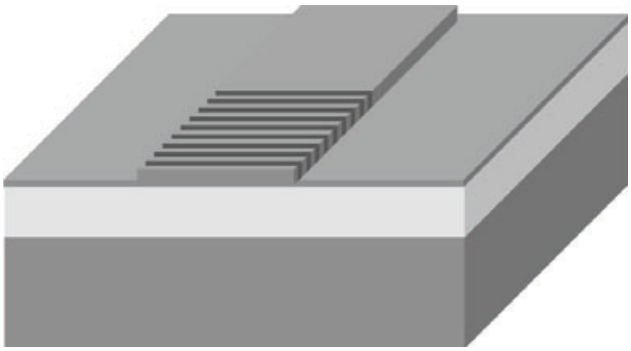

Figure 5 A schematic representation of a grating structure etched into the waveguide layer in SOI.

The fundamentals of grating theory and design are well known [34] but will be briefly summarized here for the reader's convenience. Coupling between field components in a grating structure is governed by the Bragg condition shown in Eq. (2):

$$\beta_2 = \beta_1 + q\mathbf{K} \tag{2}$$

where β_1 and β_2 are the propagation constants of the individual components, $\mathbf{K}$ is normal to the plane of the grating and has magntiude $K = 2\pi/\Lambda$ for grating period Λ, and $q = 0, \pm1, \pm2, \ldots$ is the coupling order. For coupling into or out of a waveguide, this resolves to the expression shown in Eq. (3):

$$\sin\theta = \frac{\Lambda n_{eff} - \lambda_0}{\Lambda n_c} \tag{3}$$

where n_{eff} is the waveguide effective index, n_c is the refractive index of the material to/from which the mode is coupled, and θ is the coupling angle.

The "strength" of the grating is defined as the product of the index difference within the grating and the fractional overlap of guided optical power with the grating structure. Increasing the grating strength improves the reflectivity and determines the grating bandwidth. The diffracted beam shape may be adjusted by apodization (i. e. non-uniform grating strength) while the spectral properties of the grating may be altered by "chirping" the grating, i. e. employing a non-uniform grating period or effective index. Sub-wavelength gratings (i. e. gratings for which the feature size is significantly less than the wavelength) allow diffracted power to be concentrated in the zeroeth order.

Gratings integrated with waveguides may be used as reflectors at one or both ends of a laser cavity – forming a distributed Bragg reflector (DBR) laser – or may be used along the length of the laser cavity – a distributed feedback

(DFB) laser. This allows the cavity length and operating wavelength to be defined using techniques such as electron-beam lithography, holography, or photolithography. Phase shifts in the grating may be used to counteract the inherent degeneracy of Eq. (2) [35, 36] so as to avoid mode-hopping in DFB lasers without relying on perturbations due to irregularities within the cavity. Holographic grating fabrication techniques are limited with respect to apodization, chirping, and the precise placement of phase-shift regions, so in practice electron-beam lithography is often required for gratings whose resolution exceeds that of available photolithography. In this respect silicon photonics (e. g. DFB lasers fabricated using the hybrid III-V/silicon platform described elsewhere in this review) offers an advantage since the lithographic resolution available in silicon foundries is superior to that readily available in III-V foundries.

A prominent application for waveguide-integrated gratings is for efficient optical coupling between on-chip and off-chip waveguides (e. g. optical fiber). Recent developments with regard to this application are discussed in the following section.

2.3. Fiber-chip couplers

Due to the mode mismatch between optical fiber and waveguides in SOI photonic circuits, efficient coupling at the input/output of the chip requires a means of converting between the large fiber mode and the comparatively small rib or wire waveguide mode. Mode converters for silicon photonics are typically based either on a grating or a taper structure.

A taper in both width and height improves mode matching between the fiber and the waveguide via a large cross-section end facet followed by adiabatic mode evolution to the desired waveguide dimensions. The approach suffers from the necessity for gray-scale lithography to achieve a vertically sloped taper, which is both a non-standard process and subject to scattering loss due to surface roughness. Vertical tapers, and hence gray-scale lithography, can be avoided by separating the taper into upper and lower regions such that the combined end-facet height is comparable to the fiber mode. A lateral taper in the upper region forces mode evolution until the beam is entirely confined to the lower. Coupling losses of less than 0.5 dB have been demonstrated using this approach with a total length of less than 1 mm [37]. Processing requires either selective epitaxial growth or two-stage silicon etch, however. It has been suggested that the use of muliple-layer SOI can circumvent the problems associated with the two-stage etch by providing an etch stop; in this technique the device acts as a vertical directional coupler rather than an adabiatic mode converter [38]. A similar approach in which two upper-level stages are used rather than one has also been demonstrated [39].

By tapering the waveguide to a narrow rather than a large tip at the end facet, mode confinement is reduced such that the mode profile expands both laterally and vertically, thus enabling mode matching to the fiber. This technique has been demonstrated with losses between 3 and 6 dB for taper lengths of only 50 µm [40], and 81% coupling efficiency using in-plane sub-wavelength gratings [41].

Grating structures can be used to diffract input radiation at near-normal incidence into the rib layer at angles that satisfy the phase-matching condition. This approach has been demonstrated for 220 nm SOI with 25% coupling efficiency [42]. Grating couplers have become increasingly popular due to their compactness and to the fact that inputs/outputs can be placed anywhere on the surface of the chip rather than being limited to the end facets. Improved coupling efficiencies of 37% have been demonstrated using shallow-etched gratings [43], 42% using photonic crystal structures within the grating [44], 64% using apodization [45], and 69% using backside reflectors [46].

2.4. Ring resonators

Resonant cavities in silicon can be accomplished using either reflective facets, gratings or photonic crystal structures, or ring resonant structures. Reflective facets suffer from the need for a non-planar fabrication step and from the limitations associated with tailoring the reflectivity to desired values: end facets can be polished and coated with a stack of dielectric films, but etched facets for cavities within the chip can generally only be made reflective at specific values owing to the difficulty of controlling film thickness on vertical features. This problem can be circumvented by adding patterned microstructures to the facet [47], however such patterns must necessarily be sub-wavelength in dimension and therefore generally require fabrication by electron beam lithography rather than standard photolithography. Ring structures offer a means of fabricating a resonant cavity with input/output coupling and resonant length determined by standard photolithographic techniques. Such resonators have been used in a wide variety of silicon photonic devices including optical filters [48–50], Raman amplifiers and lasers [51–53], hybrid III-V/silicon lasers [54–56], integrated multiplexers [57], resonant-cavity photodiodes [58–61], and modulators [62–69]. It should also be noted that ring resonant structures may also be used as mirror elements [68] in lieu of facets on a separate resonator. The theory of ring resonant structures will briefly be summarized here; the interested reader may find a more detailed analysis provided by Yariv [70, 71].

The simplest ring resonator structure comprises a bus waveguide coupled to a ring with amplitude coupling coefficient k such that for input bus amplitude a_1, amplitude coupled to the ring $b_2 = ka_1$ and output bus amplitude $b_1 = ka_2$ for ring round-trip returned amplitude a_2. The ring has amplitude transmission coefficient r such that $a_2 = b_2 re^{j\theta}$ with round-trip phase $\theta = 2\pi n_{\text{eff}}/\lambda_0$ for effective index n_{eff} and free-space wavelength λ_0 (here the phase change induced at the coupler has been included in the round-trip phase change θ). This structure and the associated coefficients are illustrated in Fig. 6. An alternate arrangement in which a second bus waveguide is coupled to the ring and used as an output is also common.

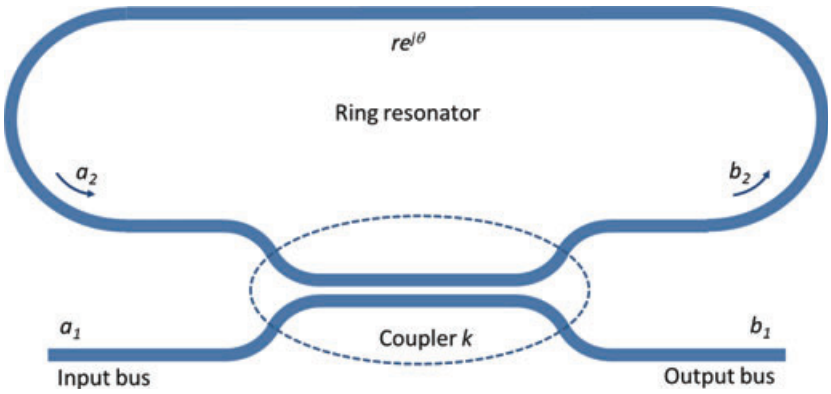

Figure 6 (online color at: www.lpr-journal.org) Schematic representation of a racetrack ring resonator structure showing the "bus" waveguide coupled to the ring. It is apparent that coupling between the ring and bus waveguide is analogous to the facet transmission of a Fabry-Perot cavity.

By substitution it is easily shown that relative ring resonant power and output bus power immediately following the coupler are given respectively by Eq. (4) and Eq. (5) with $t^2 = 1k^2$:

$$\frac{B_1}{A_1} = \left|\frac{b_1}{a_1}\right|^2 = \frac{t^2 + r^2 - 2rt\cos\theta}{1 + r^2t^2 - 2rt\cos\theta}, \tag{4}$$

$$\frac{B_2}{A_1} = \left|\frac{b_2}{a_1}\right|^2 = \frac{k^2}{1 + r^2t^2 - 2rt\cos\theta}. \tag{5}$$

For the special case in which $\cos\theta = 1$ (i. e. "resonance") it can be shown that the output power reaches a minimum, approaching zero for the case of "critical coupling" in which $r = (1 - k)$, i. e. coupling into the ring equivalent to round-trip loss within the ring. For coupling greater than round-trip loss the structure is said to be "overcoupled", while for the opposite case the structure is "undercoupled". The calculated transmission of a typical ring resonator versus round-trip phase for three coupling cases is shown in Fig. 7.

It is evident that by designing the resonator to be close to critical coupling, power stored within the ring at resonance reaches a maximum suitable for efficient detection and optical pumping. Modulation can be achieved by altering the effective index of the waveguide such that the resonator can be tuned between on-resonance and off-resonance conditions.

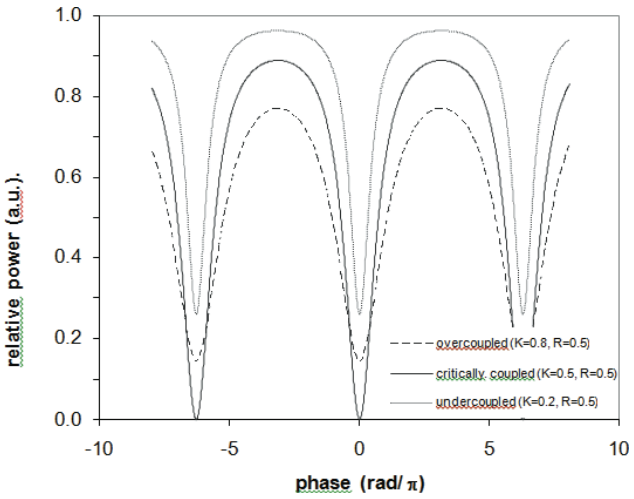

Figure 7 (online color at: www.lpr-journal.org) Calculated transmission of a typical ring resonator versus round-trip phase for three cases of coupling to the ring: overcoupled, critically coupled, and undercoupled.

2.5. Photonic crystals (PhC) and slow light

The term photonic crystal refers to a structure in which there is a periodic modulation of the dielectric in one, two or three dimensions [72]. For wavelengths which are equivalent to the periodicity of the modulation, the propagation of light is affected by the interference caused by interaction with the periodic perturbations in refractive index. SOI provides an ideal material for the formation of photonic crystals. The etching of the thin silicon film in a periodic pattern results in a PhC with a large change in refractive index at the silicon/air interface of each etched 'hole'. An example of a PhC waveguide formed in 2D in a silicon substrate (the same structure could be used with an SOI substrate) is shown in Fig. 8, reproduced form Loncar et al. [73]. Waveguiding is performed via the introduction of a crystal 'defect', which may be for example a row of missing holes.

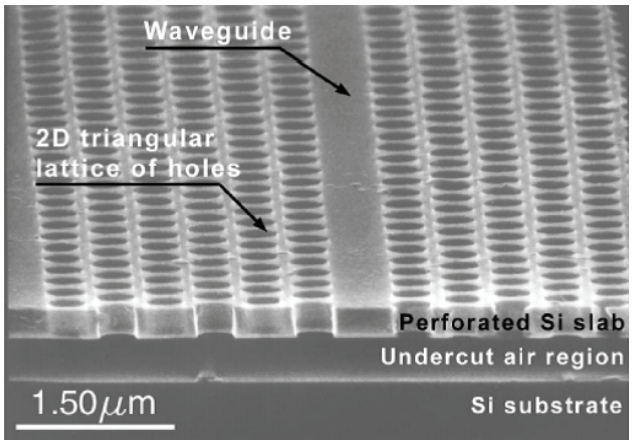

Figure 8 Photonic crystal waveguide fabricated in a silicon substrate. Reprinted with permission from [73]. Copyright (2000) American Institute of Physics.

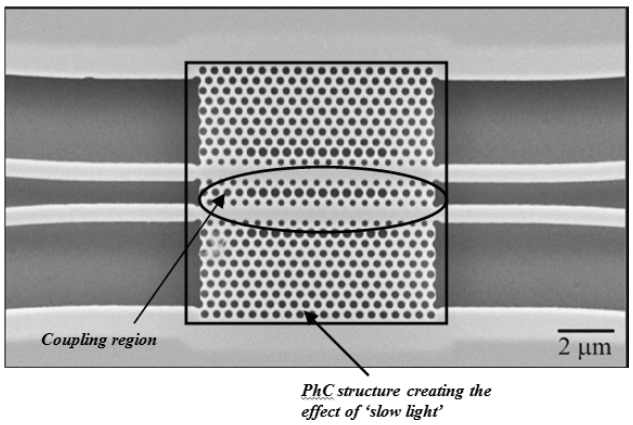

Figure 9 The coupling region of a slow-light enhanced MZ switch. Reproduced from [76].

Although, in principle, PhC could be used in the formation of waveguides for optical interconnection it is the opinion held in this review that a complete guiding system reliant on PhC is impractical from a view-point of integration and propagation loss. However, recent work on the development of 'slow light' structures using the principles of PhC fabrication show great promise for effective index engineering, allowing an increase in cross section for propagating signals in devices such as Mach Zhender interferometer (MZI) based switches [74]. The slow light waveguide operates in a similar manner to a conventional cavity device except that it is somewhat leaky with the advantage of higher optical bandwidth [75]. The result is a group refractive index which may be an order of magnitude higher than in conventional small cross section SOI waveguides. We highlight one example of an integrated device which exploits this concept. Figure 9 shows a reproduction from Beggs et al. [76], in which a thermo-optic MZI switch was fabricated in SOI. The PhC structure which creates the slow light effect is shown enclosed inside the rectangle, while the coupling region of the two waveguides is shown inside the oval. The device afforded thermal switching for an optical bandwidth of 1.2 nm for an applied power of 200 mJ. Or, in other terms, the device length required to allow switching was 36 times smaller than in conventional thermal switches.

The concept outlined by Beggs et al. could easily be applied to other devices such as those which rely on carrier injection and depletion with significant impact on speed and device footprint.

2.6. Polarization control

Due to their geometry (assuming the core is not perfectly square) and the high index contrast between silicon and common cladding layers, significant birefringence is a typical property of waveguides fabricated in SOI. Polarization diversity, whether by polarization splitting/rotating or by counteracting the geometrical birefringence of the waveguide, is of considerable importance to the success of silicon photonic circuits.

Polarizing beam splitters (PBS) have been implemented in SOI using a variety of techniques including directional and mode evolution waveguide couplers, Mach-Zehnder and multi-mode interferometers, and photonic crystals/gratings. Directional coupler polarization splitters are designed such that the device length corresponds to an even multiple of the coupling length (or is negligible relative to the coupling length) for one polarization and an odd multiple for the other. This approach was first demonstrated with rib waveguides in SOI by Kiyat et al. [77] with polarization extinctino ratios (PER) of 18.1 dB (TE) and 8.8 dB (TM) for a device length of 120 μm. Fukuda et al. [78] have demonstrated a similar approach using SOI wire waveguides with 15 dB PER for a device length of 16 μm, and PER $>$20 dB for a dual cascaded device. Slotted waveguide [79–82] and mode evolution [83] designs have been proposed for further improvements in PER and footprint.

Interferometer-based polarization splitters operate by using waveguide birefringence to accomplish polarization-dependent interference at the outputs. A Mach-zehnder interferometer PBS with 1 cm length and PER $>$ 15 dB for both polarizations was demonstrated by Liang et al. [84], while multi-mode interferometer polarizing beam splitters have been demonstrated by Katigbak et al. [85] with PER of 13 dB (TE) and length $<$ 50 μm, and by Yang et al. [86] with PER of 18.2 dB and length of 8.8 μm.

Photonic crystal based polarizing beam splitters have been reported by Ao et al. [87] with PER of 10 dB, while Feng et al. [88] demonstrated a PBS incorporating a 2-layer blazed grating coupler. The latter device exhibited 20 dB PER with a coupling length of 14 μm.

The ability to rotate polarization in combination with polarizing beam splitters is a requirement for true polarization diversity within a silicon photonic circuit. While polarization rotation can be accomplished in principle via cascaded waveguide bends [89], the performance is highly dependent on waveguide geometry and as such is very sensitive to fabrication parameters such as etch depth and sidewall angle. Slanted-core [90, 91] and missing-corner [92] waveguides have also been proposed but are similarly difficult to fabricate. Taillert et al. [93] and Bogaerts et al. [94] reported a 2-dimensional grating coupler for fiber-coupling to the chip which combined polarization and rotation of TM to TE. This technique is particularly elegant in that it combines the fiber-coupling, polarization splitting, and polarization rotation functions into a single element on the chip. A schematic diagram of this approach is reproduced from Bogaerts et al. [94] in Fig. 10.

A stacked-waveguide approach proposed by Yue et al. [95] avoids the need for angled features; stacked waveguide adiabatic tapers have been proposed by Feng et al. [96] and demonstrated by Zhang et al. [97] Rotators have also been demonstrated using an off-axis double-core structure such that the eigen axes of the waveguide are tilted relative to the TE and TM polarization axes. [98]

Polarization independence has also been shown to be achievable by engineering the cladding-induced stress in an SOI waveguide so as to compensate for geometrical birefringence [99]. This ingenious approach renders devices

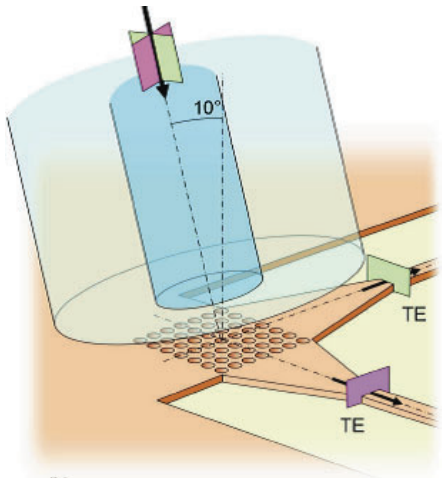

Figure 10 (online color at: www.lpr-journal.org) Schematic of the 2D grating coupler / polarization splitter. Reproduced from [94].

effectively polarization diverse across a wide wavelength range [100], and also raises the possibility of birefringence "trimming" towards the back end of the fabrication process.

3. Development of processing strategies

3.1. CMOS compatible processing where possible

A significant advantage of the silicon photonics platform is that it is compatible with the processing facilities and strategies which have been developed for the microelectronics industry over the previous five decades. With minimum feature sizes now well-below 100 nm [101], the fabrication of waveguides with dimensions of many hundreds of nanometers would appear straightforward. With the exception of the extended processes outlined in Sects. 3.2–3.4, the fabrication of devices proceeds with well-documented strategies such as photolithography, ion implantation, oxidation, dielectric deposition, annealing etc. [102].

Of some significance, the last five years has witnessed the emergence of a number of foundry facilities which now routinely provide access to those wishing to fabricate silicon photonic chips [103–105]. Other major commercial manufacturers have developed exclusive relationships with established microelectronic foundries [106] or rely on state-of-the-art in-house facilities. For those with more modest development budgets, such as in the academic environment, the use of a shared space on a common process via 'shuttle runs' is deemed enabling. The importance of the emergence of this fabrication capability cannot be overestimated. It is clearly a major advance in the quest for the commercialization and deployment of silicon photonics.

3.2. Hybridization

With no readily apparent means of achieving electrically pumped optical gain in monolithic silicon, the alternative approach of bonding III-V materials to silicon devices has emerged as the most viable for the integration of lasers and amplifiers in silicon photonic circuits. The inherent challenge presented by such techniques is one of alignment: with waveguides present on the silicon and lasers/amplifiers pre-fabricated on the III-V chip, the two must be bonded together in a manner that allows for low-loss transfer of optical power from one to the other, thus requiring alignment precision that is small relative to the mode size in each material, i. e. typically less than 1 μm. Until the advent of hybrid integration, the most promising approach was bump-bonding in which the alignment relied on the surface tension of stripe-type Au-Sn solder bumps on either chip pulling them together during bonding to achieve an estimated 4.5 dB coupling loss, estimated to be due to ±1 μm misalignment [107]. The process is illustrated in Fig. 11.

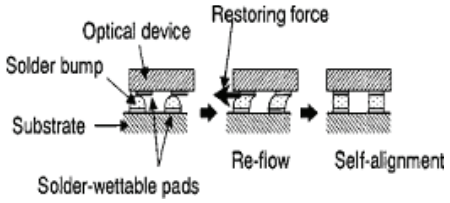

Figure 11 Hybrid chip alignment by solder bump bonding. Reproduced from [107].

This alignment issue can be largely circumvented by bonding a III-V wafer to the patterned silicon waveguides. The penetration of the evanescent tail of the guided optical mode into the III-V material is used to accomplish gain while the mode remains within the silicon waveguide thus eliminating the need for either fine alignment or high coupling losses. Ensuing etch steps can then be used to define devices within the III-V layers but since the lateral mode confinement is determined by the silicon rib waveguide, the III-V features can be considerably larger than standard waveguide widths. This approach, illustrated schematically in Fig. 12, was used in 2005 to fabricate an optically pumped laser [108], and in 2006 to demonstrate the first electrically pumped laser in silicon [109].

Wafer bonding is not new, having been used for some time in the production of commercially available bond and etch-back silicon-on-insulator (BESOI) and SmartCut® [110] silicon-on-insulator (SOI) wafers; however the wafer bonding in these processes is typically done at temperatures in excess of 600 °C, which is not feasible for the hybrid bonding approach due to dopant diffusion within the already patterned silicon devices and to the disparate thermal expansion coefficients of III-V materials and silicon. For hybrid III-V/silicon devices two low-temperature processes are established: low temperature oxygen plasma-assisted direct bonding (LTOPA) and adhesive bonding using divinylsiloxane-bis-benzocyclobutene (DVS-BCB).

The LTOPA process [109] was developed at the University of California, Santa Barbara. The process begins with an aggressive cleaning of both surfaces to be bonded in order to remove contaminant particles. The native oxides on each

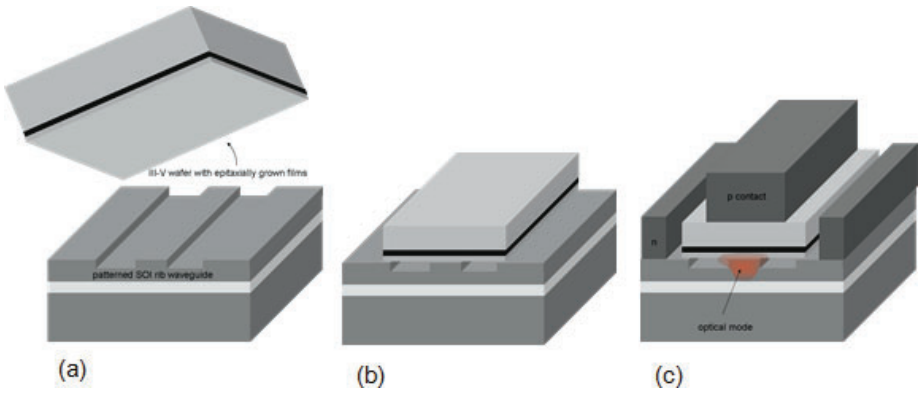

Figure 12 (online color at: www.lpr-journal.org) Diagram of simplified hybrid silicon device process, (a) bonding of III-V wafer with epitaxial layers grown on InP to patterned silicon rib waveguide, (b) removal of excess InP and etching, (c) contact deposition, with the region occupied by the optical mode shown overlaid.

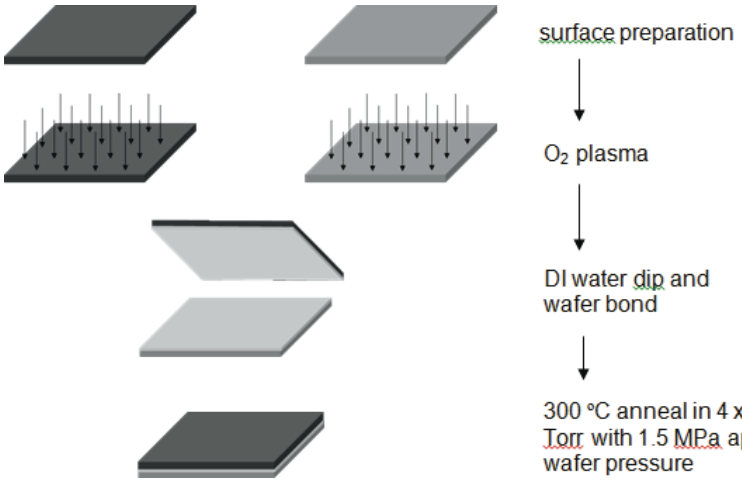

Figure 13 (online color at: www.lpr-journal.org) Schematic diagram of the LTOPA wafer bonding process.

surface are then removed by an HF (for silicon) / NH_4OH (for InP) dip, and a new thin (<5 nm) oxide is grown by a second O_2 plasma treatment. The surfaces are then prepared for bonding by a deionized water dip, and the wafers mated together. A subsequent 300 °C anneal cements the bond, after which excess InP can be removed by wet etching. This process is shown schematically in Fig. 13.

The DVS-BCB process [111, 112] for low-temperature hybrid bonding was developed at the University of Ghent, Belgium. Again, the process begins with an aggressive clean of both surfaces to remove particulates and organic contaminants. Commercial adhesion promoter AP3000 and then DVS-BCB are spun onto the SOI surface followed by a 150 °C anneal for one minute to evaporate most of the adhesion promoter and reflow the DVS-BCB. The samples are then brought into contact at 150 °C, after which the adhesive is cured at 250 °C under flowing nitrogen. The overall process is shown in Fig. 14. Devices which take advantage of the integration of III-V materials with silicon using the hybrid approach are discussed in further detail in Sect. 4.

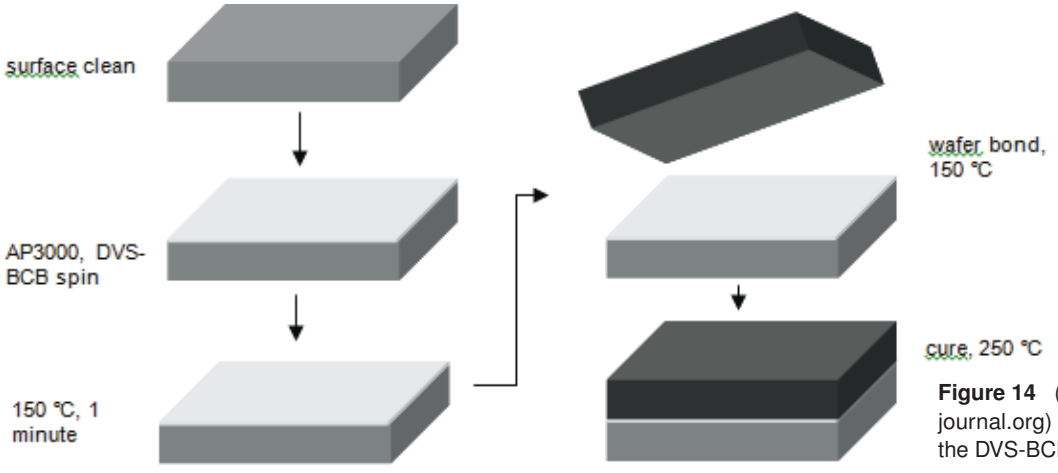

Figure 14 (online color at: www.lpr-journal.org) Schematic diagram of the DVS-BCB adhesion process.

3.3. Defect engineering

Defect engineering refers to the deliberate introduction of perturbations to the silicon device (or its dielectric components) in order to induce a change in the device properties either during operation or to elicit a process that would not normally be permitted by the undefected silicon or structure alone. This is a very broad definition and may include (in microelectronics applications alone) carrier lifetime engineering through enhanced Shockley Reed Hall (SRH) recombination; internal gettering of impurities; and modification of diffusion of dopants [113]. This review has already discussed the important role that defect engineering plays in the creation of SOI via the SmartCut® technique, crucial to silicon photonics [13].

In the case of silicon photonics, defect engineering has a complex impact on both the manipulation of charge carriers (as in microelectronics) and the propagating optical signal. Both the real and imaginary component of the refractive index (RI) of silicon is susceptible to lattice defect concentrations. This fact has been known and studied for many decades, for example the early work of Fan and Ramdas showed that particle irradiation of silicon would significantly enhance optical absorption of light at wavelengths with equivalent energy lower than the bandgap [114]. In the same work the authors showed that such carrier excitation could lead to a small photo-current in silicon for such sub-bandgap wavelengths. In 1973, Baranova et al. determined the relationship between RI and dose for a number of implanted ions [115]. Unlike for the case of optical absorption though, the exact nature of this increase in the real component of RI with implantation dose is still not determined. In Fig. 15 we reproduce the work of Fan and Ramdas et al. with respect to the modification of the RI of silicon.

In 2005, Bradley et al. [116] published the first work on the use of defect engineering as a means to modify the functionality of a silicon photonic device. In that case the authors showed that it was possible to fabricate a photodetector with sensitivity at 1550 nm by introducing low concentrations of point defects into a silicon ridge, integrated with a p-i-n diode. The linear relationship with input optical power suggested an excitation process which combined optical and thermal excitation to induce charge separation. In 2006, work by Foster et al. developed an empirical model to predict the absorption to be expected following a wide range of ion implantation processes with a variety of ion species, energies and doses [117]. Further, by monitoring the annealing characteristics of the ion implanted waveguides, shown in Fig. 16, they were able to deduce that the dominant, optically-active defect had the same annealing characteristics as the silicon divacancy. More recently, Doylend [118] confirmed the role of the divacancy as the defect that mediates charge separation in the photodetectors reported by Bradley et al. [116].

There has been a modicum of published work on the exploitation of the modification of the real component of RI via defect engineering in silicon photonics. The most notable has been the demonstration of planar Bragg gratings in the surface of silicon ridge waveguides. Bulk et al. [31] showed that such devices could provide adequate RI modification to observe significant filtering of signals propagating in

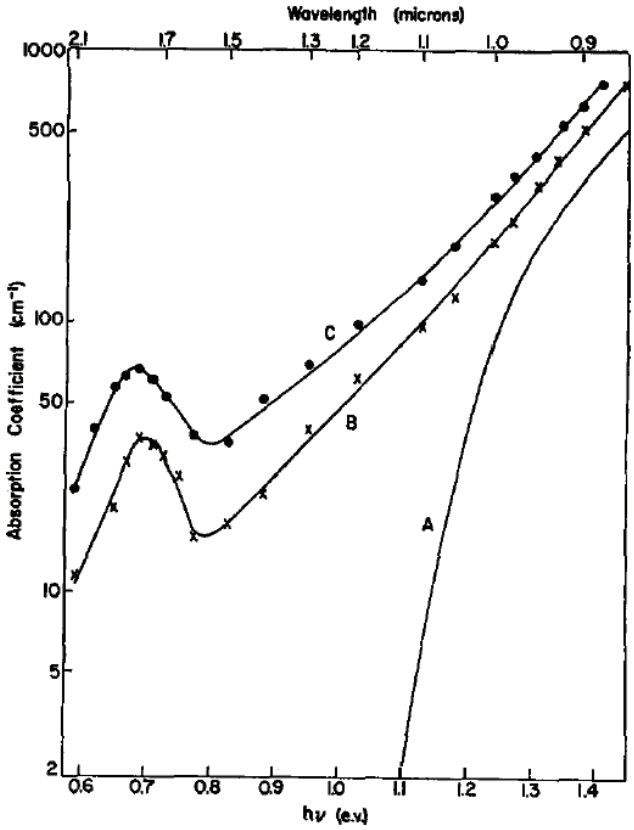

Figure 15 The modification of optical absorption of silicon following irradiation – slope A is for undefected silicon; slopes B and C are for silicon irradiated successively with deuterons. Reprinted with permission from [114]. Copyright (1959) American Institute of Physics.

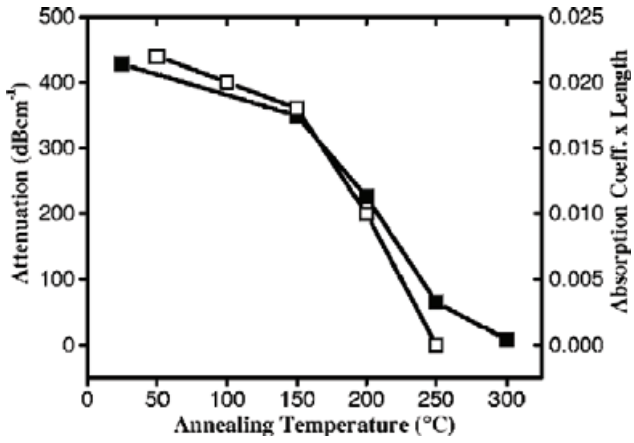

Figure 16 The response in excess absorption of ion irradiated silicon as a function of annealing temperature for: solid data points as measured in an SOI waveguide; open data points as determined from spectroscopic absorption measurements sensitive to the removal of the silicon divacancy. Reprinted with permission from [117]. Copyright (2006) American Institute of Physics.

SOI. This work was continued by the same group with Homampour et al. [119] demonstrating Bragg gratings in ridge waveguides, tunable via the thermo-optic effect.

The power of defect engineering lies within its ease of implementation. Defects may be introduced via masked ion implantation at energies and doses used in standard silicon device fabrication, particularly if the silicon ridge height is close to 220 nm. Such thin films allow boron ions for example to pass through to the buried oxide leaving a trail of defects at a dilute concentration [120]. Modification of the implanted defects either to create more complex secondary structures, or simply to remove a fraction of their initial concentration, can be achieved through relatively low annealing of approximately 300 °C. As device designers become comfortable with the defect implantation process and the increase in monolithic functionality that it brings, it is likely that defect engineering will play a significant role in the future of silicon photonics.

3.4. Integration of Germanium

The transparency of silicon to wavelengths around 1300 nm and 1550 nm (the property that makes it an ideal substrate for integrated photonics) prevents the straightforward optical to electrical conversion required in integrated photonics. By adding germanium to the silicon matrix it is possible to engineer the absorption edge so that it is moved from 1100 nm to a wavelength deeper into the infrared toward 1880 nm (the absorption edge for pure Ge). The introduction of Ge also results in an increase in the RI which may be used to create waveguides, or manipulate the propagating mode for large volume interaction with an integrated detector [2].

The heteroepitaxial growth of Ge (or Si/Ge) on a silicon substrate presents a number of issues related to the introduction of crystalline defects such as dislocations. This is a direct result of the 4.2% lattice mismatch of Si and Ge [121]. In the case of detectors, dislocations are usually manifested in the form of unacceptably large dark current.

There has been a great deal of work to overcome the problems with Ge integration which has enabled the development of fast and efficient integrated detectors. It is beyond the scope of this review to describe all of the detailed work which has led to this remarkable achievement, although notable milestones were reported by Fama et al. [122], Liu et al. [123] and Colace et al. [124]. As with the case of defect engineering, the use of Ge benefits from its compatibility with standard silicon processing- for instance in the strain engineering of transistors [125].

4. Device technology

Silicon photonics is certainly an application driven research field. There are four functions ideally required by a circuit: (1) waveguiding (optical confinement); (2) light generation and amplification; (3) light detection; (4) light modulation. In this section we explore recent advances in approaches to (2)–(4), whereas waveguiding was described in detail in Sect. 2.

4.1. Sources

The development of an efficient light source or laser using a monolithic, silicon structure would be deemed an achievement of monumental significance. It would revolutionize almost every aspect of modern technology; including the pursuit of silicon-based optical interconnects [126]. The difficulty in achieving this goal is founded in the indirect bandgap of silicon, which prevents efficient radiative recombination observed in III-V based optoelectronic materials such as GaAs and InP. Band edge luminescence in bulk silicon is a three-body process involving an electron, hole and phonon. The probability of defect mediated recombination is far greater than radiative recombination and thus room temperature internal quantum efficiency is as low as 10^{-6}. Two further mechanisms limit light amplification in silicon: the Auger process and free carrier excitation, both of which increase in probability with an increase in doping level.

On the nano-scale, crystalline silicon can be made to efficiently emit light because of the effects of quantum confinement [127]. Here, the radiative recombination of an exciton is increased due the enhancement in overlap of the electron-hole wavefunctions. Further, the probability of recombination via a defect state is dramatically reduced due to the small scale of the crystalline silicon. Efficient light emission was originally described by Canham in relation to (nano-scale) porous silicon [128]. The instability of the porous structure, and difficulty in transferring the efficient photoluminescence to an electroluminescence device has however proved problematic in the widespread adoption of porous silicon as a route to efficient silicon Light Emitting Diodes (LEDs) and precludes its use as a gain medium. Of more interest from a view point of stability and optical gain is the fabrication of nano-structures embedded in a silicon based dielectric such as SiO_2 or Si_3N_4. The obvious compatibility of these materials with silicon processing also makes this an attractive approach [126]. Silicon nanocrystals (Si-nc) may be introduced via the deposition of sub-stoichiomteric dielectric [129] or through the implantation of silicon into a thermally grown oxide [130]. Subsequent high temperature (>1000 °C) annealing forces phase separation and the formation of crystalline silicon particles with diameters on the nm scale. An example of such a particle is shown in Fig. 17, taken from Bonafos et al. [131]. Strong photoluminescence is observed from such systems, an example of which is shown in Fig. 18 [132], and despite the difficulties associated with carrier injection into the dielectric host, (weak) electroluminescence has also been observed, as shown in Fig. 19 [133].

Of significance, doping the silicon-rich dielectric with a rare-earth ion such as erbium results in an efficient transfer of energy from the Si-nc and emission at a wavelength associated with the rare-earth is observed. This effect is extremely important because it results in photon emission which is sub-bandgap in nature and thus suitable for waveguiding in silicon. The early observation of this phenomenon was reported by Franzo et al. [134], with a great deal of work following by others. Recently Crowe et al. [135] have shown that through modification of the fabrication process

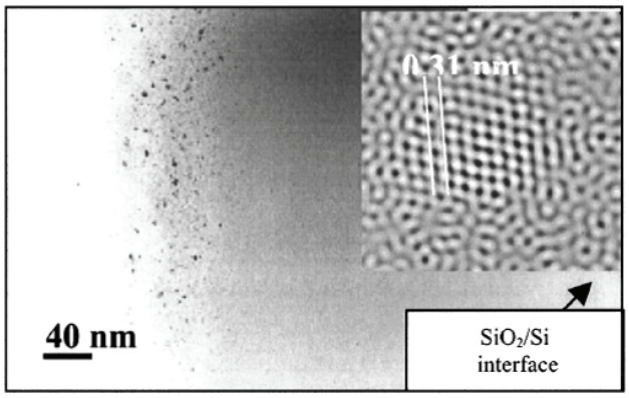

Figure 17 High resolution TEM image of silicon nanocrsytals embedded in SiO_2. Reprinted from [131]. Copyright (2001), with permission from Elsevier.

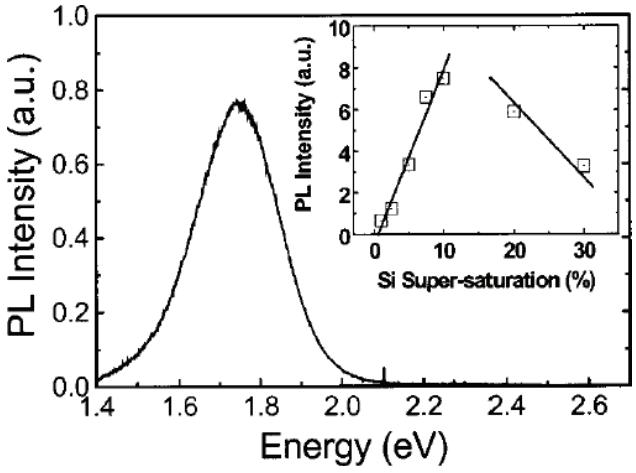

Figure 18 Absorption and Photoluminescence spectra for an ensemble of silicon-nanocrystals embedded in SiO_2. Reprinted with permission from [132]. Copyright (2002) American Institute of Physics.

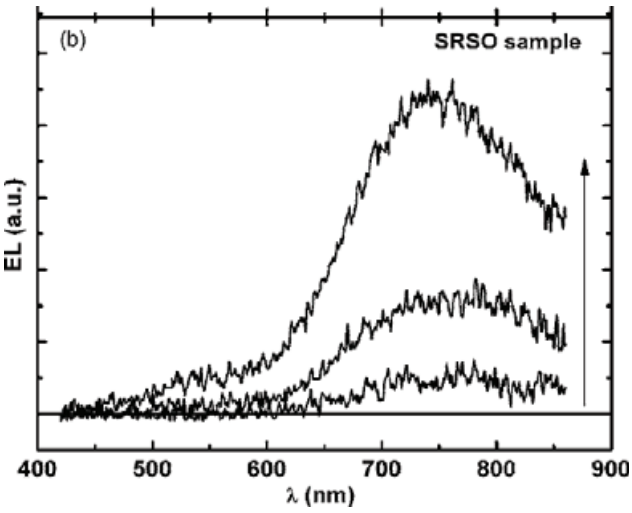

Figure 19 Electroluminescence obtained from silicon-rich SiOx. Silicon nanocrystals were formed via implantation and annealing. The arrows indicate increasing electric field applied to the SiOx film containing the silicon nanocrystals. Reprinted with permission from [133]. Copyright (2006) American Institute of Physics.

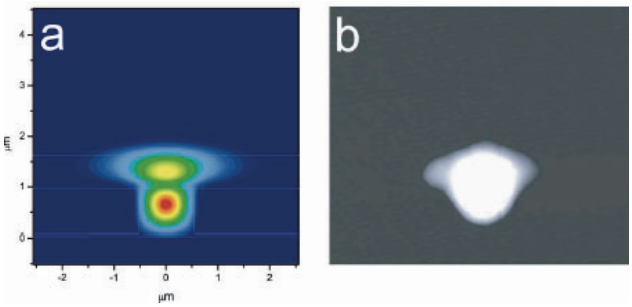

Figure 20 (online color at: www.lpr-journal.org) a) Calculated fundamental TE mode. b) Observed lasing mode of the UCSB hybrid laser. Reproduced from [108].

such that the erbium is implanted into the silicon prior to oxide growth and Si-nc formation, a process of self-alignment of the erbium and Si-nc takes place yielding enhanced luminescence.

Although there have been reports of optical gain in Si-nc based systems, there is still no evidence that emission efficient enough in nature to make these structures useful in advanced optical interconnection is forthcoming. For these applications the only viable demonstration of on-chip integration has used an approach of hybridization of III-V material via intimate wafer bonding, described in Sect. 3.2. This approach utilizes a silicon waveguide mode evanescently coupled to III-V semiconductor multiple quantum wells, thus combining the advantages of high-gain III-V materials and the integration capability of silicon. Moreover, the difficulty of coupling to silicon-based passive optical devices is overcome by confining most of the optical mode to the silicon. This approach restricts laser operation to the region defined by the silicon waveguide. Park et al. [108] reported the first demonstration of a silicon evanescently coupled laser operating at a wavelength of 1538 nm with an optically pumped threshold of 30 mW and a maximum power output of 1.4 mW. The calculated and observed optical modes for this remarkable device are shown in Fig. 20. Fang et al. then demonstrated an electrically pumped hybrid laser with a threshold of 65 mA and output power of 1.8 mW [109]. Distributed feedback lasers [136], racetrack-resonator lasers with output power as high as 29 mW [54] (the highest output power demonstrated from a silicon evanescent laser to date), tunable lasers [137], mode-locked lasers [55], lasers operating around 1310 nm [138], and micro-ring lasers [56] have since been demonstrated with the hybrid platform. The interested reader may find these advances specifically reviewed elsewhere [139]. This work spurred a significant research effort in hybridization, which holds great promise as a method for the introduction of virtually any optical functionality (including high-performance detection) using a CMOS compatible approach.

A recent and significant development in the quest for an optical source which can be fabricated in a CMOS compatible process flow is the demonstration of optical gain in a SiGe device. The culmination of a volume of work led to a report by the MIT research group in 2010 which demonstrated optically pumped lasing from a germanium waveguide grown directly on a silicon substrate [140]. The device relies upon strain and doping in the germanium waveguide to induce direct bandgap transitions at room temperature. Figure 21 shows the device and optical output characteristics as a function of pump power and output wavelength. The pumping threshold for gain is estimated to be 5–6μJ, and at around 1590nm it is compatible with silicon photonic circuits. The authors estimate that an equivalent electrical injection current of several kAcm^{-2} is required to induce electrically pumped lasing.

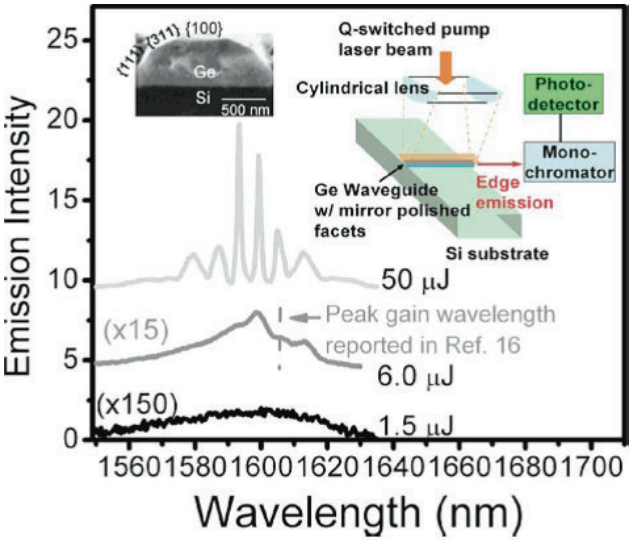

Figure 21 (online color at: www.lpr-journal.org) Optically pumped spectrum obtained from a Ge-on-Si waveguide laser. The inset show a schematic of the device and an SEM reproduction of the Ge waveguide section. Reproduced from [140].

It is appropriate to acknowledge here the landmark work from the group of Bahram Jalali at UCLA [141]. They showed the first lasing in a silicon waveguide, working on the principle of the Raman effect. Silicon exhibits a particularly strong Raman effect which allows gain to be observed on the chip scale. Subsequent work showed continuous wave pumping through the integration of a p-i-n diode [142], shown in Fig. 22. The device permitted the removal of free carriers created via the two photon absorption effect and resulted in an operating characteristic described by Fig. 23. Although it is difficult to envisage the use of the Raman laser as a primary optical source, its wide tunability and primary demonstration of gain suggests it will continue to be an important component in silicon photonics.

The final methodology listed in this section is the approach of direct growth of a III-V laser on a silicon platform. Despite decades of work to achieve seamless integration in this manner [143], the realization of long wavelength lasers

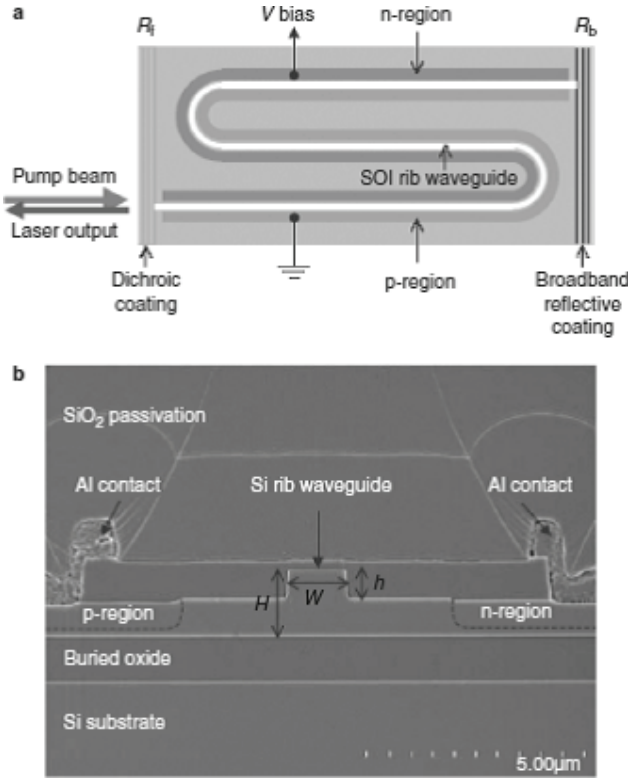

Figure 22 Schematic representation (a) and electron micrograph (b) of a Raman silicon laser with integrated p-i-n diode to sweep away free carriers. Reprinted by permission from Macmillan Publishers Ltd. [142], copyright (2005).

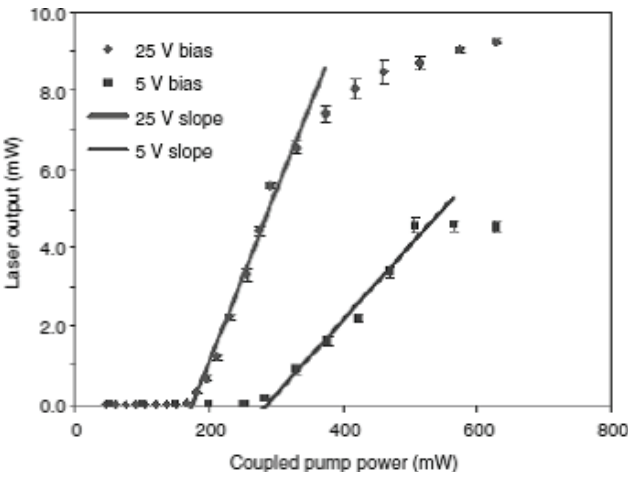

Figure 23 Optical output obtained from the device shown in Fig. 22. Reprinted by permission from Macmillan Publishers Ltd. [142], copyright (2005).

operating at room temperature is only just becoming a reality. A recent report of laser operation resulting from the direct growth of InAs/GaAs quantum dots on a germanium substrate has suggested a route to this end. Liu et al. [144] have reported lasing at a wavelength of 1305nm with a threshold current density of 55.2 A cm^{-2}; performance com-

parable to that obtained from devices grown on GaAs. These types of device have the potential for lasing at a range of wavelengths and as discussed elsewhere in this review their growth on Ge likely makes their fabrication on Ge on Si substrates possible. Although more work is required to fully prove these lasers in a complex silicon photonic circuit, it is exciting to anticipate all photonic functionality may soon be fabricated using standard tool-sets.

4.2. Modulators

Optical transmission can employ either direct modulation (i. e. the optical source is modulated) or external modulation (i. e. the continuous-wave source output is separately modulated downstream from the source). The latter is generally preferable owing to reduced cost for the source and the avoidance of redundant wavelength stabilization on multiple devices and will be the focus of this section.

Unlike traditional modulator substrates such as $LiNbO_3$, silicon has no Pockels effect available for electro-optic modulation due to the centro-symmetry of the crystal lattice, and both the Kerr and Franz-Keldysh effects are small at standard telecommunication wavelengths [145]. Instead modulation in silicon is generally accomplished using either electro-absorption or electro-refraction via changes in the free carrier density. The latter approach is typically implemented using either a Mach-Zehnder interferometer (MZI) or a resonant structure. In an MZI structure the optical input is divided along two waveguide branches and then recombined such that phase modulation in either branch is converted into amplitude modulation at the output. In a resonant structure (e. g. a ring resonator) the resonant wavelength can be varied by altering the effective refractive index, and hence the optical path length, within the resonator. Modulators based on a resonant or photonic crystal structure offer the advantage of compactness and often higher extinction ratios relative to MZI devices but suffer from inherent bandwidth limitations due to the narrow spectral width of the resonance.

The change in refractive index and absorption as quantified by Soref and Bennet [145] for 1.55 μm wavelengths in silicon are given Eq. (6) and Eq. (7) respectively:

$$\Delta n = -\left(e\lambda/2\pi c\right)^2 \left(2\varepsilon_0 n\right)\left(\Delta N_e/m_{ce}^* + \Delta N_h/m_{ch}^*\right), \quad (6)$$

$$\Delta\alpha = \left(e\lambda/2\pi c\right)^2 \left(ec\varepsilon_0 n\right) \times \left(\Delta N_e/{m_{ce}^*}^2\mu_e + \Delta N_h/{m_{ch}^*}^2\mu_h\right) \quad (7)$$

where e is electron charge, λ is free-space wavelength, n is refractive index, ε_0 is the vacuum permittivity, μ_e and μ_h are the electron and hole mobility , m_{ce}^* and m_{ch}^* are the conductivity effective masses of electrons and holes, and N_e and N_h are the concentrations of free electrons and free holes.

Free-carrier concentration can be varied either by injection, depletion, or accumulation. Schematic diagrams of the devices associated with each of these three modulation approaches are shown in Fig. 24. It should be noted that although each is shown with a transverse diode geometry, it is entirely possible and sometimes advantageous – particularly from the standpoint of planar processing steps – to orient the diode vertically such that barrier dielectrics and dopant layers are fashioned as horizontal planar layers during fabrication.

Injection is accomplished by applying forward bias to a p-i-n diode straddling the waveguide such that electrons and holes are injected into the junction. This approach was first demonstrated by Treyz et al. [146] in the form of an electro-absorption modulator with an extinction ratio of 6.2 dB and transition time of 50 ns. Similar devices which use a FET structure to draw injected current into high overlap with the guided optical mode have also been demonstrated [147]. Since the waveguide can often be flooded with carriers at concentrations exceeding 10^{18} cm^{-3}, this approach yields high modulation depth with relatively short length, but suffers from bandwidth limitations due to minority carrier lifetime.

Also demonstrated by Treyz was an MZI electro-refraction modulator [148] using carrier injection to induce phase shift. Several improvements based on this approach have been reported, achieving speeds on the order of 10–20 MHz [149, 150]. By incorporating the MZI in a photonic crystal structure (a scheme described in Sect. 3), the "slow light" effect can be leveraged to enhance the interaction between injected carriers and the optical mode, thus enabling modulation at gigahertz speeds in a compact form factor [151].

Carrier injection in resonant cavities has been accomplished using both photonic crystals [152, 153] and ring

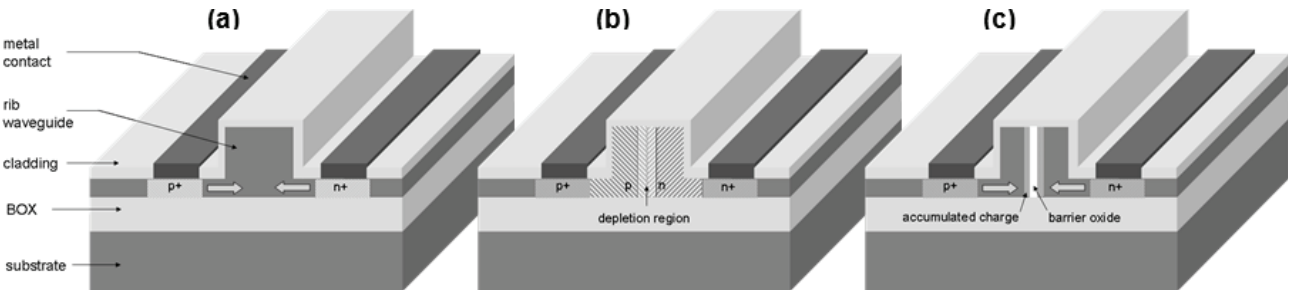

Figure 24 Optical modulation in a silicon rib waveguide via the plasma dispersion effect using (a) free-carrier injection, (b) free-carrier depletion, and (c) free-carrier accumulation.

resonators [67, 154–157], and together with the use of reverse bias pulses to extract free carriers, modulation speeds as high as 18 Gb/s have been achieved [155].

An alternative to carrier injection is carrier depletion: a p-n or p^+pnn^+ junction is reverse biased such that the width of the space-charge region (i. e. the region depleted of free carriers), and hence its overlap with the optical mode, is varied. Since outside the space-charge region the free-carrier concentration is approximately equivalent to the dopant concentration while inside it the free-carrier concentration is approximately zero, modulation of the effective index is accomplished. In order for the change in depletion width to be significant at practical bias voltage levels, however, the dopant concentration within the space-charge region cannot generally be as high as that achieved by free-carrier injection. Carrier depletion modulation is therefore less efficient than carrier injection, but has the comparative advantage of being independent of minority carrier lifetime and can achieve higher modulation speeds despite the size increase and concomitant *RC* limitations imposed by the reduction in modulation efficiency. This tradeoff was well illustrated by Spector et al. [158] who demonstrated a MZI modulator that could be operated in either carrier injection or depletion mode, with a bandwidth of 100 MHz and voltage-length product ($V_\pi L$) of 0.0025 V-cm in current injection mode (i. e. forward biased) and a bandwidth of 26 GHz with $V_\pi L$ of 4 V-cm in carrier depletion mode (i. e. reverse biased).

Carrier depletion modulators were first proposed by Gardes et al. in 2005 [159] and demonstrated within a MZI by Liu et al. in 2007 [160] with speeds in excess of 20 GHz, and shortly thereafter with speeds in excess of 30 GHz, with operation up to 40 Gb/s and efficiency of $4V_\pi$ cm [161]. The latter is illustrated in Fig. 25 and is the fastest monolithic silicon modulator demonstrated to date. Similar devices were subsequently reported with improved $V_\pi L$ of 1.8 V-cm [162] and 1.4 V-cm [163] at 12.5 Gb/s.

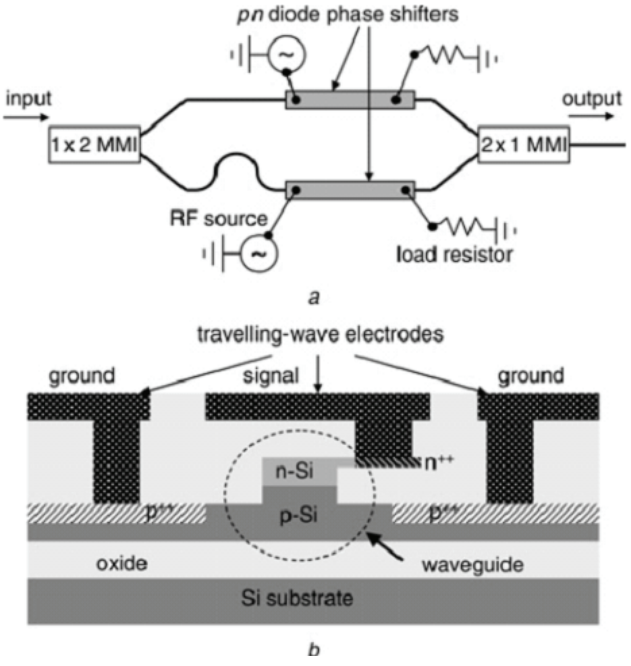

Figure 25 Schematic top-view and cross-section diagrams of the device reported in [161]. Reproduced from [161].

Ring resonators have been used to overcome the efficiency disadvantage associated with carrier depletion modulators and thereby reduce the overall device footprint [63,64,69] to less than 1000 µm [2] with a drive voltage of 2.2 V_{pp} [63]; this device is shown in Fig. 26.

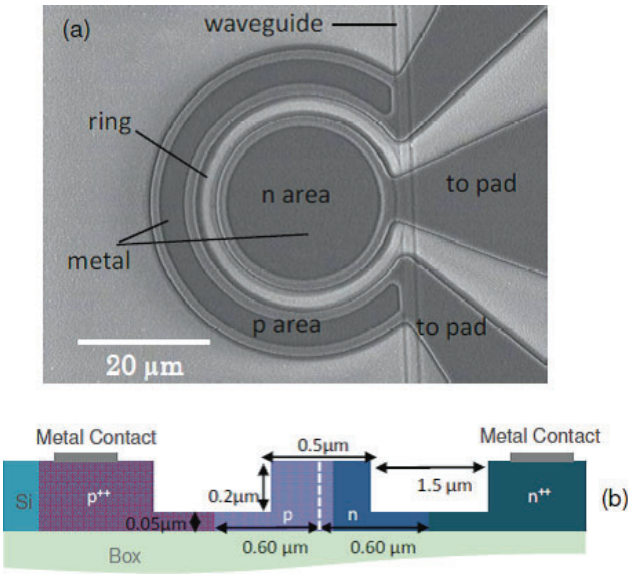

Figure 26 (online color at: www.lpr-journal.org) SEM image and schematic cross-section of the device described by Dong et al. Reproduced from [63].

A third approach to modulation is carrier accumulation, in which an insulating barrier is incorporated into the waveguide to form a capacitor which accumulates charge under applied bias. This architecture was demonstrated by Intel Corp. in an MZI and was the first modulator to achieve operation at speeds in excess of 1 GHz [16], and later 10 GHz operation by means of improvements in optical mode overlap with the charge accumulation and in driver circuitry [164].

Modulation can also be accomplished using various non-standard CMOS processes to take advantage of nonlinear effects not normally feasible in silicon such as the Kerr effect in a silicon-polymer hybrid [165], the Pockels effect in strained silicon [166] and the quantum-confined Stark effect [167] or Franz-Keldysh effect [168] in silicon-germanium. The case for the latter can be made on the basis that other such devices such as high-speed photodetectors may already be integrated on the chip, and therefore the fabrication complexity of a silicon-germanium modulator comes without additional cost. This argument can be extended to the hybrid integration of III-V materials which may already be in use on the chip for integrated lasing and amplification. Beyond its compatibility with hybrid gain elements on the chip, advantages of such an approach are the contribution of band-filling, Kerr, and even Pockels (with proper crystal orientation) effects to the refractive index change in a multiple-quantum-well structure as carriers

are depleted. Modulators employing III-V integration have been demonstrated using micro-disk cavities [165], electroabsorption [170, 171], and MZI structures [172], with the best performance to date reported for an electroabsorption modulator by Tang et al. of 42 GHz 3 dB bandwidth, operation at 50 Gb/s, extinction ratio of 9.8 dB, and a drive voltage of 2 V [171].

4.3. Photodetectors

The development of power monitoring presents one of the key challenges for integrated optical communication technology. The facilitation of signal interrogation requires the capability for efficient optical to electrical conversion. Clearly, it is desirable that the optical signal is carried at a sub-bandgap wavelength to avoid significant on-chip attenuation; however, this would imply virtually zero responsivity for monolithically integrated detectors or optical monitors. Research currently in progress then attempts to reconcile this contradiction in performance specification.

There are three approaches for the integration of detectors in silicon photonics: (1) hybrid integration; (2) Ge growth; (3) defect mediated detection. The processing technology associated with these three approaches has been discussed in Sect. 3.

The recent use of direct bonding of III-V materials for signal generation has been discussed. It is perhaps an obvious step to use the same approach to integrate sub-band detectors. Indeed, this has been demonstrated by the same collaboration led by UCSB which developed the hybrid silicon laser [173].

The approach to detection which has attracted most attention is the use of the direct growth of germanium on the SOI waveguide structure. Germanium based detection is the solution that has to date been adopted by many research groups. Morse et al. described the fabrication process for a Ge-on-Si photodetector [174]. Epitaxial Ge films were grown on a p-type silicon substrate in a commercial CVD reactor. The initial optical characterization of the fabricated devices was performed at 850 nm, with emphasis being placed on the detector performance relative to commercially available GaAs structures. The responsivity was found to saturate for a Ge film thickness of 1.5 µm at 0.6 A/W. The bandwidth was determined to be $\sim$9 GHz.

The same group has also led attempts to integrate Ge detectors with SOI waveguides [175]. Their report of a detector with a bandwidth of 31 GHz is of some significance. A Ge layer was grown on top of a SOI waveguide. The detector was shown to have a repsonsivity of 0.89 AW^{-1} at a wavelength of 1550 nm, while the dark current was limited to 169 nA. An electron micrograph of the device is shown in Fig. 27. Although the current detector design appears limited to terminal detection, one might imagine how these devices could be used to couple fractions of an optical signal for monitoring purposes. Other groups have also demonstrated efficient, high bandwidth (>40GHz) detection of wavelengths around 1550nm [176] and it is generally accepted that Ge-on-Si will dominate for high

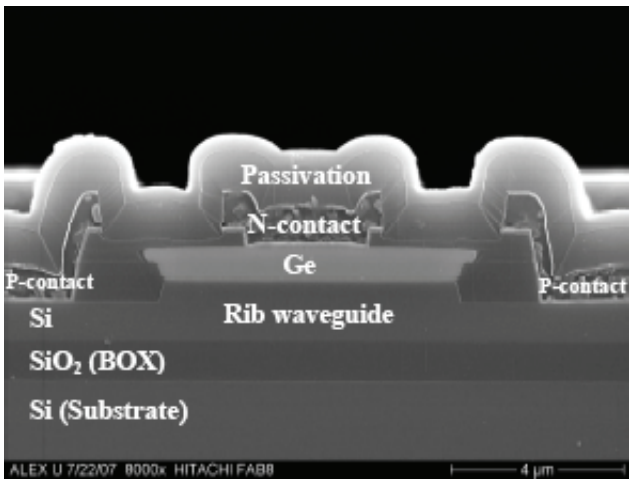

Figure 27 Cross-sectional SEM of the Intel germanium/SOI detector. Reproduced from [175].

performance requirements, particularly as the processing issues associated with direct growth are addressed.

A relatively straightforward solution to integrated detection has been pioneered by the McMaster University Silicon Photonics research group, based upon the absorption of sub-bandgap light via defect states introduced by selective ion implantation. Work by the McMaster group has led to the development of a waveguide detector suited to tapping a small fraction of an optical signal while allowing the vast majority of the signal to pass unaffected—this device then forms the basis of an almost perfect "tap monitor" providing signals that permit a "health check" on an optical circuit, or allowing the electrical signal to be used elsewhere in the same integrated circuit [120]. The advantage of this approach is highlighted by the fact that the detectors were formed by the modification of a commercial product- the Variable Optical Attenuator which is manufactured by Kotura Inc.

A small volume of work has focused on the use of such defect detectors for performance at high speed and with high responsivity. This has been led by the group at Lincoln Labs at MIT. Scaling defect mediated detectors to the submicron level, they were able to show responsivity concomitant with the reduction in size [177, 178]. A 3 mm long detector was reported to absorb 99% of the incident light at a wavelength of 1545 nm. At a reverse bias of 25 V, the responsivity exceeds unity quantum efficiency, indicating carrier multiplication in the strong electric field. The authors demonstrated the thermal stability of these devices (tentatively associated with the presence of oxygen), showing that annealing at 300°C increased the detector responsivity. Perhaps the most important result from this work is that associated with bandwidth. For a detector of length 250 µm, the frequency response was measured using a vector network analyzer and an optical modulator capable of 50 GHz operation. The half-power point of the detector frequency response after correcting for the frequency response of the modulator was approximately 20 GHz.

In an attempt to reduce the physical size of defect mediated detectors, work has been reported on the incorpora-

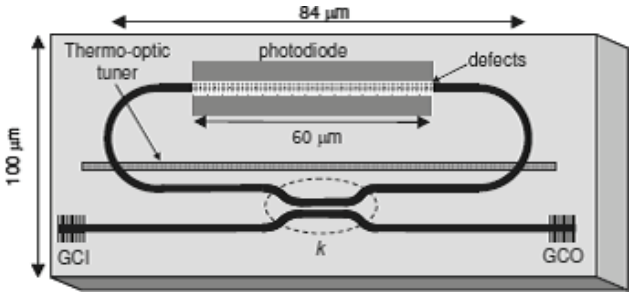

Figure 28 Schematic diagram of a resonant enhanced defect mediated detector. GCI/GCO indicate grating coupled input and output. Reproduced from [59].

tion of these detectors in resonant structures. For example, Doylend et al. used optical lithography to fabricate ring resonant detectors in which boron implantation was used to introduce defects [59], whereas, Logan et al. utilized electron beam lithography and inert silicon ion implantation to create deep-levels to facilitate the detection process [60]. A schematic of the device used by Doylend et al. is reproduced in Fig. 28. In that case, a detector of physical length of 60 µm resulted in responsivity of 0.12 A/W for wavelengths around 1550 nm, with an associated dark current of only 0.2 nA. Further, the detected wavelength was tuned across the entire free spectral range using an integrated heater, implying sensitivity to wavelengths through the entire *C*-band. The response as a function of tuned wavelength is shown in Fig. 29.

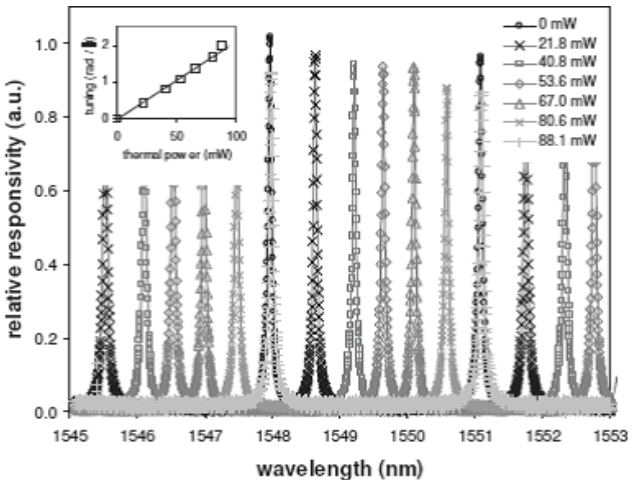

Figure 29 Response of a resonant defect mediated detector. The inset indicates the efficiency of the integrated heater which permits tuning of the response to any wavelength within the *C*-band. Reproduced from [59].

4.4. Integration

Historically, the adoption of optics into the domain of electrical data transmission has always begun with the longest distance links, and silicon photonics is no exception. The need for optical links is more immediately apparent for chip-to-chip than intra-chip interconnects due to the larger data traffic requirements of a transmission artery together with higher price-point. The electro-optical conversion, however, must either be performed off-chip and employ a relatively large, high-bandwidth electrical interconnect between the chip and the opto-electronic module which cannot avoid the problems described above, or must be integrated on-chip. On-chip photonic integration can therefore provide significant throughput advantages together with reduced power consumption [179] and so the integration of multiple active and passive devices within a single planar optical circuit is thus a key requirement to maximize the advantages of silicon photonics. A schematic of one such approach put forward by IBM is shown in Fig. 30 [180].

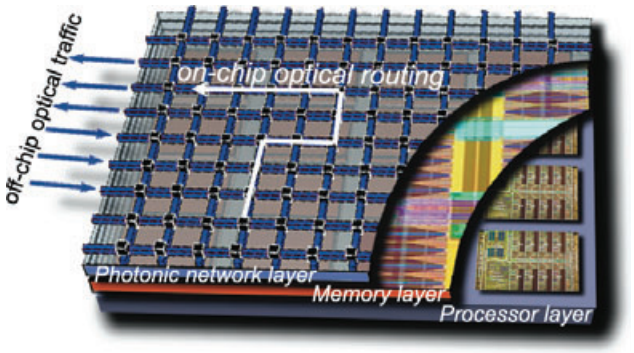

Figure 30 (online color at: www.lpr-journal.org) On-chip optical interconnects using a photonic network layer as envisioned by IBM. Courtesy of International Business Machines Corporation, © 2011 International Business Machines Corporation.

Although a variety of discrete optical devices have been developed in silicon over the past decade, it is only within the last several years that integration of multiple functions together on-chip has been demonstrated. A complete photonic link using flip-chip bonded integration of III-V lasers with on-chip modulators and germanium-based photodetectors was demonstrated by Luxtera in 2006 [181] and later commercialized. Luxtera has since demonstrated 40 GB/s optical transceivers with all functions integrated in silicon on a standard CMOS line other than the flip-chip bonded optical source [182].

The hybrid platform [112] has also been used to accomplish multi-function integration of sources with photodetectors [54] and with modulators [183] in photonic circuits. Since this approach involves bonding III-V substrates to a defined silicon device the fabrication of photodetectors as well as lasers and amplifiers adds little or no additional processing complexity. This technique is currently the only approach which can provide on-chip sources without the need for precise optical alignment and soldering of discrete elements during bonding and is therefore particularly promising.

Truly monolithic integration without bonding either discrete devices or additional substrates is limited insofar as

there is currently no means of fabricating an on-chip optical source within silicon. However an optical link has been demonstrated at 3 Gb/s using ring resonator modulators and germanium photodiodes [62]. Control of an optical signal using an integrated current-injection variable optical attenuator and a germanium photodiode [184] as well as defect-enhanced all-silicon photodiodes [59, 185, 186] has been reported, with the devices demonstrated as an automated dynamic channel-leveller [185]. In a notable demonstration of true electro-optic integration, a CMOS modulator together with its driver circuitry were recently fabricated monolithically and operated at 5 GB/s [187], indicating that the age of true photonic integration with CMOS circuitry is perhaps finally here.

5. Concluding remarks

This review has discussed recent developments in silicon photonics with specific emphasis on devices and processing strategies. The development of the present generation of functionality has evolved from that associated with relatively large waveguides prior to 2003 (with cross-section of many microns squared) to sub-micron waveguides fabricated using SOI substrates with a silicon film thickness of less than 300 nm. The use of such small dimensions has allowed the fabrication of modulators capable of speeds in excess of many tens of GHz – a crucial development. Necessary advancement in light coupling has seen an evolution from simple 'butt-coupling' to the use of surface gratings which provide for high efficiency of transfer of optical signals from optical fiber to the silicon chip. A further recent advance has been the integration of non-silicon material (such as III-V or germanium) with photonic circuits in a manner compatible with standard device processing. This has allowed the incorporation of any required functionality in a CMOS based device or system. In summary, it is likely that optical interconnection will only grow in importance over the coming decades, and as with other widely deployed semiconductor technologies, that growth will be based primarily on the silicon substrate. The work described in this review and that to emerge in the next few years will be the foundation upon which this remarkable photonic evolution will be based.

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Andrew P. Knights received his Ph. D. in 1995 from the University of East Anglia following research in charged particle interactions with solid surfaces. After post-doctoral positions at the University of Western Ontario and the UK Ion Beam Facility, University of Surrey, he took up a position as Principal Engineer at Bookham Technology in 2000. There he worked with the team that brought the first silicon photonics devices to market. In 2003 he joined the Department of Engineering Physics, McMaster University where he continues to lead a research group in high-level integration of optics and electronics on silicon substrates. He has authored over 150 articles and is a regular contributor at international conferences.

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