*Electrochemical and Solid-State Letters*, **14** (11) H457-H459 (2011)
1099-0062/2011/14(11)/H457/3/$28.00 © The Electrochemical Society



# High Power Density UV Optical Stress for Quality Evaluation of 4H-SiC Epitaxial Layers

**A. Canino,[z] M. Camarda, and F. La Via**

*Consiglio Nazionale delle Ricerche, Istituto di Microelettronica e Microsistemi, Z.I. VIII strada, 95121 Catania, Italy*

We present a characterization technique to assess the quality of 4H-SiC CVD growth process based on optical methods. The setup allows characterizing the epilayer and the substrate at the same time, leading to a self-consistent determination of the epitaxial layer quality with respect to the substrate. By using high power density UV optical pumping to stress 4H-SiC epitaxial layers, we are able to check the generation and evolution of Single Shockley faults on large areas, without fabricating bipolar junctions. This characterization technique is a fast and non-destructive method to compare the quality of different 4H-SiC CVD growth process.
 [DOI: 10.1149/2.014111esl] 

Manuscript submitted February 24, 2011; revised manuscript received July 26, 2011. Published September 23, 2011. This was Paper 1478 presented at the Montreal, QC, Canada Meeting of the Society May 1–6, 2011.

Silicon Carbide (SiC) is a material of great interest for the manufacturing of devices, as it can achieve excellent performance in high-power and high-frequency electronics and in harsh environment applications such as high-temperature or space applications.[1]

The growth of high quality 4H-SiC epitaxial layers is one of the main steps of the device manufacture. The "step-controlled epitaxy"[2] allows to reach a reduction of growth temperature and a higher quality of epilayers. Unfortunately, the growth on off-axis substrate implies the exposition of basal planes on the surface and, as a consequence, leads to the possible propagation of stacking faults and basal plane dislocations (BPDs) from the substrate up to the film surface. In particular, the Single Shockley stacking fault (SSF) is considered as the main responsible of the observed electrical instability of 4H-SiC bipolar devices.[3] It has been demonstrated that a high e-h pairs density (due to current or to high power optical pumping) can supply the energy either to enlarge pre-existing SSFs or to open/generate them.[3–6] The latter mechanism is based on the separation of a perfect BPD into two partial dislocations, a fixed one and a mobile one under UV optical pumping or under a bipolar current stress as shown in the scheme of Fig. 1 .

For high quality 4H-SiC epitaxial layers grown on 4° off-angle substrates, generation and enlargement of SSFs remain the main question to solve in order to improve the stability of bipolar devices. Given an actual BPD surface density in a range between $10^2$ and $10^5$ $cm^{-2}$ for 4H-SiC substrates, it is essential to find a non-destructive characterization technique able to evaluate if the epilayers can be used for the manufacturing of bipolar devices without leading to a progressive degradation of electrical properties.

Whole wafer PL mapping[7] and electro-optical investigations on BPDs structural properties and behaviour[8–12] as well as PL imaging and identification of SFs[13–21] have been widely reported in literature as characterization techniques for the localization of extended defects on both restricted and large areas. These methods either analyze the epilayer or the substrate only[7,21] by mean of non-destructive techniques (optical/electrical) or compare the quality of the epilayers with respect to that of the substrate through molten KOH etching,[22,23] i.e., with destructive methodologies.

In this work we want to evidence the possibility of using optical methods to compare the quality of different CVD growth processes self-consistently (i.e., evaluating the quality of the film with respect to that of the substrate). The idea is to stress at the same time the 4H-SiC epitaxial layer and the substrate in order to monitor the post growth evolution (opening or enlargement) of SSFs. By appropriately using high power density UV optical pumping, it is possible to evaluate both the capability of epitaxial layers to avoid the arising of SSFs after the 4H-SiC CVD growth process, and to simultaneously assess the quality of the substrate. This technique allows to perform an analysis of the stability of epitaxial layers without the manufacturing of any bipolar devices, as PIN diodes, thus resulting in a fast and simple characterization tool.

In particular, spatially resolved micro-photoluminescence (μPL) and spatially resolved optical pumping have been used to map density of SSFs and to irradiate the surface of samples. The pumping source is a He-Cd laser emitting at 325 nm with a power output of 50 mW. The power density can be set in a range between some $W/cm^2$ up to about 2 $kW/cm^2$. To check the epilayers quality, two samples (S1 and S2) grown on 3 inches 4° off-angle substrates with a thickness of about 7 microns have been used. S1 has been grown by using a silane CVD process while S2 has been grown by using a trichlorosilane CVD process with similar growth rate (about 6 micron/h) and are both n-type epilayers with a doping concentration of about $10^{16}$ $at/cm^3$. The aim was to reach the interface with the He-Cd laser emitting at 325 nm (penetration depth of about 7.4 $\mu m$[24]). The SSF has a specific peak of photoluminescence centered at about 2.93 eV at room temperature.

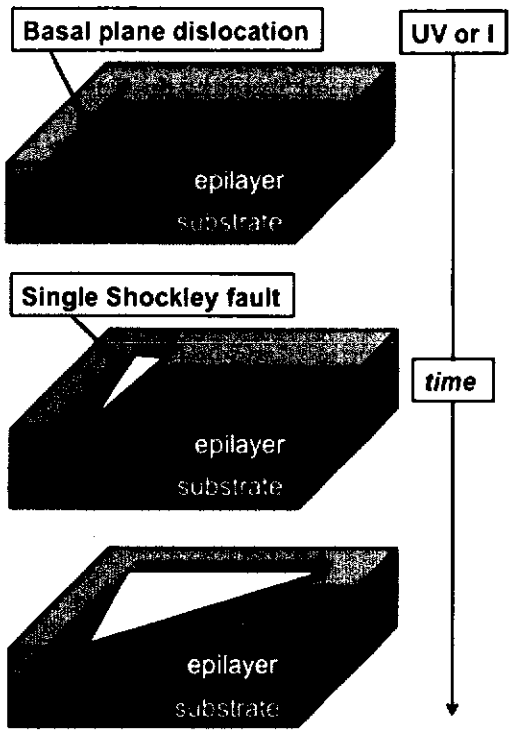


**Figure 1.** (Color online) Schematic view of the conversion of a basal plane dislocation into a SSF. The conversion and the growth of the defect can be caused by an electrical stress (bipolar current flow indicated as I) or by an optical stress (UV irradiation of the sample).

[z] E-mail: andrea.canino@imm.cnr.it

Having set this value of energy, it is possible to map the defect density on the surface by performing a PL map. It has been demonstrated that for a fixed exposure time under a corresponding threshold for the UV power density,[5] it is possible to observe SSFs distribution on a surface without affecting the structural properties of the sample. Consequently, a low power density (about 250 W/cm$^2$) low exposure time (0.1 sec) setup has been used to measure the surface density of SSFs before the stress test by revealing PL signals at 2.93 eV. The same setup has been used to observe the effects after the stress test. By using this experimental setup SSFs are not subjected to any change[5] and their PL signals are very intense while the PL signals due to defects below the interface have intensities too low to be detected.

The stress test is performed on samples by enhancing the power density up to 2 kW/cm$^2$ and the exposure time up to 2 seconds for several repetitions in order to investigate the effect of a high-density plasma of electron-hole couples. The 2 seconds exposure allows reaching and maintaining a steady state condition during which e-h plasma can generate a photo-induced current (corresponding to a current density of about 1000 A/cm$^2$) flowing through the sample. Thus it was possible to verify the epilayers behavior under high stress conditions similar to the operational conditions of bipolar devices. Furthermore, with the chosen setup, i.e. by using 325 nm as pumping source on 7 μm thick samples, it is possible to fully stress the epilayer up to and below the interface with the substrate and therefore, to explore the quality of the substrate itself during high power optical pumping. In these conditions we are able to observe the defects below the interface because the pumping power density is 10 times higher and the integration time is 20 times higher. So even if the PL signals due to defects below the interface have a low intensity, we are able to observe them.

PL signals due to the SSFs are bright spots on a uniform background and exhibit a triangular shape (not shown). This feature allows distinguishing them from $(2,3_3)$ stacking fault that exhibits a similar PL peak centred at about 2.9 eV and a typical bar shape.[17] Moreover $(2,3_3)$ SFs have typical dimension of several hundreds microns on the direction normal to growth direction.[11-20] On the PL map reported in Fig. 2 it is possible to observe the difference between the two different defects. Moreover whole wafer PL mapping allows evidencing high defective areas.

To perform the stress test, restricted representative areas of our samples have been considered. These areas have a dimension of about 0.5 cm$^2$. Fig. 3a and 3d show the initial SSF μPL maps of S1 and S2. The 2 different samples show a marked difference in the initial value of SSF density. This difference, without any other information, can be attributed to the process and/or to the quality of the substrate.

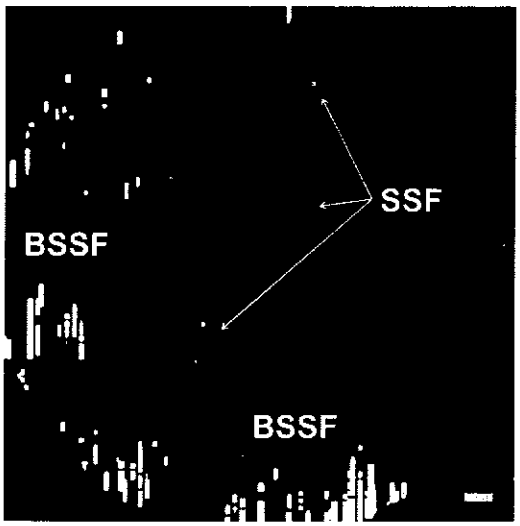


**Figure 2.** (Color online) (a) PL map at room temperature of a 3″ wafers. Bright spots are PL signals at 2.93 eV recorded at room temperature due to the SSFs and bar shaped bright lines are due to BSSFs emitting at about 2.9 eV.

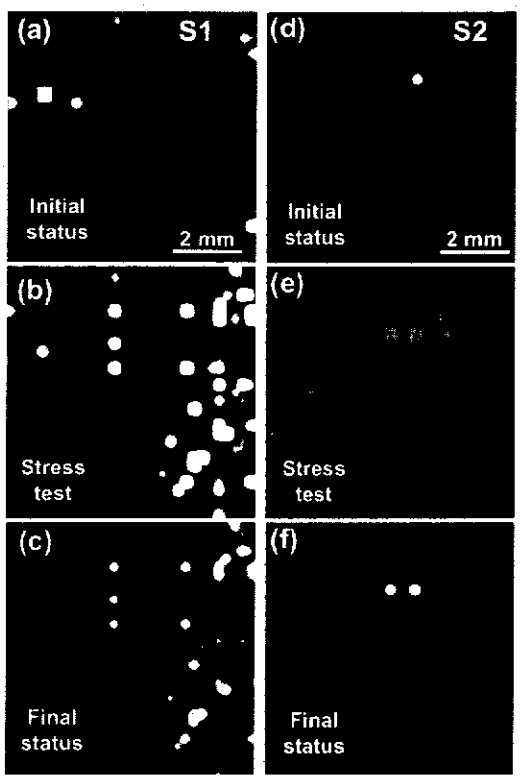


**Figure 3.** (a) and (e) Low power density (about 250 W/cm$^2$) low exposure time (0.1 sec) micro-photoluminescence maps of SSFs obtained by revealing the 2.93 eV peak of the defect. Bright spots are SSF. (b) and (e) High power density (about 2 kW/cm$^2$) long exposure time (2 sec × 10 times) micro-photoluminescence map of the same area. (c) and (f) Low power density (about 250 W/cm$^2$) low exposure time (0.1 sec) micro-photoluminescence map of the same area to verify the stress test effects.

The stress test has been performed on the same areas, recording in the same time the PL signals due to SSFs. On Fig. 3b and 3e it is possible to observe several signals due to the SSFs. These signals are due to defects both inside the epilayers and inside the substrates under the interface with the epilayer. The density of signals visible in this image is comparable (about 80–100 cm$^{-2}$). This fact allows to assume that the initial status of substrates for S1 and S2 is comparable. We can also assume that BPDs present inside the epitaxial layers or at the film/substrate interface have been dissociated, due to the high power density UV exposure, into 2 partial dislocations leading to the formation of several SSFs, showing a progressive degradation of the samples.

In Fig. 3c and 3f, the stress test effects on S1 and S2 can be compared. These two PL maps have been obtained by using again the low power density and low exposure time conditions, observing thus the defects which are present inside epilayers only. On S1 several SSFs are now visible also with the low power density PL mapping setup (Fig. 3c). As far as S2 is concerned, almost all of these signals are absent in the final PL map (Fig. 3f). This is the evidence that it is possible to avoid the propagation of defects inside the epilayers even if they are present in the substrate by changing the CVD process.

By comparing the stress test results for the two samples (see Fig. 4 ), it is possible to conclude that, being more resistant to SSF evolution under stress conditions, the second epitaxial layer (S2) has a higher stability than the first (S1). The stress test allows a self-consistent evaluation of 4H SiC epitaxial layers quality before the beginning of bipolar devices production.

In conclusion, the method used allows a self-consistent evaluation of quality of the epilayer with respect to the substrate and to perform

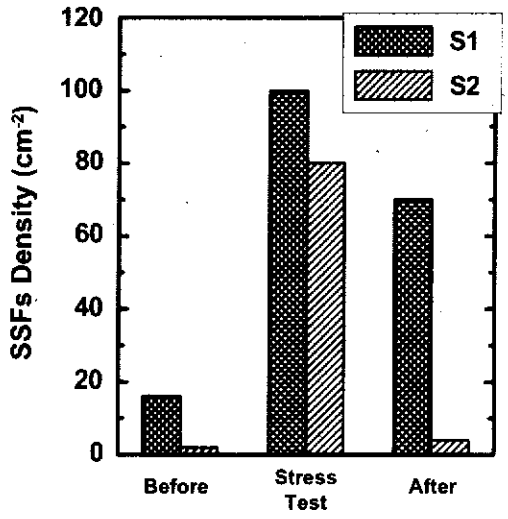


**Figure 4.** (Color online) In this graph, the remarkable difference in the behaviour of S1 and S2 epitaxial layers is visible, despite the stress test evidences a similar SSFs density on substrates. S2 shows a higher stability under stress condition than S1 resulting in a lower final density of of SSFs, i.e., in a higher quality epilayer and thus in higher quality of the CVD process.

a stability test on thin 4H SiC epitaxial layers by using high power density UV optical stress. This technique allows to verify directly the capability of epilayers to avoid the post growth evolution of SSFs and to evaluate, directly and fast, the epilayers stability without the production of PIN diodes on the wafer. Thanks to this characterization method it is possible to choose accurately the CVD process for the growth of epitaxial layers without processing the wafers. This is a fundamental step for the manufacturing of efficient bipolar devices and to obtain a better yield of devices on single wafer.

## Acknowledgments

Ms Oriana Antichi for proofreading the text.

## References

1. H. Matsunami and T. Kimoto, *Mater. Sci. Eng. R.*, **20**, 125 (1997).
2. N. Karoda, K. Shibahara, W. S. Yoo, S. Nishino, and H. Matsunami, *Extended Abstract, 19th Conference on Solid State Devices and Materials*, Tokyo, 227 (1987).
3. M. Skowronski and S. Ha, *J. Appl. Phys.*, **99**, 011101 (2006).
4. T. Miyanegi, H. Tsuchida, I. Kamata, T. Nakamura,, K. Nakayama, R. Ishii, and Y. Sugawara, *Appl. Phys. Lett.*, **89**, 062104 (2006).
5. A. Canino, M. Camarda, and F. La Via, *Mater. Sci. Forum*, **645–648**, 555–558 (2010).
6. G. Feng, J. Suda, and T. Kimoto, *Jpn J. Appl. Phys.*, **49**, 090201 (2010).
7. R. E. Stahlbush, K. X. Liu, Q. Zhang, and J. J. Sumakeris, *Mater. Sci. Forum*, **556–557**, 295–295 (2007).
8. X. Zhang and M. Skowronski, K. X. Liu, R. E. Stahlbush, J. J. Sumakeris, M. J. Paisley, and M. J. O'Loughlin, *J. Appl. Phys.*, **102**, 093520 (2007).
9. Y. N. Picard, K. X. Liu, R. E. Stahlbush, M. E. Twigg, X. Zhang, and M. Skowronski, *J. Appl. Phys.*, **103**, 074904 (2008).
10. A. Galeckas, J. Linnros, and P. Pirouz, *Mater. Sci. Forum*, **433–436**, 933–936 (2003).
11. M. E. Twigg, R. E. Stahlbush, M. Fatemi, S. D. Arthur, J. B. Fedison, J. B. Tucker, and S. Wang, *Appl. Phys. Lett.*, **82**, 2410 (2003).
12. N. Hoshino, M. Tajima, M. Naitoh, E. Okuno, and S. Onda, *Mater. Sci. Forum*, **600–603**, 349 (2009).
13. S. Izumi, H. Tsuchida, I. Kamata, and K. Izumi, *Appl. Phys. Lett.*, **86**, 202108 (2005).
14. G. Feng, J. Suda, and T. Kimoto, *Appl. Phys. Lett.*, **92**, 221906 (2008).
15. G. Feng, J. Suda, and T. Kimoto, *Appl. Phys. Lett.*, **94**, 091910 (2009).
16. J. Hassan, A. Henry, I. G. Ivanov, and J. P. Bergman, *J. Appl. Phys.*, **105**, 123513 (2009).
17. M. Camarda, A. Canino, A. La Magna, F. La Via, G. Feng, T. Kimoto, M. Aoki, and H. Kawanowa, *Appl. Phys. Lett.*, **98**, 051915 (2011).
18. H. Iwata, U. Lindefelt, S. Öberg, and P. R. Briddon, *J. Appl. Phys.*, **93**, 1577 (2003).
19. T. Robert, M. Marinova, S. Juillaguet, A. Henry, E. K. Polychroniadis, and J. Camassel, *Mater. Sci. Forum*, **645–648**, 347 (2010).
20. G. Feng, J. Suda, and T. Kimoto, *Physica B*, **404**, 4745 (2009).
21. M. Camarda, A. La Magna, P. Delugas, and F. La Via, *Appl. Phys. Exp.*, **4**, 025802 (2011).
22. R. E. Stahlbush, B. L. VanMil, R. L. Myers-Ward, K-K. Lew, D. K. Gaskill, and C. R. Eddy, *Appl. Phys. Lett.*, **94**, 041916 (2009).
23. Z. Zhang and T. S. Sudarshan, *Appl. Phys. Lett.*, **87**, 151913 (2005).
24. S. G. Sridhara, R. P. Devaty, and W. J. Choyke, *J. Appl. Phys.*, **84**, 2963 (1998).