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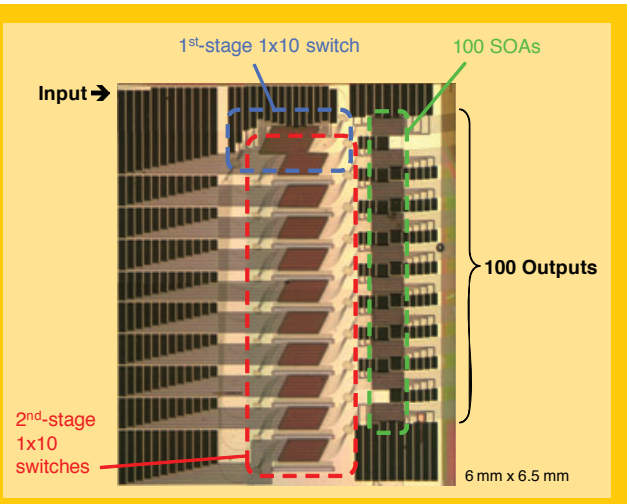
LASER & PHOTONICS REVIEWS

Abstract Integrated phased-array optical switches, having a high port-count scalability and broad spectral coverage, can potentially be used as building blocks of large-scale optical routers. In this article, recent works on monolithically integrated InP phased-array switches and their applications to optical packet switching (OPS) are reviewed. After describing the theory of integrated phased-array switches, experimental results on a single-stage 1×16 switch, which features wavelength-independent nanosecond switching characteristics, are presented. A series of OPS experiments, employing high-bit-rate optical packets with different modulation formats and a tunable optical buffering experiment are presented as potential applications of these switches. Finally, a large-scale monolithic switch with as many as 100 ports is realized on a single photonic integrated circuit by cascading the phased-array switches.



Integrated phased-array switches for large-scale photonic routing on chip

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1. Introduction

The information age has caused a dramatic increase of the data traffic in communication networks in the last two decades. The global internet protocol (IP) traffic is estimated to continue growing with an annual rate of 32% in the near future [1]. This rapid increase of traffic necessitates capacity upgrades, which have been achieved by scaling up the links and network equipments up to now. However, this approach is facing fundamental limitations, set in particular by the power consumption. Conventional routers utilize electronic switching, which requires bit-by-bit processing along with optical/electrical/optical conversion, multiplexing and demultiplexing. As an alternative technology, optical switching may potentially achieve higher energy efficiency than electric switching by bypassing the optical/electrical/optical conversion and multiplexing/demultiplexing processes, and by routing high-bit-rate data transparently instead of bit-by-bit switching [2–4].

Optical packet switching (OPS) is of particular interest because of its high granularity, which is especially important in the present network conditions dominated by the IP traffic. In spite of these advantages, OPS has been very demanding in terms of optical device technologies. The switching components have to operate with high reconfiguration speed (typically of the order of picoseconds to a few nanoseconds) and port-count scalability up to several hundreds. Large-capacity optical buffers, which are required for the contention resolution as well as synchronization of incoming packets, impose another technical challenge that has not yet been solved. Several articles on OPS have mentioned these difficulties. For example, Furukawa et al. [5] have reported a 2×2 packet switching node with a high bit rate of 640 Gb/s (64×10 Gb/s) per port, but the authors state the difficulty of scaling the port count because of the high insertion loss of $(Pb,La)(Zr,Ti)O_3$ (PLZT) switches. In another project, a 64×128 switch fabric was built from discrete semiconductor optical amplifiers (SOAs) for optical interconnection in high-performance computers. Strict design specifications, including the low latency, were achieved [6]. However, a cost advantage compared to electric switching was not achieved because the switch fabric was made of a large number of discrete optical components [7].

To construct an OPS router with the data capacity of 1 Pb/s, an optical switching fabric with as many as 25 000 input/output ports is necessary if we assume a line rate of 40 Gb/s per port. The number of ports can be reduced to several hundred if we use broadband optical switches and wavelength-division- multiplexed (WDM) optical packets. In either case, compact, low-cost, low-power, and scalable optical switching circuits are mandatory and the photonic integration is the only possible solution to meet these requirements. The conventional approach to building an $N \times N$ switch matrix is cascading several 1×2 or 2×2 switches

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in crossbar or tree architectures [8, 9]. Cascading a large number of this type of switches, however, faces difficulties in terms of the optical insertion loss and footprint.

Two of the most investigated types of switches that can reach more than two ports in a single stage are the broadcast-and-select (BS) SOA gate array switches and the wavelength-routing switches. The BS switches broadcast the input signal to multiple output waveguides and control the power of individual waveguides via the SOAs attached on them. They have several advantages, such as large extinction ratio, relatively simple control circuits, broadband and modulation-transparent operation, and broadcast/multicast capabilities. Recently, an integrated 16×16 switch matrix has been realized on InP using this scheme [10]. There have been a number of separate experiments on packet switching using BS switches, some including large-capacity WDM packets [11–15]. A serious drawback of these switches is the optical loss in the broadcast section of the device, which increases linearly with the number of ports. As a result, the estimated power consumption of these switches is relatively high in the case of a large number of ports [16].

The wavelength-routing switches, on the other hand, operate by first converting the wavelength of the input signal and then forwarding the wavelength-converted signal to an arrayed waveguide grating (AWG) [17–22]. These switches have an excellent degree of port-count scalability and can achieve $N \times N$ switching in a single stage. Recently, a monolithically integrated 8×8 switch matrix has been demonstrated by integrating tunable wavelength converters and an 8-port AWG on a single InP chip [22]. While these devices are promising, owing to their high port-count scalability, the bit rate and modulation format of the optical signal are critically dependent on the available wavelength-conversion technology, which may limit their applicability in some systems.

As an alternative approach to the above technologies, we have recently investigated optical phased-array switches, which exhibit multichannel broadband operation as well as moderately high port-count scalability [23–32]. The present article reviews the recent research progresses on fabrication of these switches and their applications to OPS subsystems.

The paper is organized as follows. Section 2 introduces the concept of integrated phased-array optical switch and explains the principle of operation and design method. In Sect. 3, we present a single-stage InP 1×16 phased-array switch and its applications to large-capacity optical packet routing and tunable optical buffering. Then in Sect. 4, we present the design and characterization of a 1×100 switching InP photonic integrated circuit (PIC) that consists of a cascade of phased-array switches. Finally, the paper is summarized in Sect. 5.

2. Integrated optical phased-array switch

A phased array is a system that controls the spatial distribution of electromagnetic waves through phase conditions of an array of signals. Arrayed antennas operating at radio frequencies have been the major application of phased arrays up to now. As shown schematically in Fig. 1, integrated optical phased-array switching is accomplished by distributing the optical signal to multiple waveguides using a passive splitter, controlling the phase conditions of individual waveguide modes via phase shifters, and generating the interference of these signals using another passive coupler. This principle can be extended to large numbers of outputs by increasing the number of phase shifters without the necessity of increasing the number of switching stages substantially.

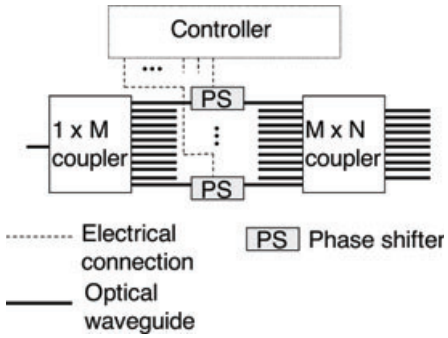

Figure 1 Schematic diagram of $1 \times N$ phased-array optical switches. By applying appropriate phase shift at each waveguide, optical interference pattern at the second coupler can be controlled dynamically to achieve switching to N output ports.

There have been only a limited number of reports on phased-array optical switches in the literature. As pioneering works, electro-optical deflectors comprising $LiNbO_3$ phase shifters were reported more than three decades ago [33, 34]. The first semiconductor-based integrated phased-array optical switch was then demonstrated with AlGaAs/GaAs guided-wave phase shifters and slab waveguides [35]. A design similar to an AWG was later proposed by using SiON-SiO_2 waveguides with thermo-optical phase shifters for up to 1×8 switching capability [36], which, however, had a slow reconfiguration speed limited by the response time of the thermo-optic effect. Another demonstration, which was not completely integrated, was a high-speed switching module combining an AlGaAs phase shifter array with free-space lenses [37]. Switches that utilize phased arrays with the imaging property of multimode interference waveguides were also developed [38].

Figure 2a shows the structure of the InP phased-array switch reviewed in this paper. Star couplers are employed for the $1 \times M/M \times N$ passive couplers due to their advantages such as simple design and high fabrication tolerance. The antisymmetric architecture is to maintain all the arrayed waveguides at equal length, which is necessary to achieve wavelength-independent switching. The basic operation of single-stage switching is possible by forming a linear distribution of optical phase (with modulo 2π) in the arrayed waveguides. The deflection angle at the output star coupler depends on the slope of this distribution, which makes electro-optical switching possible.

The switching properties can be analytically estimated as follows. Ignoring the propagation loss and excess losses at the phase shifters, the amplitude transmittance to the nth

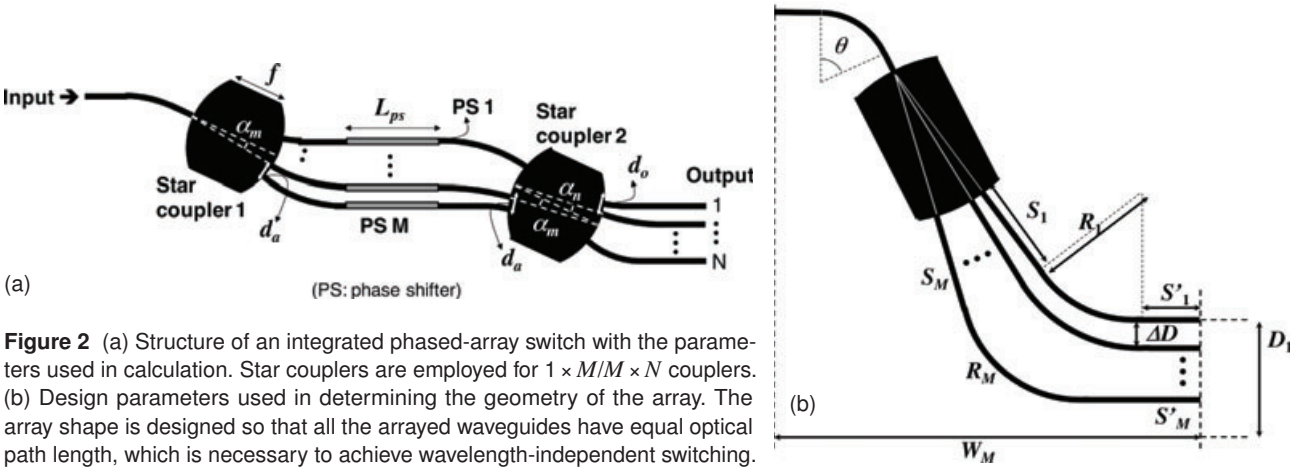

Figure 2 (a) Structure of an integrated phased-array switch with the parameters used in calculation. Star couplers are employed for $1 \times M/M \times N$ couplers. (b) Design parameters used in determining the geometry of the array. The array shape is designed so that all the arrayed waveguides have equal optical path length, which is necessary to achieve wavelength-independent switching.

output port is expressed as

$$T_n = \sum_{m=1}^{M} \eta(0, \alpha_m) \cdot \eta(\alpha_m, \alpha_n) \cdot \exp(j\varphi_m). \qquad (1)$$

As shown in Fig. 2a, α_m and α_n are the angular coordinates of the phased-array port and output port, respectively, and φ_m is the phase shift applied at the mth phase shifter. M is the total number of phase shifters. The function $\eta(\alpha_1, \alpha_2)$ denotes the transmittance of the star coupler from the input port angle α_1 to the output port angle α_2, and is expressed under the Fraunhofer approximation as

$$\eta(\alpha_1, \alpha_2) = \sqrt{\frac{k}{2\pi f}} \cdot \int u_1(x) \exp(jkx\alpha_2)\mathrm{d}x \cdot \int u_2(x) \exp(jkx\alpha_1)\mathrm{d}x \cdot \exp(-jkf\alpha_1\alpha_2), \qquad (2)$$

where k is the propagation constant at the star coupler, f is the star coupler length, and $u_1(x)$ and $u_2(x)$ are the mode-field profiles of the radiating and receiving waveguides, respectively [39].

A sufficient number of phase shifters are necessary in order to achieve high extinction ratio and low insertion loss. To examine the requirement of the number of phase shifters, M, (1) and (2) are solved for a typical InP waveguide structure [32]. We set $d_a = 2.50\,\mu\mathrm{m}$, $d_o = 2.35\,\mu\mathrm{m}$, and assume a 2-μm wide waveguide with the effective indices of 3.3 (core) and 3.2 (clad) in solving the mode fields $u_1(x)$ and $u_2(x)$. Figure 3 shows the required M as a function of the switch port count $N$to achieve an insertion loss below 5 dB and an extinction ratio above 30 dB at all output ports. Optimized values of f are also plotted for the respective cases. Here, the insertion loss is defined as the optical loss to a desired port under the ON state (when the switch is set to this particular port), while the extinction ratio is the ratio of the power under the ON state to that under the OFF state (when the switch is set to other ports). From Fig. 3, both the star coupler length and the number of phase shifters increase linearly with N. These results show that as long as

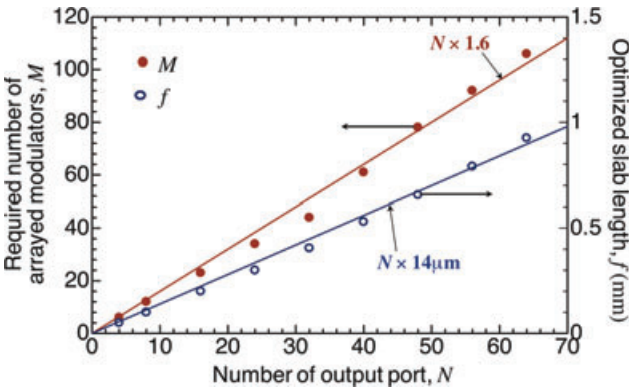

Figure 3 (online color at: www.lpr-journal.org) Number of arrayed waveguides (M) and the star coupler length (f) required to achieve an insertion loss below 5 dB and an extinction ratio above 30 dB.

a sufficient number of phase shifters are employed, the basic switching characteristics do not degrade even at a large number of output ports. The critical value of M required to achieve an extinction ratio over 30 dB is estimated to be approximately $1.6N$.

A geometrical optimization strategy was developed to achieve the wavelength insensitivity and the shortest optical path [32]. In order to achieve wavelength-independent operation, the path lengths through all arrayed waveguides must be designed to be equal. This condition is expressed as

$$\Delta L \equiv L_{m+1} - L_m = \text{const.}, \quad m = 1, \ldots, M-1), \qquad (3)$$

where L_m denotes the path length of the mth waveguide from the output of the first star coupler to the phase shifter input. This parameter is written as

$$L_m = S_m + R_m(\theta + \alpha_m) + S'_m, \qquad (4)$$

where S_m, R_m, θ, α_m are defined in Fig. 2b. Equations (3) and (4) should also be used to design the right side of the phase shifters with a rotation of 180°. Two additional condi-

tions are

$$W_m = (f + S_m)\cos(\theta + \alpha_m) + R_m \sin(\theta + \alpha_m) = \text{const.}, \quad (5)$$

$$\Delta D_m \equiv D_{m+1} - D_m = \text{const.}, \quad (6)$$

where

$$D_m = (f + S_m)\sin(\theta + \alpha_m) + R_m[1 - \cos(\theta + \alpha_m)]. \quad (7)$$

The physical size of the switch is defined by Eq. (5). Equal spacing between adjacent phase shifters is maintained by Eq. (6), where ΔD is determined by the required separation to achieve electrical isolation. While Eqs. (3), (5), and (6) provide $(3M - 3)$ conditions, there are $(3M + 2)$ of independent variables $\{R_m, S_m, S'_m (m = 1, \ldots, M), \theta, \Delta L\}$ to be solved. We therefore have five degrees of freedom in determining the array geometry, within which we find an optimal set of parameters that gives the minimum total path length.

3. Single-stage InP 1×16 switch and its applications

3.1. Design, fabrication and basic characterization of the device

To examine the feasibility of integrated large-scale switching using the phased-array technique, a single-stage 1×16 switch was designed and fabricated [25]. The device specifications were an extinction ratio over 30 dB, an insertion loss below 3 dB, and low wavelength sensitivity in the *C*-band (1530–1560 nm) of optical communications. In this particular device, an InP/InGaAsP p-i-n double heterojunction epitaxial structure with a bulk intrinsic layer as listed in Table 1 was employed in the entire chip. This structure maintains photon confinement in the InGaAsP core layer, where the phase shift is applied by carrier injection under a forward bias and/or electric field under a reverse bias. The bandgap wavelength of the intrinsic InGaAsP layer was selected as 1.3 μm to obtain sufficient phase-shifter efficiency, while avoiding high Urbach absorption [40, 41]. The core layer thickness was designed to 500 nm to support a single vertical mode with a high optical confinement ratio of 77%. A 1-μm thick InP upper cladding layer was inserted between the core and the contact layers to reduce the optical absorption loss. Highly p-doped InGaAs was employed as an upper contact layer to obtain an ohmic p-contact.

Table 1 Epitaxial profile of the 1×16 switch.

Material	Thickness (nm)	Doping (cm^{-3})
p-InGaAs	200	1×10^{19}
p-InP	750	5×10^{17}
u-InP	300	N/A
u-Q1.3 InGaAsP	500	N/A
u-InP	50	N/A
n-InP	250	5×10^{17}
n-InP	substrate	2×10^{18}

Next, the waveguide structure was designed. A ridge waveguide structure with a single-step shallow etching until the top 50 nm of the core layer was employed in the entire device. To maintain single-mode operation, the waveguide width was designed to be 2 μm at the bends and intersections with the star couplers. At the phase shifters, waveguides were widened to 4 μm to prevent critical damages in crystal quality, which may be caused during the reactive-ion etching process [42, 43]. The waveguides were linearly tapered to 5 μm at the input and outputs of the device to reduce the fiber coupling loss. The minimum radius of curvature in the bends was 500 μm. The length of the phase shifters (L_{ps}) was chosen to be 800 μm. The layout of the 1×16 switch was designed using the procedure formulated in Sect. 2. The final design parameters are listed in Table 2. In order to achieve the aforementioned extinction ratio and loss values, the number of phase shifters (M) was set to 24. The estimated values of the extinction ratio and the optical loss were 31 dB and less than 3.5 dB, respectively. Figure 4 shows the calculated transmittance to the 16 output ports as a function of the phase difference between adjacent phase shifters.

Due to the identical epitaxial design in the entire chip, the wafer was grown using a single-step metalorganic chemical vapor deposition (MOCVD). The waveguides were formed by methane (CH_4)-based reactive ion etching. A

Parameter	Value
M	24
f_1	240 μm
f_2	240 μm
d_a	2.5 μm
d_o	2.8 μm
On-chip loss	< 3 dB
Extinction ratio	> 31 dB

Table 2 Design parameters and calculated characteristics of the 1×16 switch.

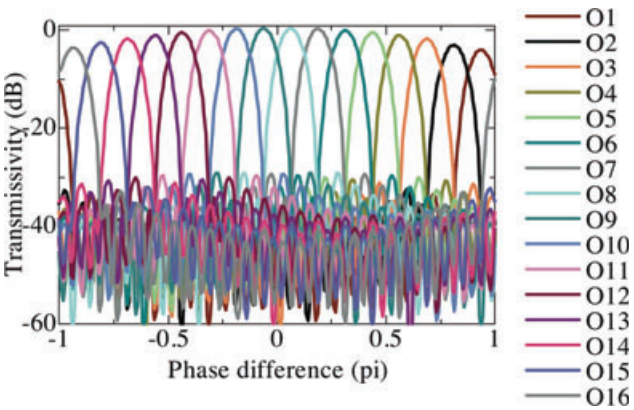

Figure 4 (online color at: www.lpr-journal.org) Calculated transmissivity to the 16 output ports (O1–O16) for different phase increment values between adjacent phase shifters.

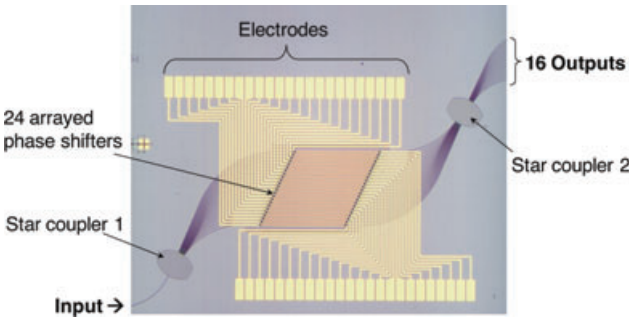

Figure 5 (online color at: www.lpr-journal.org) Micrograph of the fabricated 1×16 optical switch. The footprint is 4.1 mm×2.6 mm.

cyclical process consisting of multiple subsequent steps of CH_4/H_2 etching and oxygen cleaning was used in order to prevent the effects of polymer deposition during etching [44]. The InGaAs contact layer was removed in all regions except at the phase shifters. A 4-μm thick layer of polyimide was employed for both passivation and planarization. The n- and p-contacts were formed using electron-beam evaporated Pt/Ti/Au layers, which were later annealed to form ohmic contacts. The top view micrograph of the fabricated switch is shown in Fig. 5.

First, the static switching characteristics were examined with a TE-polarized input light at a wavelength of 1550 nm. The phase shift was obtained by using a combination of the electro-optic and carrier-induced phase-modulation mechanisms. The voltage applied to each phase shifter was between −10 to +1.5 V with the maximum injection current of 20 mA at +1.5 V. The operating conditions of the switch were found for 16 switching states, each forming a light path to one output port. In each state, the optimal voltages were found iteratively by the steepest descent method; the voltages applied to all the phase shifters were scanned one by one while measuring the power at the corresponding port. After the operating conditions were found, the insertion loss and the extinction ratio were measured in the wavelength range of 1530–1565 nm. Figure 6 presents the wavelength dependence of the fiber-to-fiber transmittance to respective output ports (O1–O16) measured in 16 different switching states (S1–S16). In all the states, the wavelength dependence of the transmitted power was below 0.8 dB in the wavelength range of 1530–1565 nm. At a wavelength of 1550 nm, the static extinction ratio had an average value of 18.6 dB and the minimum value of 11.3 dB (Output 9, S9/S8). The difference between the theoretical and experimental extinction ratios is attributed to aberrations in the waveguides and star couplers, possible excitation of higher-order modes in the wide waveguide sections, and electrical and thermal crosstalk between phase shifters. The fiber-to-fiber loss was between 15.1 dB (S11) and 17.0 dB (S1), out of which approximately 10 dB was estimated to be due to the fiber coupling according to our measurements on test waveguides. Under static operating conditions, the power penalty of the switch was measured with a 40-Gb/s nonreturn-to-

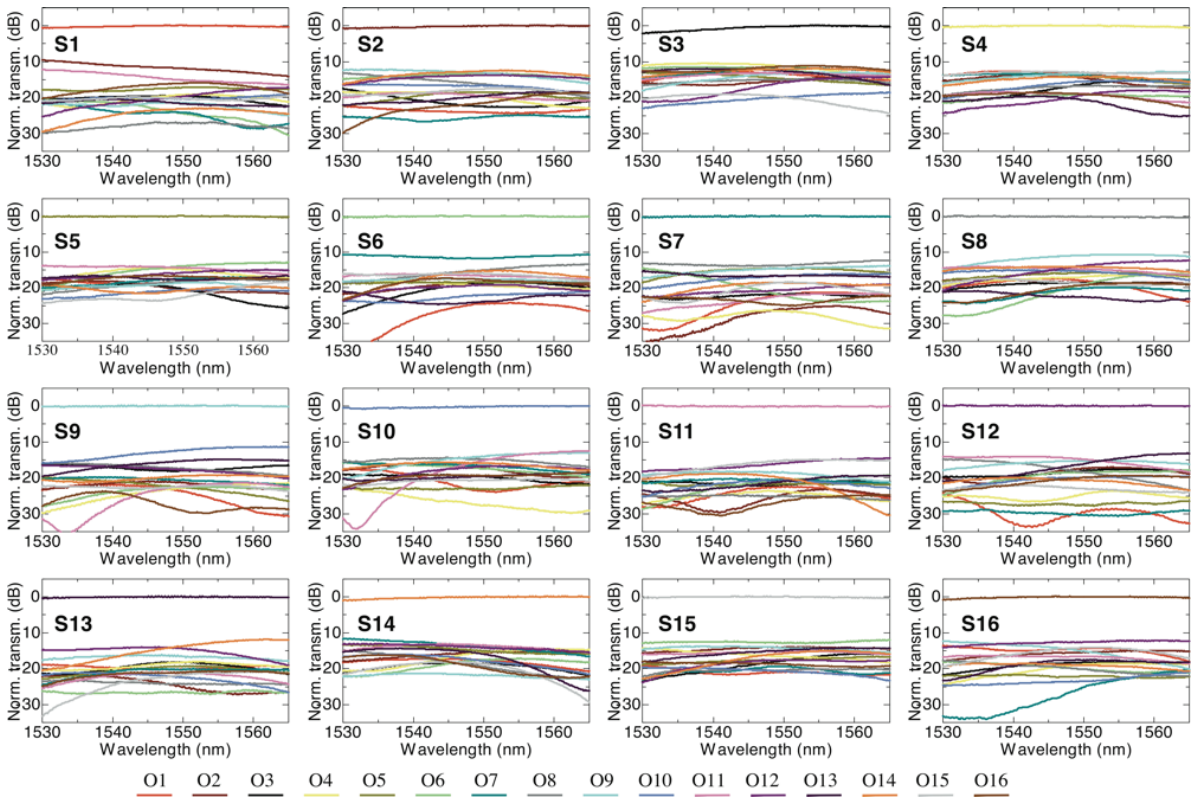

Figure 6 (online color at: www.lpr-journal.org) Fiber-to-fiber transmittance to the 16 output ports (O1–O16) as a function of wavelength in State 1 (S1) – State 16 (S16).

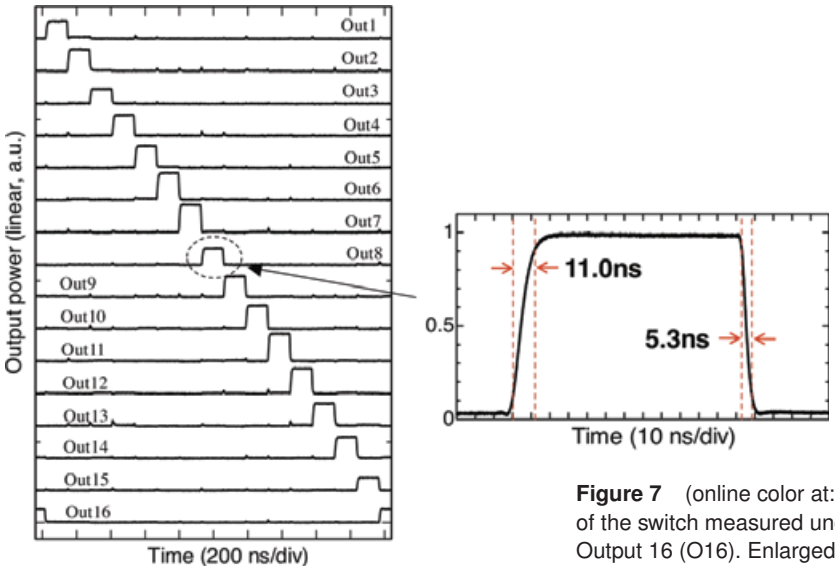

Figure 7 (online color at: www.lpr-journal.org) Waveforms at the outputs of the switch measured under dynamic switching from Output 1 (O1) until Output 16 (O16). Enlarged waveform at Output 8 is shown in the inset.

zero (NRZ) signal. The power penalty was less than 0.4 at a bit error rate (BER) of 10^{-9}.

The dynamic operation of the switch was also tested. An electric switch driver was built using a field-programmable gate array (FPGA) and digital-to-analog converters (DAC) to control individual phase shifters dynamically. The FPGA was programmed to reconfigure the voltage set to the predefined values according to a 4-bit control signal. Figure 7 displays the power measured at the outputs in the time domain, while the switching state changes from 1 to 16 sequentially with a clock period of 130 ns. The minimum dynamic extinction ratio of the switch was 10.9 dB. In the inset of Fig. 7, a zoomed image of the waveform at Output 8 is shown during the transition between States 7, 8, and 9. The reconfiguration time is less than 11 ns, which includes the effects of the dynamic response of the driver circuit and the electrical parasitics at the wire bonds.

3.2. Optical packet switching using an integrated phased-array switch

The wavelength insensitivity, transparency and nanosecond-scale reconfiguration time of phased-array switches, as demonstrated in the previous subsection, imply a potential of the phased-array switches for OPS applications, where the switching is performed transparently to the bit rate and modulation format. To investigate the feasibility of this application, an optical packet switch with a label processor was constructed using the 1×16 phased-array switch, an electric switch controller, and an all-optical label extractor [28, 29]. In order to verify the compatibility of this technology with different modulation formats, two types of packets carrying 160-Gb/s optical time-domain multiplexed (OTDM) on-off keying (OOK) and 120-Gb/s WDM differential phase-shift keying (DPSK) payloads were used.

In general, an optical packet consists of two sections, namely the payload and the label (header). Payload is the data carried by the packet, and the label consists of the necessary information to transport the data to the destination successfully. Since the label consists of a considerably smaller number of bits than the payload, it can be processed at a bit rate much lower than that of the payload. As a consequence, a scheme based on label processing in the electrical domain and transparent data switching in the optical domain has been recognized as a useful OPS architecture. In this way, the maturity of electronic signal processing and the data capacity of transparent optical switching are utilized simultaneously.

Labels can be classified into two types as serial and parallel labels, depending on the way they are attached to the payload. Serial labels are serial to the payload in the time domain. The extraction of this type of labels requires strict control of timing, which may become challenging, especially for asynchronous and variable-length packets. Relatively complicated envelope detection circuits are necessary to extract these labels. On the other hand, parallel labels share the same time interval with the payload. The label is located on a different wavelength, frequency, modulation format, or code from that of the payload so that they can be distinguished. Among them, wavelength-multiplexed labeling schemes are advantageous in the sense that the labels can be separated from the payload relatively easily with the use of passive optical filters [45]. In this experiment, optical in-band parallel labels were attached to the packets to encode the address information. These are parallel in-band labels, which have two differences from the conventional wavelength-multiplexed labels. In one packet duration, only one bit is represented in a wavelength channel and the labels are located inside the payload spectrum. The single-bit-per-channel approach has the advantage of removing serial-to-parallel conversion from the label extractor.

Figure 8 demonstrates the schematic diagram of the OPS node subsystem. It consists of three building blocks, namely the label extractor, optical switch and the switch controller. The label extractor separates the labels from the payload by wavelength filtering and sends them to the switch controller after optical-to-electrical (O/E) conversion. Ac-

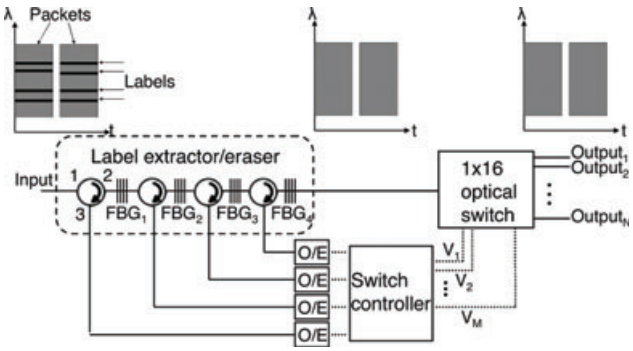

Figure 8 Schematic diagram of the optical packet switching node with a 1×16 optical phased-array switch.

cording to the address information encoded in the labels, the switch controller reconfigures the state of the optical switch. During label processing, the payload propagates in a fiber delay line to adjust the timing of switch reconfiguration and arrival of the payload at the input of the switch. The payload propagates through the switch without any processing and exits the output determined by the switch controller according to the label. In the experiments, label extraction/erasure was achieved using a cascade of fiber Bragg gratings (FBGs), whose reflection peaks matched the wavelengths of respective label bits. The integrated 1×16 phased-array switch was employed as the optical switch. The switch driver used in the dynamic switching experiments in Sect. 3.1 was reprogrammed as the electronic controller of the packet-switching node.

The 160-Gb/s OOK payload was obtained by time-multiplexing sixteen 10-Gb/s data streams, which were generated by modulating 10-GHz pulse trains from a mode-locked fiber laser (MLFL). The optical pulses had a full width at half-maximum (FWHM) of 1.5 ps and a 20-dB spectral width of 5 nm around the peak wavelength of 1546 nm. The second type of packet consisted of 12 DPSK-modulated 10-Gb/s nonreturn-to-zero (NRZ) channels with wavelengths between 1543.7 nm and 1548.5 nm (50 GHz spacing). These payloads were gated by using another $LiNbO_3$ Mach–Zehnder modulator to form packet trains with a packet length of 147.2 ns and a guard time of 32 ns. Four in-band parallel labels were located at wavelengths of 1543.9 nm, 1544.3 nm, 1547.7 nm, and 1548.2 nm and inserted inside the 20-dB bandwidth for the OOK payload and between the WDM channels for the DPSK payload, respectively. At the receiver, the payload was demultiplexed to the bit rate of 10 Gb/s for BER analysis. The OTDM payload was demultiplexed by using two cascaded electroabsorption modulators, whereas the WDM-DPSK payload was demultiplexed with a tunable optical bandpass filter. Demodulation of the DPSK signal was implemented by using a one-bit-delay Mach–Zehnder interferometer.

The optical power of each extracted label was approximately –20 dBm and the average power at the input of the switch was 7 dBm. The polarization state was maintained to be TE at the switch input. Figure 9a presents the time-domain waveforms and eye diagrams of dynamically switched 160-Gb/s OTDM-OOK packets at the outputs (O1–O16) of the 1×16 OPS node, observed in an example scenario. The input waveforms of labels (L_1–L_4) are also plotted in the same figure. These waveforms indicate that the packets were switched autonomously to the destination address represented by "$L_4L_3L_2L_1$." For example, the packet was sent to O1 if the label configuration was "0001". The minimum dynamic extinction ratio was between 11.0 dB and 13.3 dB among the 16 output ports. The results for 120-Gb/s WDM-DPSK packets are shown in Fig. 9b. Once again, each packet was routed according to the label information and clear eyes were observed after switching. Figure 10 shows the BER characteristics of the demultiplexed payloads, which were measured under a dynamic switching condition between two states. Error-free packet switching

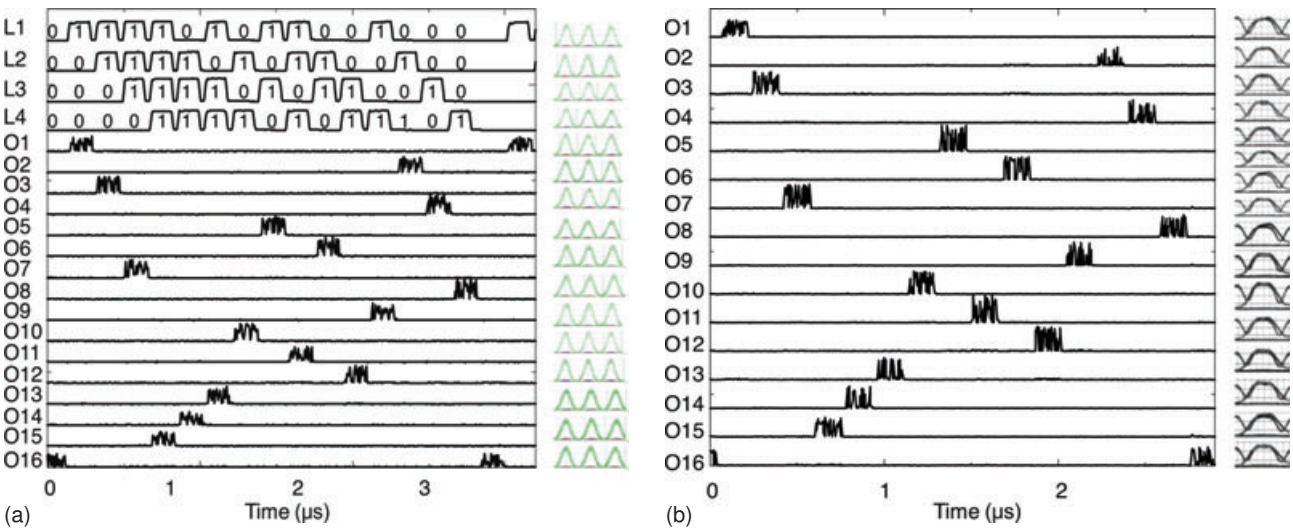

Figure 9 (online color at: www.lpr-journal.org) Waveforms and eye diagrams of (a) 160-Gb/s OTDM-OOK packets with labels, and (b) 120-Gb/s WDM-DPSK packets after switching.

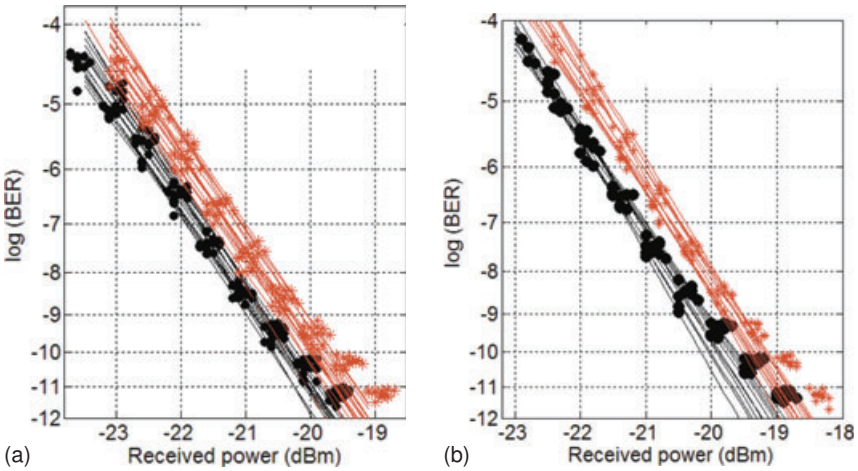

Figure 10 (online color at: www.lpr-journal.org) BER characteristics of the output packets for (a) OTDM-OOK and (b) WDM-DPSK packets.

was achieved with a power penalty of 0.7 dB for the OTDM-OOK packets and 0.6 dB for the WDM-DPSK packets at the BER of 10^{-11}.

3.3. Large-capacity tunable optical buffering using an integrated phased-array switch

Tunable optical buffering, which is required for temporal contention resolution of colliding packets, is another major technical challenge in implementing OPS. Using the transparency and port-count scalability of the phased-array switches, we can construct large-capacity broadband optical buffers in relatively compact dimensions [31]. The schematic of the tunable buffer is shown in Fig. 11. The $1 \times N$ switch routes the signal to the desired fiber delay line (FDL) according to the required buffering length. At the output, the passive coupler combines all the FDLs to a single output fiber. In principle, the passive coupler can be replaced

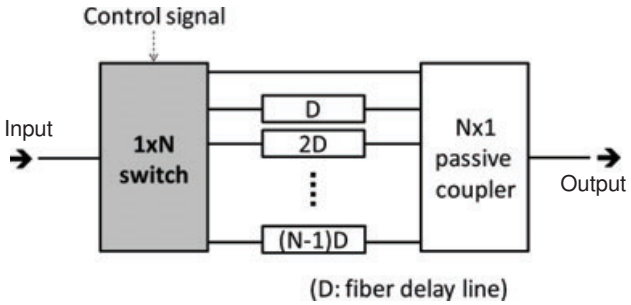

Figure 11 Schematic of a tunable optical buffer that consists of a $1 \times N$ switch, FDLs and an $N \times 1$ passive coupler.

by another $N \times 1$ switch, which can not only reduce the optical insertion loss, but also suppress the crosstalk. By using high-index-contrast thin-cladding fibers, FDLs can be packaged into a compact bobbin with a coin-sized footprint [46].

Figure 12 shows the experimental setup of tunable buffering as well as the schematic and photograph of the

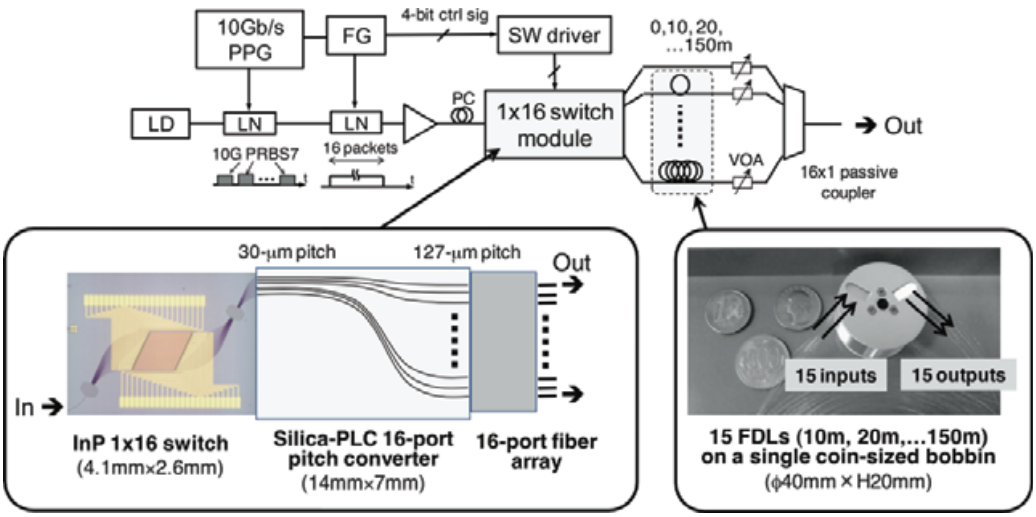

Figure 12 (online color at: www.lpr-journal.org) Setup of the tunable optical buffering experiment. Schematic structure of the 1×16 switch module and the photograph of the compact FDL module are shown in the insets. LD: laser diode, PPG: pulse-pattern generator, FG: function generator, PC: polarization controller.

developed buffer module. It has been theoretically proposed that under certain conditions, a buffer capacity of 10–20 packets is sufficient to reach a throughput of 0.8 [47, 48]. In order to investigate the feasibility of tunable optical buffering at this scale, a 1×16 integrated phased-array switch was used together with 15 high-index-contrast FDLs. The multiport coupling between the phased-array switch and the FDLs was achieved using a 16-port silica planar lightwave circuit (PLC) chip.

Ultrathin-cladding highly nonlinear fibers (HNLF) were employed to build compact FDLs. The tight optical confinement in the HNLF made it possible to reach a bending radius as small as 7.5 mm without inducing high optical loss and mechanical damage [46]. Fifteen fibers with lengths of 10, 20, 30, ..., 150 m (total length of 1.2 km) were coiled onto a single bobbin to achieve the temporal resolution of 50 ns and buffering capacity of 16 packets. The dimensions of the entire FDL module were 40 mm in diameter and 20 mm in height. The fiber-to-fiber loss of the 15 FDLs ranged from 0.4 to 0.9 dB, which included splicing losses from both ends. Although the nonlinear coefficient of HNLF is higher ($13\ W^{-1}\ km^{-1}$) than a standard single-mode fiber, its effects should be negligible for these FDL lengths as long as the optical peak power is lower than 1 W, which is the case for practical implementations.

As a demonstration of tunable buffering, a periodic series of sixteen optical packets with 10-Gbps payload, 30-ns duration, and 20-ns guard time was transmitted through the subsystem, as shown in Fig. 12. Figure 13 shows the waveforms at the input of the switch, outputs of the switch and the output of the 16×1 coupler. In this demonstration, 16 packets were forwarded sequentially to respective output ports to experience different delays. As a result, the packet intervals of 20 ns at the input were expanded successfully to 70 ns after the buffer, and the maximum delay of 750 ns was achieved with the 150-m FDL. A bursty packet traffic at the input was thus shaped into a more uniform traffic pattern at the output.

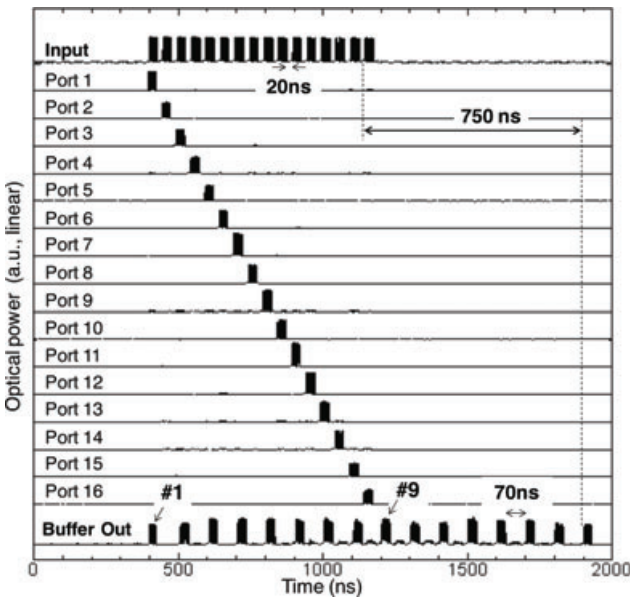

Figure 13 Packet waveforms at the input of the 1×16 phased-array switch, outputs of the switch and the output of the 16×1 coupler.

4. Two-stage 1×100 monolithic InP switch

In the previous section, we have presented a single-stage 1×16 switch and its applicability to OPS subsystems. In order to increase the port count further, while keeping the power consumption low, it is beneficial to employ the multi-stage configuration. In addition, the suppression of crosstalk becomes more and more important as the port count increases. The crosstalk suppression ratio can be improved with the help of active components such as SOAs. Recently, we have demonstrated that by employing two-stage phased-array switches and an SOA gate array, a large-scale photonic integrated switch with an output port count as large as 100 can be fabricated monolithically on a single InP chip [26]. In this section, we summarize the design, fabrication and characterization of this 1×100 switching PIC.

4.1. Design of the two-stage 1×100 switching PIC

The schematic diagram of the 1×100 switching PIC is shown in Fig. 14. Although phased-array switches can in principle switch to 100 outputs in a single stage, two cascaded stages of 1×10 switches were employed to reduce the number of phase shifters operated simultaneously. As a result, the total power consumption of phase shifters was reduced to one fifth of the single-stage configuration. In addition, an SOA was attached at each output port, as shown in Fig. 14. Note that unlike the SOAs in BS switches, the SOAs in Fig. 14 were not necessary for switching, but these multifunctional components were employed to improve the on/off extinction ratio by operating as gates, to compensate for the insertion loss partially, to regulate the power distribution among ports, and to serve as power monitors under reverse bias. During regular single-port operation of the switch, only one of the SOAs had to be biased electrically.

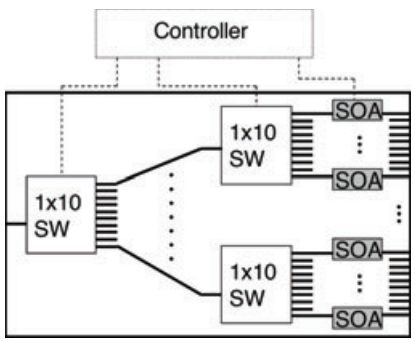

Figure 14 Schematic diagram of the InP 1×100 switching PIC.

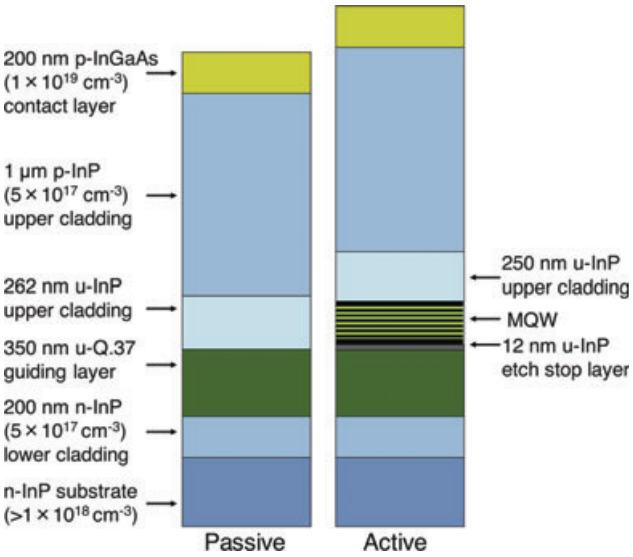

Figure 15 (online color at: www.lpr-journal.org) Epitaxial structure in the passive and active regions of the PIC

Due to the presence of SOAs, an active/passive integration method had to be employed. Among several techniques, such as the selective-area growth [49], butt-joint regrowth [50], offset quantum well (QW) [51], dual QW [52], and QW intermixing [53] methods, the offset QW technique was selected in this work. In the offset QW technique, both the active and passive waveguides share the same bulk guiding layer, whereas a lower-bandgap multiple quantum well (MQW) layer lies above the guiding layer in the active components. This method was preferred for this particular PIC for multiple reasons. First, it presents a relatively low active/passive coupling loss since the guiding layer is continuous in the entire chip. This method is relatively easy to implement because it includes only one additional step of etching and growth. The propagation loss in the passive waveguides is as low as in all-passive devices due to the bulk guiding layer in the passive regions. Low overlap of the waveguide mode with the offset MQW, which is usually undesired for active devices, is an advantage in this PIC because lower modal overlap leads to higher output saturation power of SOAs [54].

Figure 15 depicts the epitaxial design in the passive and active regions of the PIC. The thicknesses and bandgaps of each epitaxial layer were designed carefully considering the propagation loss, efficiency of the phase shifters and the SOA gain. To achieve high efficiency of carrier-induced phase shift, the emission edge of the InGaAsP core layer was set to 1.37 µm. According to the exponentially decaying absorption model [55], the absorption by InGaAsP at this wavelength is estimated to be approximately 0.53 dB/cm. The phase-shifter efficiency is proportional to the confinement factor, which increases with the thickness of the core layer. However, the free-carrier concentration for a fixed amount of current reduces as the volume increases. From the calculation based on the confinement factor and the carrier concentration, phase-shifter efficiency was estimated to be within 95–100% of the maximum value as long as the thickness of InGaAsP core layer lies in the range of 350–550 nm. Considering that a thinner guiding layer leads to larger overlap with the MQW layer at the SOA sections, 350 nm was selected as the thickness of the InGaAsP core layer. The MQW layer was designed to obtain an emission peak at a wavelength of 1.55 µm. The thickness of both InGaAs wells and InGaAsP (Q1.25) barriers was set as 8 nm. The wells were designed to have a compressive strain of 0.4% in order to maximize the gain in the TE polarization. Seven quantum wells were employed in the MQW. A 1.25-µm thick InP cladding layer was located above the guiding layer (and MQW in active regions) to minimize the optical mode overlap with the lossy contact regions. The lowest 250 nm of the cladding layer was designed to be undoped to reduce the absorption in the p-InP cladding layer. Finally, a 200-nm thick InGaAs contact layer was located at the top of the stack.

The important design parameters and estimated switching properties of the phased-array switches in the PIC are listed in Table 3. The two-stage 1 × 100 phased-array switches in this PIC had a different design strategy compared to that of the single-stage 1 × 16 switch presented in Sect. 3. Owing to the presence of the SOAs, the extinction ratio of these switches did not have to be as high as that of the 1 × 16 switch. In the second stage, the number of phase shifters (M) was reduced to 12 in order to reduce the footprint, power consumption and the complexity of operation. The major mechanism that increases the loss in switches with low array-to-output ratios is the truncation of the diffracted light at the input of the arrayed waveguides. Because of the small number of arrayed waveguides, a significant portion of the diffracted light does not couple to the waveguide modes. This phenomenon also increases the effects of mode distortion at the output plane. The solution of this problem is shortening the star couplers. However, the second star coupler cannot be shortened freely, because all the output ports must be placed inside a free spectral range (FSR). Therefore, the first star coupler of the second-stage switches was shortened to 100 µm without modifying the length of the second one (135 µm). Similar to the 1 × 16 switch, the layout of each switching stage was optimized using the design procedure described in Sect. 2, so that the optical path lengths through all arrayed waveguides were equal.

Table 3 Design parameters and calculated characteristics of each phased-array switching stage in the PIC.

Parameter	1st stage	2nd stage
N	10	10
M	15	12
f_1	110 µm	100 µm
f_2	135 µm	135µm
d_a	2.5 µm	2.5 µm
d_o	2.55 µm	2.55 µm
Loss	< 3.7 dB	< 4.3 dB
Extinction ratio	> 31.2 dB	> 22.0 dB

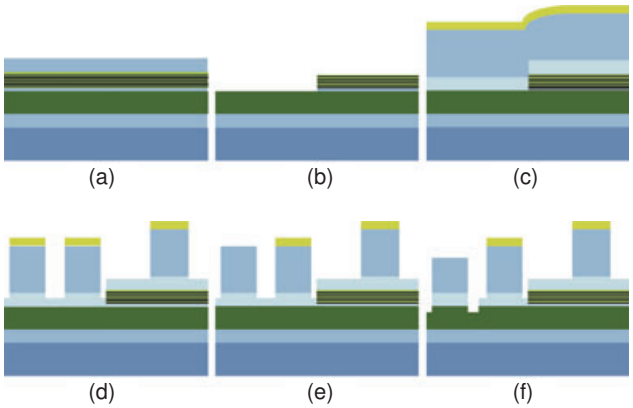

Figure 16 (online color at: www.lpr-journal.org) Fabrication process of the PIC until the end of waveguide etching: (a) unprocessed wafer, (b) after cladding layer and MQW are etched in the passive regions, (c) after regrowth, (d) after the first-step waveguide etching, (e) after removing InGaAs contact layer in passive waveguides, (f) after the second-step waveguide etching. Waveguides in (d–f) represent a relatively deeply etched passive waveguide, phase shifter and an SOA from left to right. Figures are not to scale. The colors correspond to those in Fig. 15. Photoresists and SiO_2 hard masks are not shown for clarity.

In order to minimize the propagation loss and the footprint simultaneously, the waveguides in the PIC were designed to have two different levels of optical confinement. The waveguide geometries are shown in Fig. 16f. The phase shifters and SOAs were designed as shallow-etched waveguides, where the etching was stopped at approximately 150 nm above the core layer in order to mitigate the damage of active layers caused by the dry etching process [41, 42]. On the other hand, comparatively deeply etched waveguides were employed at the bends to reduce the radius of curvature. In these sections, the entire top InP cladding layer and the top 100 nm of the core layer were etched. The reason for stopping the etching at the top of the core layer was to prevent the higher-order modes in the 2-μm wide waveguides and suppress the propagation loss caused by the sidewall roughness. The coupling loss between the shallow and deeply etched waveguides was reduced by tapering the deeply etched waveguides laterally to 5 μm at the intersections.

All SOAs were 5 μm wide and 500 μm long. The phase shifters were 4 μm wide and 800 μm long in the first stage and 600 μm long in the second stage. The minimum radius of curvature of the bends was set to 200 μm. At the intersections, straight waveguides and bends were offset from each other in the transverse direction in order to maximize coupling to the fundamental mode [56]. An optimal value of offset was used for each individual bend in the PIC depending on its radius of curvature. The waveguides at the input and output facets were tilted by 7° to prevent the reflected light from coupling back to the waveguide modes. The interface between active and passive regions was also tilted laterally by 7° to prevent internal reflections.

The switches were located on the chip in a configuration to minimize the footprint and average optical path length. Although very large electrodes are usually not preferred because of their large capacitance, the electrode pads were designed as large as possible in this PIC in order to increase the yield of wire bonding. The final dimensions of the PIC were 6.0 mm × 6.5 mm, a significant portion of which was occupied by the electrodes.

4.2. Fabrication of the 1×100 switching PIC

Figure 16 describes the fabrication steps until the end of the waveguides etching process. After the first MOCVD growth, (Fig. 16a), the active/passive regions were defined by using wet chemical etching techniques (Fig. 16b). First, the InP cladding and MQW layers were selectively etched. Next, InP and InGaAs layers were regrown on the entire sample by using MOCVD (Fig. 16c). Following the regrowth, the first-step methane-based reactive ion etching (RIE) was carried out using a sputtered SiO_2 hard mask until reaching the etching depth of the shallow waveguides (Fig. 16d). The contact opening regions were then defined by lithography, after which the InGaAs contact layer was removed from the passive waveguides by wet chemical etching (Fig. 16e). Finally, the deep and shallow regions were defined and the second-step RIE was performed to form the deeply etched waveguide regions (Fig. 16f). The rest of the process was identical to that described in Sect. 3.1. The cross-sectional scanning electron microscope (SEM) image of the active-passive interface is shown in Fig. 17. The micrograph of the PIC at the end of the fabrication is shown in Fig. 18.

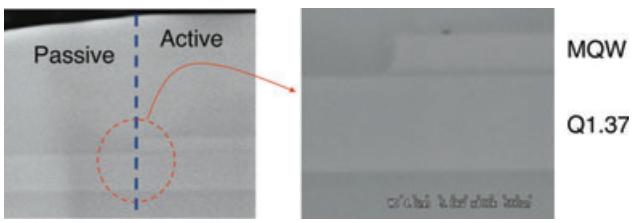

Figure 17 (online color at: www.lpr-journal.org) SEM image of the active/passive interface in the fabricated PIC.

4.3. Characterization of the 1×100 switching PIC

Before testing the operation of the entire PIC, the properties of phase shifters and SOAs were characterized separately. Figure 19a shows the power measured at one of the output ports of the PIC as a function of the current injected to one of the phase shifters. A 2π-current of less than 1.5 mA (0.9 V) was obtained owing to the optimized design of the phase shifters. Next, the transmittance curve of a typical SOA was measured as plotted in Fig. 19b. The SOA gain was calculated by subtracting the loss of two-stage phased array switches, which was estimated by comparing the ASE power from both the input and output ends of PIC [26]. With a current of 100 mA (2.2 V), the SOA gain was approximately 6 dB including the active-passive coupling loss.

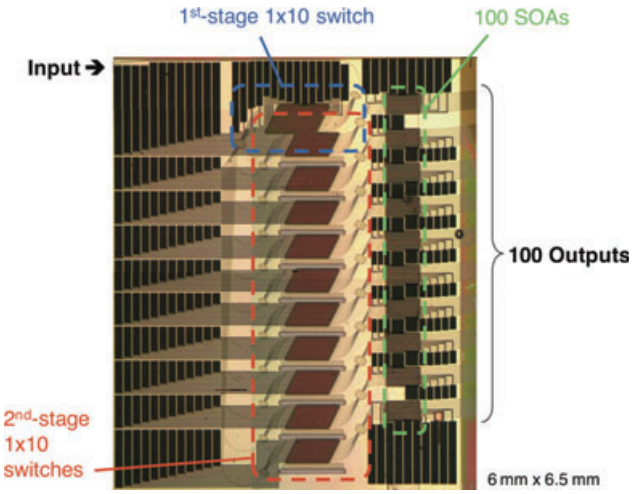

Figure 18 (online color at: www.lpr-journal.org) Top micrograph of the fabricated InP 1×100 switching PIC. The dimension is 6.0 mm×6.5 mm.

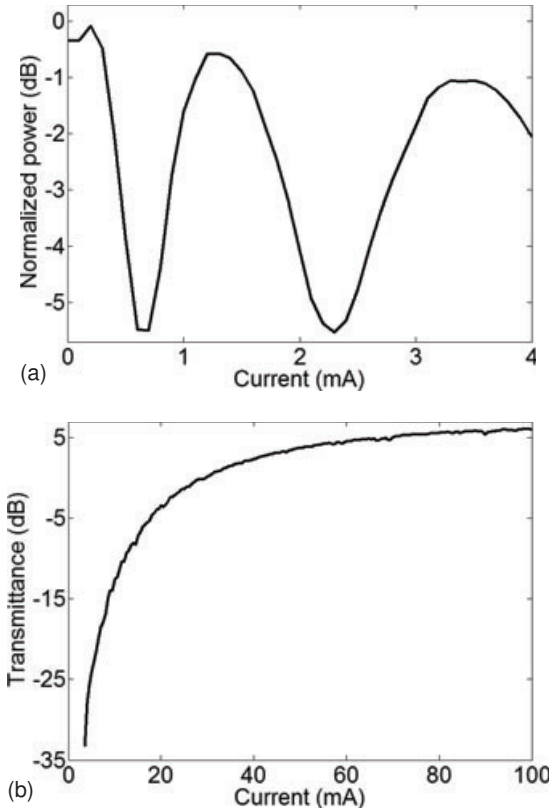

Figure 19 (a) Normalized optical power at an output as a function of the current injected to one of the phase shifters. (b) Transmittance of an SOA versus the current.

The operating conditions of the switch were then derived for respective switching states. In each state, 27 phase shifters (15+12) had to be controlled simultaneously. Figure 20 shows the on-chip loss of States 1–10 and States 70–90. The injection current to the SOA was set to 100 mA (2.2 V), while the injection current to each phase shifter was optimized in the range from 0 to 1.5 mA (0–0.9 V). The total static power consumption to drive all 27 phase shifters was less than 25 mW in all states. Only these 31 switching states were selected for testing due to the physical limitations of wire bonding. These states, however, theoretically have the higher losses as the signal is routed to the outermost ports. The on-chip loss was measured to be less than 15.2 dB for all the 31 states. We should note that out of 51 phase shifters in the first and second stages, which we have tested, 9 of them could not be controlled because of problems associated with wire bonding. This should be one of the reasons for the increased loss and interchannel nonuniformity compared with those estimated in design. Owing to the SOAs, the total extinction ratio of the switch was over 50 dB for all states, which was beyond the dynamic range of the measurement. By measuring the spectral response, the 3-dB optical bandwidth of the entire 1 × 100 switch was found to be from 1533 nm to beyond 1570 nm. Finally, the performance of the switch was tested with a 2^{31}-1-bit long pseudorandom binary sequence at a bit rate of 10 Gb/s using a preamplified receiver. As shown in Fig. 21, the power penalty was below 1 dB at a BER of 10^{-9} in all the states measured (States 81–90). The fluctuations of BER data points and the negative power penalty at some channels were attributed to the fluctuation in the fiber-waveguide coupling.

5. Conclusions

Integrated phased-array switches have been demonstrated and their potential applications have been investigated both experimentally and theoretically. Experimental works on the device level have led to some of the largest-scale integrated

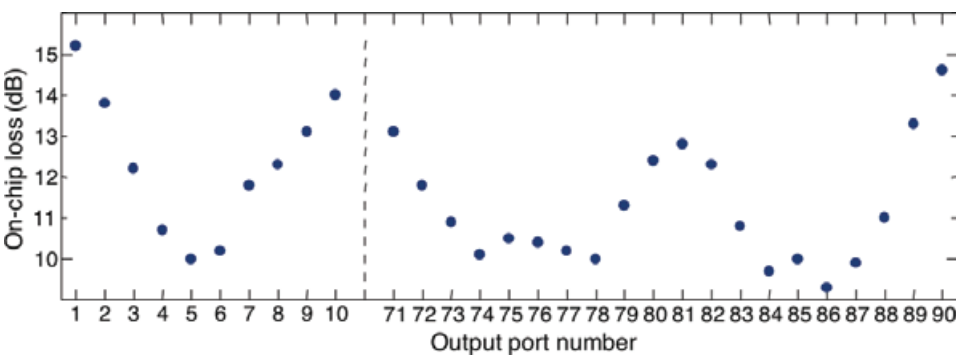

Figure 20 (online color at: www.lpr-journal.org) On-chip optical loss measured in 31 switching states.

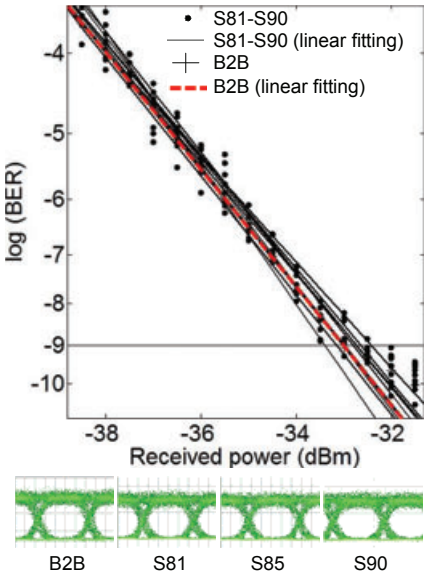

Figure 21 (online color at: www.lpr-journal.org) BER characteristics and eye diagrams of 10 Gb/s NRZ signal before (B2B: back-to-back) and after switching.

semiconductor photonic switches in the literature. These devices also demonstrated compatibility with large-scale photonic integration. As a potential application, optical packet routing was demonstrated with different bit rates and modulation formats. The switching performance was independent of the bit rate and the modulation format owing to the transparency and ultrabroad bandwidth of phased-array switches. These devices were also used to demonstrate tunable optical buffering, where optical packets were synchronized in the time domain.

This field has potential for further development due to the limited number of research efforts up to date. Improvements of the device design and fabrication methods will lead to lower loss, higher extinction ratio, lower power dissipation and smaller footprint. Since routers with large bit rate capacities will necessitate a large number of devices of this type, large-scale photonic integration is required. In addition to the amplitude-controlling devices introduced in this article, other photonic devices have to be integrated with phased-array switches. For example, integrated power monitors are useful for calibration of large-scale phased-array switches. The integration of a 1×8 InP phased-array switch with inline power monitors has been reported recently [27]. Phased-array switching is expected to increase its feasibility and impact further in parallel with the improvements of semiconductor photonic integration technology.

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