Simulations of Buffer Layers in a-Si:H Thin Film Solar Cells Deposited with an Expanding Thermal Plasma

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ABSTRACT

With an Expanding Thermal Plasma Chemical Vapor Deposition system (ETP-CVD), solar grade amorphous silicon (a-Si:H) can be deposited at high deposition rate (> 2 nm/s). We think that during the first stage of deposition, a material is grown with a higher defect density than the rest of the bulk creating a defect-rich layer (DRL). Therefore we analyzed, by the means of simulations, the influence of the position of the DRL on the performance of a p-i-n a-Si:H solar cell when moved from the p-i towards the i-n interface and as a function of its thickness. We investigate the effect of a buffer layer in between the p- and the i-layer on the external parameters of the solar cell. The presence of a buffer layer increases the electric field near the p-i interface, which leads to a higher collection of free charge carriers at the interface, although the electric field is then diminished deeper in the bulk. It appears that 10 nm thick buffer layer is sufficient to improve the performance. In case no buffer layer is applied, recombination losses at the p-i interface diminish the performance of the solar cell. We also observe that an increase of the DRL thickness results in a reduction of the solar-cell performance, which is more pronounced when the DRL is located in the region close to the p-i interface rather than close to the i-n interface.

INTRODUCTION

In order to reduce the production cost of thin-film amorphous silicon solar cells, high growth rates for the deposition of the intrinsic layer are required. With expanding thermal plasma chemical vapour deposition (ETP CVD), deposition rates of up to 10 nm/s for solar grade a-Si:H have been achieved [1]. At high growth rates, however, higher deposition temperatures are required to obtain high-quality amorphous silicon. In turn, these high deposition temperatures lead to deterioration of the p-layer when these intrinsic layers are implemented in p-i-n solar cells [2]. It has been demonstrated experimentally [3] that implementation of a high-quality intrinsic layer (which we will refer to as the 'buffer' layer) in between the p- and high-rate ETP i-layer improves the performance of the solar cells, in particular due to an enhancement of the open-circuit voltage, V_{oc}, and the fill factor, FF. We think that this buffer layer protects the p-layer from thermal damage by reducing the diffusion of hydrogen out of the p-layer. However, a performance improvement was observed also for solar cells with a low temperature (250°C), high-rate (0.9 nm/s) intrinsic layer in which a buffer layer was implemented [3]. We think that with ETP CVD a thin defect-rich layer (DRL) is formed during the first stages of deposition, whereas the quality of the remainder of the intrinsic layer is good. Implementing the buffer layer

in the cell moves the DRL away from the critical p-i interface, reducing the recombination and improving the *FF*.

In this article we present simulations, carried out with the Advanced Semiconductor Analysis (ASA) program [4], that aim to investigate the position dependence of the DRL on the solar-cell performance. By increasing the thickness of the buffer layer, the DRL is shifted through the intrinsic layer. We also investigate the influence of the DRL thickness on the cell performance. These simulations may shed light on the properties of the material deposited during the initial stages of the growth with ETP CVD. Other workers (e.g., see [5]) have simulated the effect of a buffer layer in the p-i region, with for example different band gap profiles, but in contrast to the work presented in this article, the aim was to optimize the cell performance.

The ASA program is an one dimensional (1-D) simulation program that calculates the internal electrical properties and external characteristics of multi-layer, heterojunctions a-Si:H solar cells by solving the system of semiconductor equations (Poisson's, continuity and transport equations) for the steady state. The main features of the ASA program include calculation of light generation profile, models describing a complete density of states distribution as function of energy, and calculation of the defect-state distribution in a layer according to the defect-pool model (DPM) [6]. The continuous change of all input parameters as a function of position in the device can be defined.

SIMULATIONS AND RESULTS

Solar cell structure

The structure of the cells simulated with the ASA program is presented in figure 1: a glass substrate covered with a transparent conductive oxide, an a-Si based p-, i- and n-layer and finally the aluminum back contact. The intrinsic layer is divided in three parts: the buffer layer with thickness varying between 0 and 390 nm, the initial grown DRL, which has a thickness of 30 nm, and finally the bulk of the ETP i-layer with a thickness varying between 410 and 20 nm. The total thickness of the intrinsic layer is kept constant at 440 nm.

Input parameters

In table I, the input parameters for the ASA program are listed. Table I includes the band gap, E_g, the electrons and holes extended-state mobility, μ_e and μ_h, the density of states at the mobility conduction band edge, N_C^{mob} and at the mobility valence band edge, N_V^{mob}, and the characteristic energy E_{C0} and E_{V0} of the conduction and valence band tail, respectively. The effective densities of extended states for the conduction band, N_C and for the valence band, N_V, were kept constant at 4×10^{26} m^{-3} and the electron affinity, χ_e, was taken to be 4 eV. We assume that the Urbach energy of the DRL is higher than in the bulk of the intrinsic layer in order to account for the higher defect density.

The density-of-states distribution is calculated using the defect-pool model (DPM) from Powell and Deane [6]. The following DPM parameters have been used: the position of the peak of the defect pool, E_P, is taken at 1.25 eV, except for the p-layer in which case it is at 1.27 eV, the width of the defect pool, σ, can be found in table I. The correlation energy between the transition energy levels representing the dangling bonds is E_{corr} = 0.2 eV.

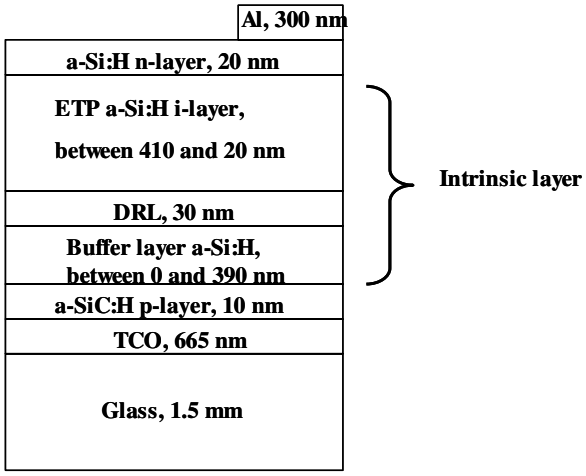

Figure 1. Schematic diagram of an a-Si:H solar cell as depicted in the ASA modeling.

Effect of buffer layer

Two kinds of simulations were carried out. In the first series, the buffer-layer thickness was increased, moving the DRL away from the p-i interface. The DRL thickness was fixed at 30 nm.

The external parameters of the simulated solar cells can be found in table II. When a buffer layer is incorporated in the cell, the V_{OC} first increases slightly, but then stays constant for a buffer-layer thickness in excess of 10 nm. The short-circuit current density, J_{SC}, decreases somewhat, though the *FF* increases significantly. The efficiency, η, also increases. The same trends have been observed experimentally on ETP solar cells [3].

The band diagram of the two simulated cells, one with and one without buffer layer, is shown in figure 2. We can see that near the p-i interface, in the region denoted as A, the bending of the conduction and valence bands is less strong for the cell without buffer layer compared to the one with a 50 nm thick buffer layer. This strong bending implies that the internal electric field is stronger in that region when a buffer layer is applied (see figure 3) and therefore the charge carriers are swept out of this region faster than when there is no buffer layer. The chance of recombination is then less and the *FF* increases. Moreover, when no buffer layer is incorporated in the cell, the defect density drastically increases at the p-i interface because of the DRL, creating a barrier for the holes to reach the p-layer for collection. The buffer layer permits to move the DRL away from the sensitive p-i area, thereby diminishing the recombination at the interface and improving the *FF*.

Table I. Parameters used in the ASA modeling.

Layers	E_g (eV)	μ_e / μ_h ($m^2V^{-1}s^{-1}$)	N_V^{mob} ($m^{-3}.eV^{-1}$)	N_C^{mob} ($m^{-3}.eV^{-1}$)	E_{V0} (meV)	E_{C0} (meV)	σ (eV)
p-type	1.97	1×10^{-3} / 1×10^{-4}	1×10^{28}	1×10^{28}	80	70	0.179
buffer	1.75	2×10^{-3} / 5×10^{-4}	5×10^{27}	7×10^{27}	50	32	0.160
DRL	1.75	1×10^{-3} / 1×10^{-4}	5×10^{27}	7×10^{27}	80	53	0.165
bulk ETP	1.75	2×10^{-3} / 5×10^{-4}	5×10^{27}	7×10^{27}	45	30	0.160
n-type	1.75	1×10^{-3} / 1×10^{-4}	7×10^{27}	7×10^{27}	90	80	0.175

Table II. External parameters of the simulated solar cells with varying buffer layer thickness.

Buffer layer (nm)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (-)	η (%)
0	0.795	11.9	0.627	5.94
10	0.801	11.7	0.658	6.18
50	0.801	11.4	0.688	6.27
75	0.802	11.4	0.693	6.32

Further in the cell, in the region denoted as B, we can see that the band bending is stronger for the cell without a buffer layer, resulting in a stronger electric field deeper in the cell. This means that, for the cell without buffer layer, more charge carriers are collected from deeper in the cell than for a cell with buffer layer at the expense of charge-carrier collection near the p-i interface. However, deeper in the cell fewer carriers are generated, but as these carriers experience a higher electric field, it is more likely that these carriers are collected, which implies that J_{SC} is higher for the cell without buffer layer.

There are several competing effects that determine the performance of a cell: the strength of the electric field and the defect density, the generation and recombination profiles. When the electric field is high, the carriers have more chance to be separated and collected, but if the defect density is also high, the carriers have more chance to recombine. The collection probability depends on where the DRL is situated and how thick it is. In our case, it seems that a buffer layer of 75 nm thick permits to increase the FF, but the J_{SC} is already slightly decreasing, so a thicker buffer layer would not increase the performances anymore.

Effect of the defect-rich layer

In the second series of simulations, we studied the effect of the variation of the thickness of the DRL, grown during the initial stages of the deposition with ETP. It appears that the thicker this defective layer, the lower the solar cell performance in terms of V_{OC}, FF and J_{SC} (see figure 4). A 10 nm thick buffer layer is sufficient to improve the V_{OC}. For thicker buffer layers, the V_{OC}

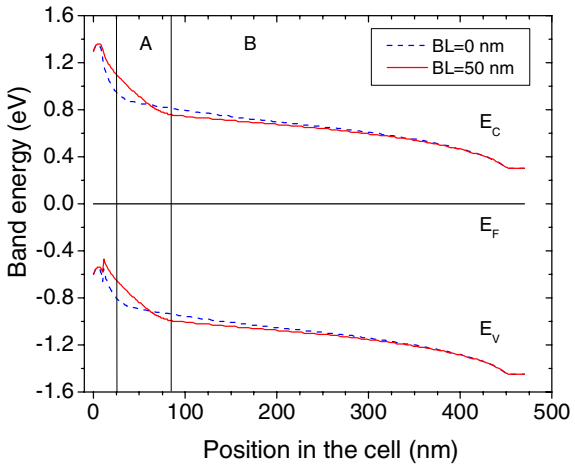

Figure 2. Band diagram of the simulated cells at thermal equilibrium with and without buffer layer. The DRL is 30 nm thick.

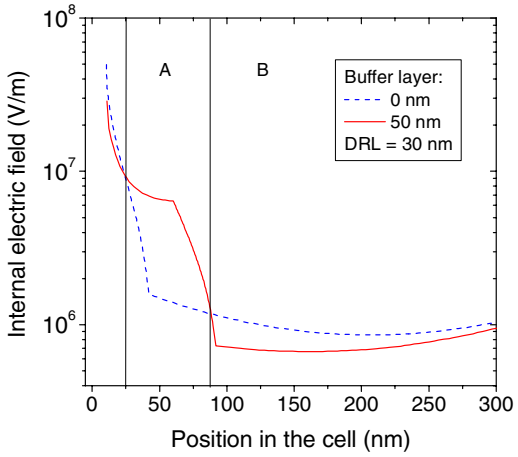

Figure 3. Internal electric field distribution for cells with and without buffer layer. The DRL is 30 nm thick.

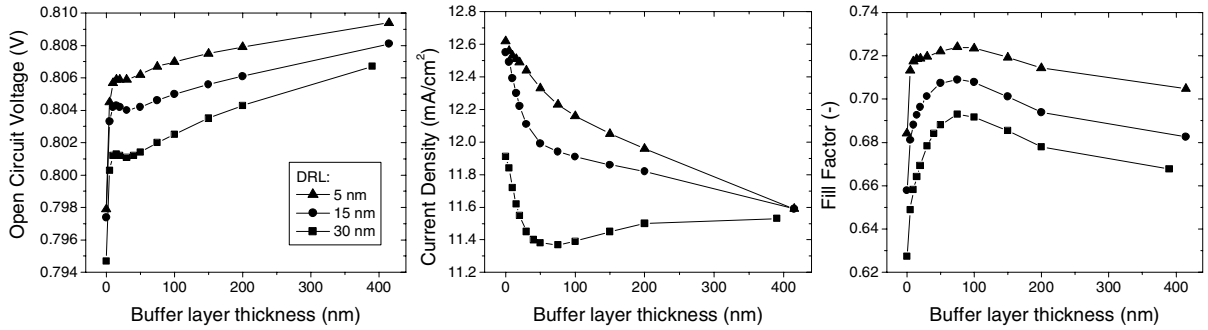

Figure 4. Simulations of the external parameters of a p-i-n cell as a function of the buffer layer thickness, this for three different thicknesses of DRL. The total thickness of the intrinsic layer is 440 nm.

increases only slightly. The J_{SC} decreases to reach a minimum value, which does not depend on the DRL thickness. The *FF* is largely affected by the DRL thickness and the same trend is observed for the three thicknesses. The *FF* becomes maximal for a buffer layer of about 75 nm. With a buffer layer at the p-i interface, the DRL is situated further in the cell, so more carriers recombine in the middle of the cell, where the defect density is highest, which means that fewer carriers are collected and the current density decreases. Moreover, the *FF* is first increased because more carriers are separated at the p-i interface. Above a certain buffer layer thickness (~75 nm), the DLR is too far from the p-i interface to have an influence on the recombination there but it starts to influence the i-n interface and the *FF* diminishes.

If the DRL cannot be avoided, it is better to situate it within the first quarter of the intrinsic layer. The *FF* is indeed optimum around 75 nm buffer thickness, V_{OC} is more or less constant and J_{SC} is decreasing.

To understand the effect of the thickness of the DRL on the cell performance, we compare two cells that have a buffer layer of 10 nm; the thickness of the DRL is respectively 5 nm and 30 nm. The band diagram of these cells at thermal equilibrium is presented in Figure 5. The DRL thickness has a little influence on the band diagram in the buffer layer, but in the ETP layer we can see that the thinner the DRL, the less strong the slope of the band. The DRL thickness does not influence the band diagram after 200 nm in the cell. Close to the p-i interface, the internal electric field is stronger for the cell with a thick DRL (see figure 6). This means that the carriers are swept away from this region faster than in the cell with a thin DRL. However, the J_{SC} and the *FF* are lower. We believe that this is due to the fact that more carriers are trapped or recombine in the DRL.

The presence of the DRL influences the current collection not only in this layer, but also in the rest of the cell. Deeper in the cell, the electric field is higher for cell with a thin DRL, which allows more carrier collection and thus a higher J_{SC}.

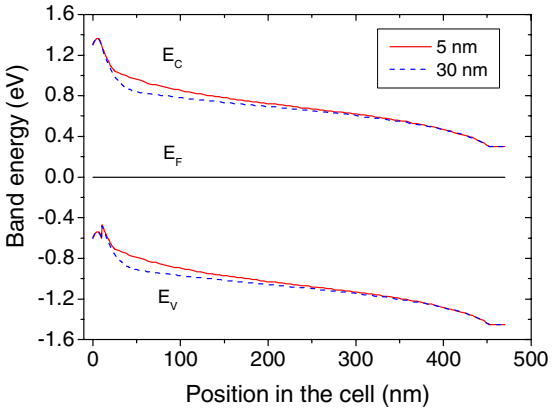

Figure 5. Band diagram of the simulated cells at thermal equilibrium with resp. a 5 and 30 nm thick DLR. The buffer layer is 10 nm thick.

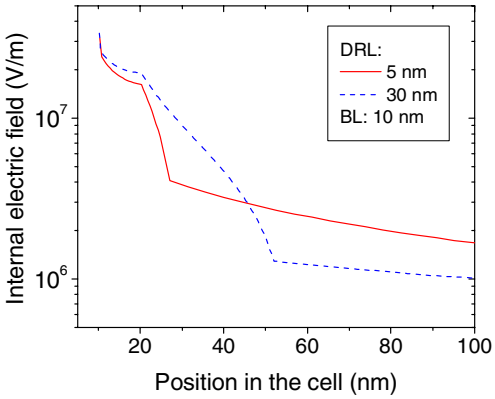

Figure 6. Internal electric field distribution for cells with resp. a 5 and 30 nm thick DRL. The buffer layer is 10 nm thick.

CONCLUSIONS

We have carried out two series of simulations. The first series shows that the incorporation of a buffer layer at the p-i interface increases the performance of the cell by augmenting the internal electric field at the interface and shifting the defect-rich layer (DRL) further in the bulk of the cell away from the sensitive p-i interface.

The second set of simulations shows that a thicker DRL suppresses the performance of the cell. The DRL has an opposite competing effect with the buffer layer. The simulations also show that if the DRL is situated close to the i-n interface its thickness has a strong influence on the *FF*, which is clearly lower for a thicker DRL. This means that a larger defective layer enhances the recombination at the i-n interface.

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