Materials Science Forum Vols. 457-460 (2004) pp. 3-8
online at http://www.scientific.net

Silicon Carbide Crystal and Substrate Technology: A Survey of Recent Advances

H. McD. Hobgood, M. F. Brady, M. R. Calus , J. R. Jenny, R. T. Leonard, D. P. Malta, St. G. Müller, A. R. Powell, V. F. Tsvetkov, R. C. Glass, and C. H. Carter, Jr

Cree, Inc., 4600 Silicon Drive, Durham, NC 27703 USA

Keywords: silicon-carbide, PVT, seeded sublimation, crystal, substrate, wafer, diameter, defects, micropipe, dislocations, stress, purity, resistivity, semi-insulating

Abstract. The quest of driving SiC toward the realization of its full potential as a semiconductor material continues in many organizations world-wide. R&D and manufacturing efforts continue to address issues of scale-up of wafer size, improvements in wafer shape and surface characteristics, reduction of background impurities in bulk crystals, controlled uniformity of electrical properties, and reduction and control of crystalline defects. Significant progress has been made in several key areas. Increased manufacturing activity in the production of 3-inch diameter crystals has led to substrates with micropipes densities <30 cm^{-2} in n-type and <80 cm^{-2} in semi-insulating material, and R&D demonstrations of substrates exhibiting micropipe densities <0.5 cm^{-2} in n-type and <5 cm^{-2} in semi-insulating wafers. Developmental 100-mm diameter substrates exhibiting micropipe densities <60 cm^{-2} in both n-type and semi-insulating materials have now been demonstrated. Significant improvement in bulk crystal purity has been achieved with reduction of impurity concentrations below $5 \times 10^{15} cm^{-3}$.

Introduction

The commercial availability of SiC substrates of greater size and improved crystalline quality has fostered an ever increasing interest in the development and manufacture of electronic devices exploiting the unique electrical and thermophysical properties of this wide-bandgap semiconductor. Device applications include: blue, green, and white GaN/InGaN-based LEDs built on conducting SiC substrates; high-frequency high power SiC MESFETs and GaN/AlGaN HEMT devices built on semi-insulating SiC substrates where the compatibility with high quality epitaxy is combined with the high thermal conductivity (~ 5 W/cmK) of SiC for effective thermal management; SiC Schottky diodes and other unipolar SiC switching devices, as well as bipolar devices such as high-voltage SiC PiN diodes-- all built on 4H, n-type, low micropipe density substrates. In this paper, we give an overview of the current state of the art of bulk SiC growth technology by discussing recent advances in the fabrication of large-diameter SiC crystals of improved crystalline quality and purity.

Large-Area SiC Substrates

Large diameter, high quality SiC crystals are challenging to produce. Their successful manufacture to date rests on significant technical advances in the course of the last ten years in the method of seeded-sublimation growth, also termed physical vapor transport (PVT) growth [1]. In this method, the crystal is grown by SiC deposition deriving from Si and C molecular species provided by a subliming source of SiC placed in proximity to the seed wafer. Recently, investigations into potential alternative methods of SiC crystal growth have included high temperature CVD (HT-CVD)[2] and continuous feed (CF-PVT)[3] approaches utilizing Si and C-bearing chemical

reagents injected directly into the growth zone. To date, these two latter developmental approaches have demonstrated substrates with maximum diameters up to 2-inches. A major consideration for the growth of 3-inch and 100-mm SiC crystals is generation of thermoelastic stresses which in unoptimized conditions can exceed the critical resolved shear stress (CRSS) of the SiC resulting in dislocation generation and high levels of residual stress which can lead to cracking. Control of stress is therefore critical. Fig. 1 illustrates 3-inch and 100-mm diameter 4H-SiC substrates grown by Cree, Inc., using the seeded sublimation method. Assessment of these substrates using cross-polarizer birefringence demonstrates the low density of macro-defects and strain associated with these wafers.

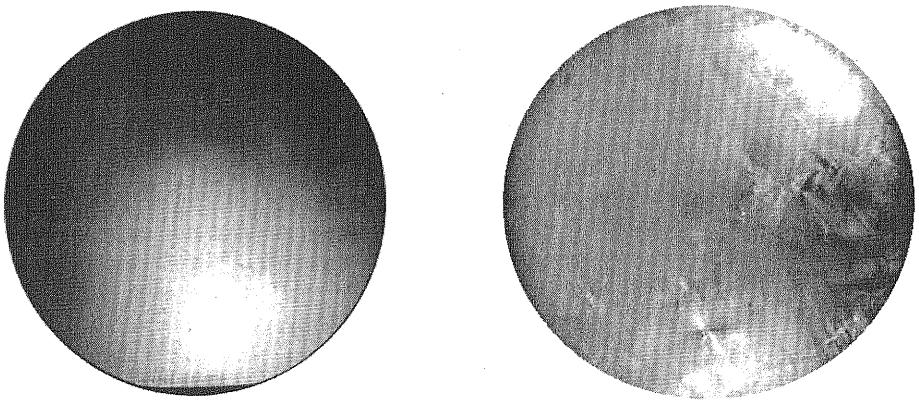


Fig. 1. Cross-polarizer assessment of 3-inch (left image) and 100-mm (right image) 4H-SiC n-type substrates showing overall low density of macro-defects and strain.

Defect Density Improvement

Open core screw dislocations (micropipes) are of particular concern in SiC in view of the detrimental effects of these defects on devices [4]. Increased knowledge of the origins and propagation mechanisms responsible for micropipes has led over the past several years to a steady reduction in their density in SiC substrates (Fig. 2).

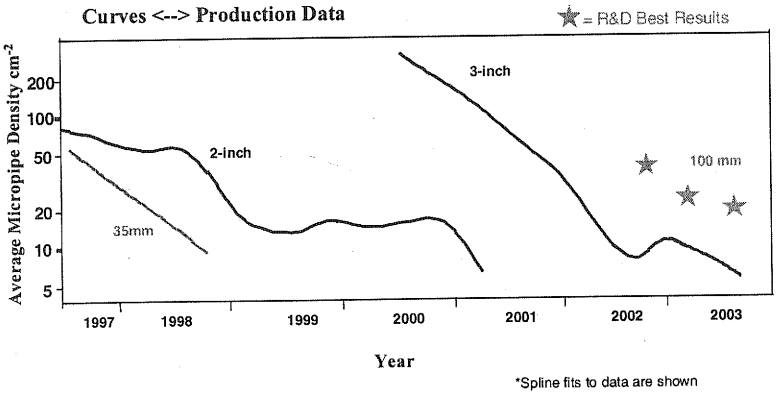


Fig. 2. Average micropipe density (MPD) vs. time for SiC substrates at 35 mm, 2-and 3-inch, and 100 mm diameter. Curves correspond to production data.

The current typical median micropipe density (MPD) in production volumes of 3-inch 4H n-type substrates is now centered round 5 cm^{-2}, with best R&D values of an order of magnitude lower (see Fig. 3).

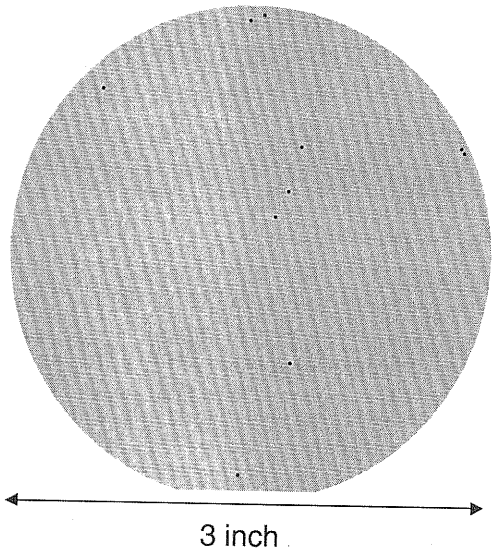


Fig. 3. R&D 3-inch diameter n-type 4H-SiC substrate exhibiting micropipe density of 0.22 cm^{-2}. KOH etching reveals a total of 10 micropipes over the full area of the wafer.

Developmental 100-mm 4H wafers in n- and semi-insulating crystal types have been demonstrated with micropipe densities as low as 22 cm^{-2} and 55 cm^{-2}, respectively [5,6]. The impact of these low micropipe densities on device yield is dramatic. Fig. 4 shows the expected yield of 10 and 100 A Schottky devices built on 3-inch 4H n-type substrates with an average micropipe density of 0.54 cm^{-2} (such as the wafer in Fig. 3) assuming that yield loss is dominated by only micropipe density. Maximum theoretical yields of up to 97% are expected for 10 A devices, while yields of up to 79% are theoretically attainable in 100 A devices.

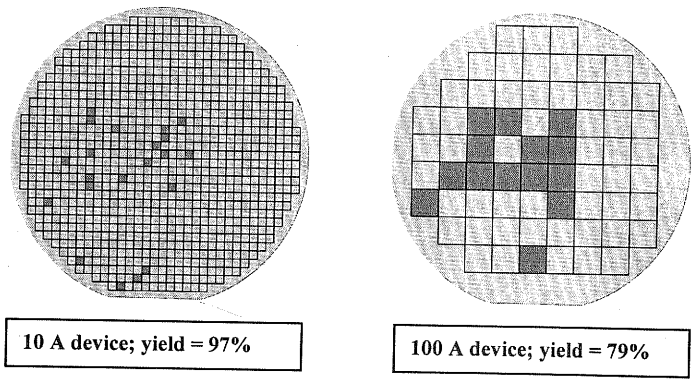


Fig. 4. Expected yield of 10 and 100 A Schottky devices on 3-inch diameter 4H n-type substrates with a micropipe density of 0.54 cm^{-2}, assuming yield loss is due solely to micropipes. Dark cells correspond to failed devices.

Residual defects in low micropipe density wafers are mainly associated with elementary threading screw dislocations, threading edge dislocations, and basal plane dislocations. These various background dislocation features are observable in whole wafer x-ray topographs (Fig. 5). Wafers

subjected to controlled KOH etching exhibit a distribution of shallow etch pits at densities in the 10^4 cm^{-2} range, associated with the general dislocation background (Fig. 6). The radial distribution of

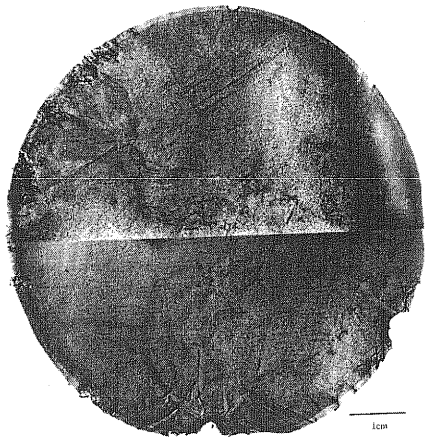
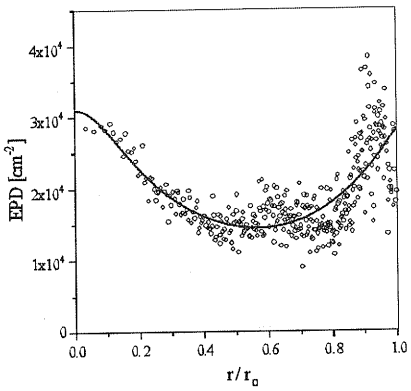


Fig. 5. Synchrotron white beam x-ray image (SWBXT) of a low MPD (< 5 cm^{-2}) 3-inch diameter 4H-SiC wafer. [Image courtesy M. Dudley, SUNY-Stony Brook].



Fig;. 6. Radial distribution for dislocation etch pit density (cm^{-2}) vs. normalized radius across a 4H-SiC wafer with 8 degree off axis orientation.

etch pits across the crystal diameter exhibits a characteristic W-pattern consistent with predictions of the radial dependence in resolved shear stress stemming from excess thermoelastic stresses during growth [7]. These results are supported by the recent observation of slip band features in SiC substrates characterized by KOH etching and TEM techniques [8]. However, as demonstrated in Fig. 5, growth conditions consistent with very little slip in large diameter substrates are possible. Nonetheless, the radial dependence of dislocation etch pits taken together with the the observation of slip in some crystals strongly suggests that thermoelastic stress plays a key role in the generation of dislocations during SiC growth.

Substrate Purity

The electrical behavior of SiC substrates is intimately connected with the purity of the as-grown crystals. In particular, substrate purity in SiC is dominated by the presence of residual nitrogen and boron impurities. Control of these impurities is critical to the manufacture of undoped high purity semi-insulating (HPSI) substrates with uniform, stable semi-insulating properties, used in the fabrication of microwave devices. Current efforts to control nitrogen in seeded sublimation growth have culminated in dramatic reductions of incorporated nitrogen. Figure 8 is a low temperature photoluminescence (LTPL) plot of a PVT-grown HPSI 4H-SiC bulk sample exhibiting a nitrogen concentration of $<1 \times 10^{15}$ cm^{-3} as determined by value of the Q_0 to I_{75} peak ratio, a technique commonly employed in the determination of nitrogen in high purity SiC epitaxial layers [9]. The controlled reduction of shallow level impurities (boron and nitrogen) in HPSI SiC crystals is key to establishing uniform semi-insulating behavior through compensation of shallow impurities by intrinsic deep levels [10]. This technology has now established the commercial availability of 3-inch diameter HPSI 4H-SiC substrates (Fig. 9) while R&D efforts have recently extended the technique to 100-mm diameter HPSI substrates [6].

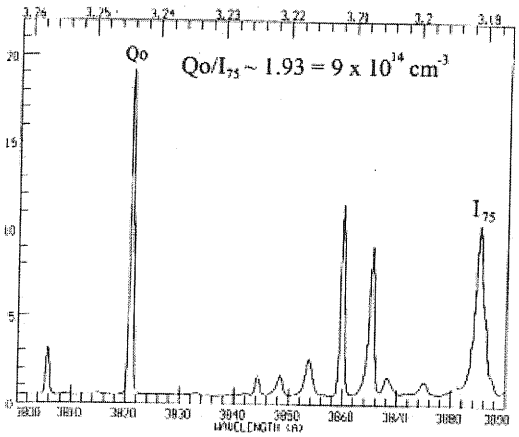


Fig. 8. LTPL plot of a PVT-grown HPSI sample exhibiting a nitrogen incorporation <1E15 cm^{-3}. [Courtesy of W. J. Choyke, Univ. of Pittsburgh].

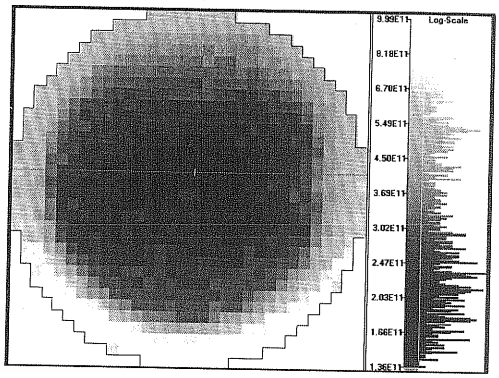


Fig. 9. High resolution resistivity map of a 3-inch diameter 4H-SiC HPSI wafer. The wafer is uniformly semi-insulating with a resistivity > 1E11 ohm-cm.

Summary

Recent progress in the development of the PVT technique for SiC bulk growth has led to the commercial availability of 3-inch diameter substrates of the 4H polytype for both n-type and semi-insulating materials with micropipe densities <30 cm^{-2} and <80cm^{-2}, respectively. Developmental 100-mm diameter substrates exhibiting micropipe densities as low as 22 cm^{-2} in n-type and <55 cm^{-2} in semi-insulating materials have been demonstrated. Crystal purity has been extended down to the 10^{14} cm^{-3} range for residual nitrogen in PVT- grown 4H-SiC crystals. This advance has led to reproducible thermally stable semi-insulating character in undoped 4H-SiC (HPSI) crystals. These advances have contributed to the establishment of SiC substrates as an optimum platform for high brightness optoelectronic devices and for many high power devices operating in both the conventional and high frequencies range.

Acknowledgements The authors gratefully acknowledge the support of the DARPA, AFRL, ONR, and the Title III Office.

References

[1] H. McD. Hobgood et al., Matls. Sci. Forum, Vols. 338-342 (2000), p. 3.
[2] A. Ellison, et al., Matls. Sci. Forum, Vols. 433-436 (2003, p. 33.
[3] D. Chaussende, et al., Matls. Sci. Forum, Vols. 433-436 (2003), p. 25.
[4] P. G. Neudeck and J. A. Powell, IEEE Electron Dev. Lett. 15 (1994), p. 63.
[5] A. R. Powell, et al., Matls. Sci. Forum, this volume.
[6] J. R. Jenny, et al., Matls. Sci. Forum, this volume.
[7] St. G. Müller, et al., Matls. Sci. & Eng., B80 (2001), p. 327.
[8] S. Ha, M. Skowronski, W. M. Vetter, and M. Dudley, J. Appl. Physics, 92 (2002), p. 778.
[9] I. G. Ivanov, et al., J. Appl. Phys., 80 (1996), p. 3504.
[10] J. R. Jenny, et al. J. Electronic Matls., 31 (2002), p. 36.