



## Formation of Semiconducting ZnO Nanowires Using Dip-Pen Nanolithography and Step Edge Decoration Approach

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We demonstrate the fabrication of a semiconducting (SC) ZnO nanowire (NW) using a dip-pen nanolithography (DPN) incorporated with a “step edge decoration” technique, where a  $Zn(CH_3COO)_2 \cdot 2H_2O \cdot 2$ -methoxyethanol solution is used to form the ZnO NW. Notably, the SC ZnO NW is position controllable to a precision of several nanometers. The semicircular ZnO NW with a diameter of 30 nm exhibits *n*-type field effect transistor behavior.

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A nanowire (NW) with inherent axial confinement and a large aspect ratio between its diameter (on the order of nm) and length (on the order of  $\mu m$ ) is useful in the design of nanoscale devices such as field effect transistors (FET), sensors, and building blocks.<sup>1-5</sup> NWs have been successfully synthesized in two ways: bottom-up and top-down approaches.<sup>4,5</sup> Semiconducting NWs demonstrate novel electrical properties quite different from those of the bulk materials due to a low electron density and small effective mass.<sup>4,5</sup> In particular, ZnO nanowires have been grown by vapor-liquid-solid growth,<sup>6-8</sup> catalyst-free,<sup>9</sup> hydrothermal,<sup>10</sup> templates,<sup>11-13</sup> and terrace<sup>14,15</sup> methods.

Controlling the positioning of NWs to a precision of a few nanometers is crucial for developing NW-based devices. Dip-pen nanolithography (DPN) is a useful method to fabricate NWs or nanodots with precise position and size control using various materials such as polymers, metals, semiconductors, and ferroelectric materials.<sup>16-20</sup> Recently, the DPN has been used as biomimetic crystallization nanolithography using a atomic force microscopy cantilever for a DPN pen.<sup>20</sup>

In this study, we report the fabrication of a SC ZnO NW using the DPN with a  $Zn(CH_3COO)_2 \cdot 2H_2O \cdot 2$ -methoxyethanol solution, where the ZnO NW is aligned along a terrace edge on a sapphire substrate. Notably, step edge decoration techniques enable to pen a NW along the terrace edge because the edges are energetically favorable for the crystallization of adatoms.<sup>3,21</sup> In addition, the DPN ZnO NW is well-localized along the terrace edge due to a large lattice misfit of about 15% between the ZnO and sapphire substrate. The DPN SC ZnO NW as a conducting channel exhibits *n*-type FET characteristics.

Figure 1 shows the schematic serial processes to fabricate a DPN ZnO NW in the DPN incorporated with step edge decoration techniques. Figure 1a shows terraces on the surface of the sapphire substrate which were prepared by annealing a miscut single crystal (0001) sapphire substrate for 1 h at 1200°C. Note that the mean height of the terrace edges is about 1.3 nm which corresponds to half of or equal to a lattice unit.<sup>3,21</sup> After coordinating the surface of the sapphire using an AFM image, we penned ZnO NW along a terrace edge with  $Zn(CH_3COO)_2 \cdot 2H_2O \cdot 2$ -methoxyethanol solution<sup>22</sup> as illustrated in Fig. 1b, where a  $Si_3N_4$  DPN tip with a diameter of about 10 nm was used at a speed of about 300 nm/s. The DPN ZnO NW was kept at atmosphere for 24 h to slowly dry the solvent inside it. To crystallize the ZnO, the NW was annealed under a 100% oxygen gas environment for 1 h at 550°C. To fabricate a DPN ZnO NW FET, we placed two Au electrodes as a source and drain at both ends of the NW as shown in Fig. 1c. A conducting atomic force microscopy (AFM) tip was used as a gate, where the distance between the tip and ZnO NW was 30 nm.

Figure 2 shows AFM images of the terraces on the sapphire substrate (a) with and (b) without the DPN ZnO NW. To anneal the sapphire substrate for 1 h at 1200°C enables to form highly uniform terraces on the surface, where the mean interval and height are about 100 and 1.3 nm. Note that the surface roughness of the sapphire substrate is smaller than 0.4 nm. We believe that the atomically flat surface of the substrate is crucial to form the DPN ZnO NW.

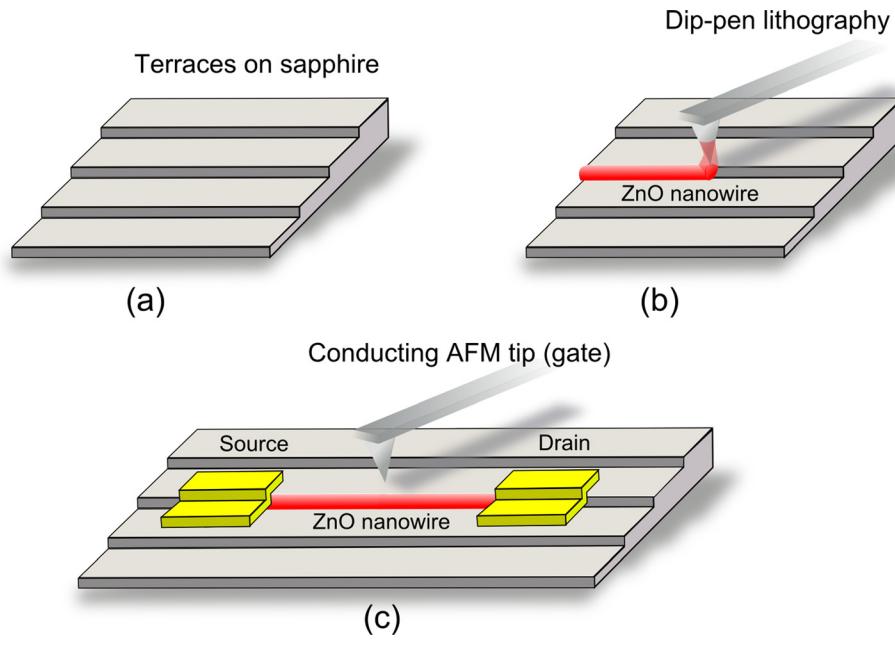
Figure 2b shows the AFM image of the ZnO NW aligned along the terrace on the sapphire substrate. The diameter of the semicircular DPN ZnO NW was about 30 nm, which is smaller than those observed in previous DPN NW studies.<sup>19</sup> Note that a *n*-type dopant of Al was mixed with the  $Zn(CH_3COO)_2 \cdot 2H_2O \cdot 2$ -methoxyethanol solution,<sup>23</sup> thus the *n*-type ZnO NW was formed by the DPN processes. Figure 3c shows an AFM image of a few DPN ZnO NWs formed along the terraces of the sapphire substrate where the diameter of the ZnO NWs is about 50 nm, which indicates that the DPN processes are reproducible to fabricate ZnO NWs.

Figure 3a shows a scanning electron microscopy (SEM) image of the DPN ZnO NW FET with two Au electrodes, where the length of the NW FET was about 2  $\mu m$ . The FET device consists of the ZnO NW used as a carrier channel, the left and right Au electrodes as the source and drain, respectively, and a Pt-coated  $Si_3N_4$  AFM tip with a diameter of 30 nm as a gate electrode (not shown in the figures). To apply a gate voltage to the NW, we placed an air gap of about 30 nm between the conducting AFM tip and the NW as shown in Fig. 1c. Figure 3b shows the source-drain current ( $I_{SD}$ ) of the ZnO NW FET as a function of gate voltage ( $V_G$ ), where the source-drain voltage ( $V_{SD}$ ) was set at 1.0 V for the measurements. The  $I_{SD}$  -  $V_G$  curve indicates that the DPN SC ZnO NW was a channel with *n*-type carriers (electrons).

We estimate the electron mobility of the ZnO NW  $\mu \sim 3 \times 10^{-6} m^2 V^{-1} s^{-1}$  from the  $I_{SD}$  -  $V_G$  characteristics. Here, we use the formula<sup>24</sup>  $I_{SD} = \mu \times C (V_G - V_t) \times V_{SD} / L_G^2$ , where  $V_t = 5.55$  V is the threshold voltage and  $L_G = 30$  nm is the gate length (*i.e.* the diameter of the Pt-coated  $Si_3N_4$  AFM tip). Note that the AFM tip is assumed a circular plate for simplicity. To estimate the capacitance  $C$  between the AFM tip and the ZnO NW,  $C \sim 2\pi\epsilon_0 \times L_G / \ln[(t+a+((t+a)^2 - a^2)^{1/2})/a]$  is used,<sup>24</sup> where  $\epsilon_0$  is the permittivity of the vacuum,  $t = 30$  nm is the air gap thickness, and  $a = 15$  nm is the radius of the ZnO NW. The electron mobility in this study is smaller by 2 and 3 orders of magnitude than that in previous results.<sup>25,26</sup> Figure 3c shows SEM energy dispersive spectrometer (EDS) data of the *n*-type ZnO NW where the EDS peaks at about 0.5, 1, and 1.5 keV correspond to O, Zn, and Al, respectively.

From the FET characteristics, we confirm the following: (i) The DPN ZnO NW processes in this study provide a promising solution for the precise position control of a NW. (ii) The DPN SC ZnO NW on a terrace edge is a well-defined continuous NW without any electrical disconnection. (iii) The DPN SC ZnO NW might provide a

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**Figure 1.** (Color online) Schematics illustrate the dip-pen nanolithography (DPN) processing of a semiconducting ZnO nanowire (NW): (a) Formation of well-aligned terraces on a sapphire substrate. (b) The DPN to form a ZnO NW with a  $\text{Zn}(\text{CH}_3\text{COO})_2\text{-}2\text{H}_2\text{O}\text{-}2\text{-methoxyethanol}$  solution. (c) Formation of two Au electrodes at both ends of the DPN ZnO nanowire. The conducting AFM tip is used as a gate electrode.

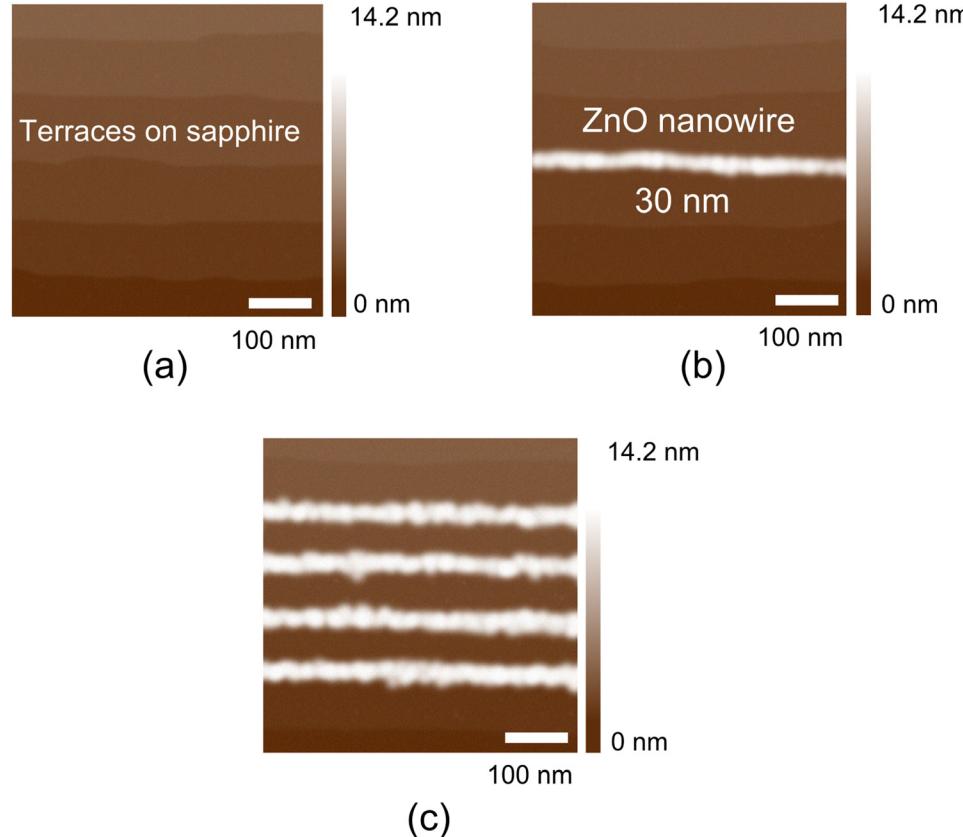
potential as a conducting channel in various SC devices such as hydrogen gas sensors and ethanol sensors.

In conclusion, we demonstrated the fabrication of ZnO NWs on the step edges of a sapphire substrate using the DPN, where a  $\text{Zn}(\text{CH}_3\text{COO})_2\text{-}2\text{H}_2\text{O}\text{-}2\text{-methoxyethanol}$  solution was used to form the ZnO NWs. The DPN provided position controllability with a precision of several nm to form the semicircular ZnO NW with a diameter of 30 nm. The ZnO NW exhibited *n*-type FET behavior with

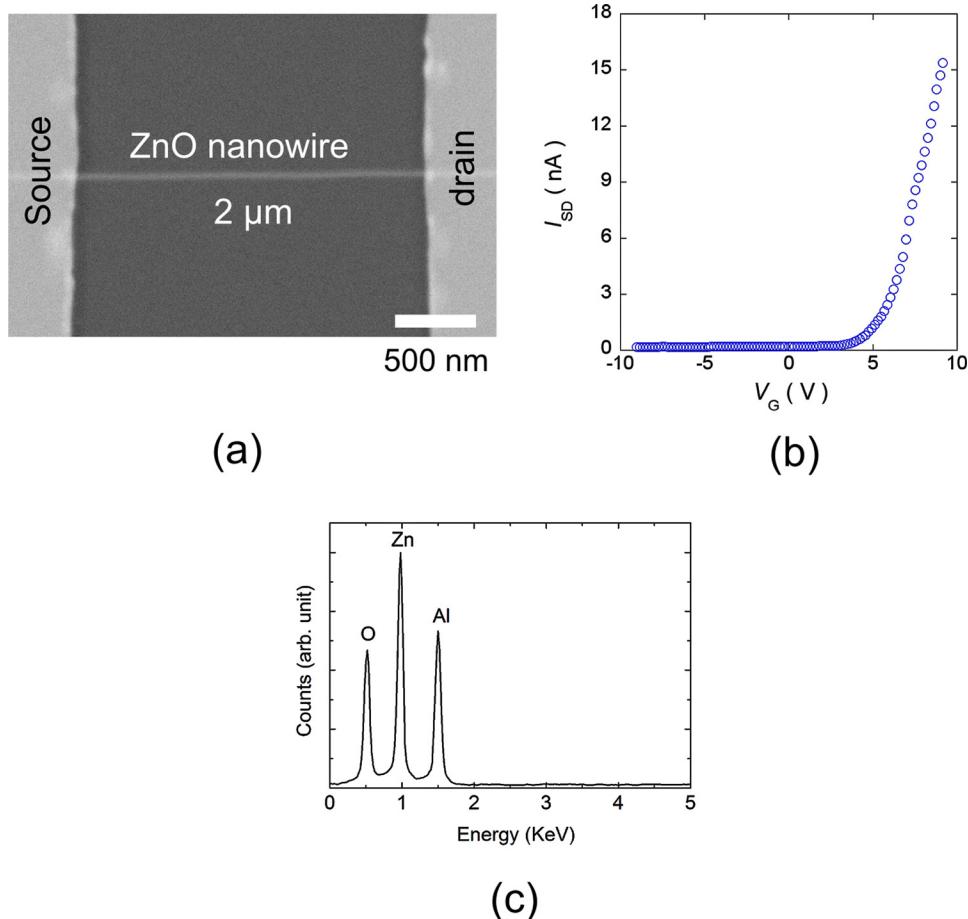
an electron mobility of about  $3 \times 10^{-6} \text{ m}^2 \text{ V}^{-1} \text{ s}^{-1}$ , where the conducting AFM tip was used as a gate.

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**Figure 2.** (Color online) AFM images: (a) Terraces on a (0001) sapphire substrate. Well-aligned terraces exhibit the mean interval of about 100 nm. (b) The DPN ZnO NW is formed along a terrace edge of the sapphire substrate where the diameter of the NW is about 30 nm. (c) A couple of DPN ZnO NWs with a diameter of about 50 nm are formed along the terraces of the sapphire substrate.



**Figure 3.** (Color online) FET characteristics of the DPN ZnO NW: (a) An SEM image of the DPN ZnO NW with the source and drain electrodes. (b) The source-drain current  $I_{SD}$  of the DPN ZnO NW FET as a function of the gate voltage. The conducting AFM tip located at the center of the NW (not shown in the figure) was used as the gate electrode. The FET device exhibits *n*-type channel behavior with an electron mobility of about  $3 \times 10^{-6} \text{ m}^2 \text{ V}^{-1} \text{ s}^{-1}$ . (c) SEM energy dispersive spectrometer (EDS) data of the ZnO NW exhibits peaks corresponding to O, Zn, and Al.

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