

Characterization of Spontaneously Bonded Hydrophobic Silicon Surfaces

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ABSTRACT

The choice of surface treatment prior to silicon wafer bonding is crucial both for the reliability of the bonding process and the electrical properties of the bonded structure. In the case of silicon direct bonding for manufacturing of buried electrical junctions, the bonding step is particularly critical for accurate and reproducible results. In this work, the attraction between HF-etched surfaces and the effect of a following water rinse were investigated by studying the bonding spontaneity, velocity of the initial bonding wave, and the electrical properties of the bonded junctions. Spontaneous bonding occurred when no subsequent water rinse was made after the HF-etch, while water-rinsed wafers did bond only with the help of an applied pressure and also ended up with more voids. The highest contact wave velocity, together with good electrical properties, was obtained for surfaces treated in a 10% solution of HF in water, without subsequent water rinse. For unipolar bonded junctions annealed at 600°C, no influence of the bonded interface was found on the electrical characteristics. In contrast, samples annealed at 800°C exhibited slightly nonlinear current *vs.* voltage characteristics and a larger dynamic resistance. For water-rinsed samples, annealed at 800°C, the dynamic resistance showed a larger spread, indicating a lower reproducibility as compared to nonrinsed samples.

A growing interest has been shown for direct bonding of silicon wafers without any interfacial oxide, for example in applications such as high power devices,¹ sensors, and micromechanical devices.² Silicon direct bonding has also been presented as an alternative to epitaxial layers. It has earlier been reported that hydrophilic surfaces are necessary for spontaneous bonding to occur, and that hydrophobic surfaces can be bonded only if pressure is applied to the wafer pair.^{3,4} Hydrophilic bonding always results in an interfacial oxide, leading to an unacceptably high density of electron states at the interface.⁵ A nonspontaneous bonding, on the other hand, makes the procedure more difficult and less compatible with a batch-process.

In contrast, we have previously shown that spontaneous bonding can be achieved even for hydrophobic surfaces, with a proper choice of pretreatment.⁶ The treatment should, according to this, not include a water rinse after the HF-dip. To further investigate this issue, we have here studied the initial bonding behavior of silicon surfaces treated in different aqueous HF-solutions of different concentrations, and the effects of a following water rinse. This was done by observing the initial contact wave, using transmitted IR light, and by measuring the resulting bond strength. The treatment prior to bonding will surely influence the electrical properties of the bonded structures. In particular, a water rinse can affect the characteristics, since it may give rise to an interfacial oxide, giving a high density of states as in the case of hydrophilic bonding.⁵ We have measured the current density *vs.* voltage characteristics of bonded unipolar Si-Si junctions, after annealing at two different temperatures. Also the current *vs.* temperature characteristics were measured, to shed some light on the nature of the current transport across the interface.

Experiments and Results

The silicon wafers used in all experiments were 3 in., n- and p-type, [100]-oriented, having a thickness of $380 \pm 5 \mu\text{m}$ (Wacker, FZ, 10 to 12 $\Omega\text{-cm}$). Prior to bonding, the wafers were etched for 1 min in aqueous solutions of hydrofluoric acid (HF), in some cases followed by a rinse in DI water. All wafers were then blown dry in N_2 before bringing the surfaces into contact.

Contact wave velocity and bond strength.—The wafers used for the investigations of the initial contact wave were etched 1 min in aqueous solutions of HF at different concentrations, ranging from 1 to 49%. Some of the samples were carefully rinsed in DI water after etching (henceforth

called rinsed samples), while the others (nonrinsed samples) were only blown dry in N_2 .

As the wafers are contacted, the contact area spreads like a wave over the whole bonding area. The contact wave was observed, and its velocity was measured, using an IR camera and a video setup. This method has earlier been presented by Spierings and Haisma.⁴ A slight pressure with the tweezers at the wafer edge is normally required to initiate the wave. If the contact area then grows without further help, the bonding is referred to as spontaneous. The process is schematically illustrated in Fig. 1.

The measured contact wave velocity *vs.* the concentration of the HF-solution is given in Fig. 2. When no water rinse was performed after the etch, all samples showed spontaneous contact waves. The highest contact wave velocity, 1.5 cm/s, was received after etching in the 10% solution. In comparison, Spierings and Haisma reported a velocity of 2 cm/s for hydrophilic wafers.⁴ Water-rinsed samples, in contrast, did bond only with the help of an applied pressure and also had a tendency to end up with more voids.

The bond strengths at room temperature were measured by determining the surface energy, using the theory of crack propagation, as first introduced by Maszara *et al.*⁷ A thin blade, having a thickness of 50 μm , was inserted between the two wafers, and the crack length was measured

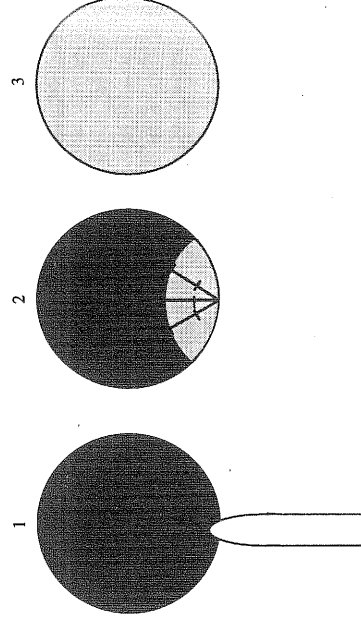


Fig. 1. Schematic illustration of a traveling contact wave, as seen in transmitted IR-light. 1, A slight pressure at the wafer edge is normally required to initiate the wave. 2, The wave proceeds across the wafer at a certain speed until, 3, completely sealed.

by observing the transmitted IR-light as described above. From this the surface energy can be calculated.⁷

With this method, we could not see any correlation between the room temperature bond strength and the contact wave velocity, in contrast to what has earlier been presumed by, e.g., Spierings and Haisma.⁴ The calculated surface energies are plotted in Fig. 2, together with the wave velocities. The energies were between 12 and 20 mJ/m² for all samples, which lies within the experimental errors. As a comparison, Maszara *et al.* reported bond strengths in the range of 60 to 85 mJ/m² for room temperature bonded hydrophilic, oxidized wafers.⁷

Electrical characteristics.—The samples used for electrical characterization were unipolar junctions made by bonding of n-type Si-wafers (10 Ω -cm). The wafers were etched in 10% HF, with and without a subsequent water rinse, prior to bonding. This pretreatment was chosen on the basis of the previous experiments, showing that 10% HF gives the best initial bonding behavior, regarding wave velocity and void density. All bonded samples were first annealed at 600°C for 30 min in N₂-ambient. The backs of the wafers were heavily doped with phosphorus to ensure ohmic contacts to aluminum. After implantation, the samples were divided in two groups and annealed for another 30 min, at 600 and 800°C respectively. A schematic view of the junction is shown in Fig. 3.

The instrumentation for the electrical characterization consisted of an HP 4145 parameter analyzer and an HP 4140 pA meter/dc voltage source connected to an HP 9000 computer. During the measurements at different temperatures, the samples were mounted in a Leyboldt refrigerator-cryo unit ROK 10-300 with a top-loading sample chamber DN20. The temperature was measured and controlled by a programmable temperature regulator LTC 60.

To evaluate the influence of the water rinse and the different annealing temperatures, the current *vs.* voltage characteristics of the unipolar samples was measured. If the influence of the bonded silicon-silicon interface on the current transport across the samples can be neglected, one would expect a linear current *vs.* voltage characteristic with a slope corresponding to the sum of the resistances of the bulk silicon, the ohmic contacts and the measurement setup. A barrier at the bonded interface would be seen as a nonlinearity or a resistance too large to be explained by the resistances mentioned above. There is, however, another possible source of such a phenomenon. If the contact between the metal and the silicon is rectifying, or at least not purely ohmic, nonlinear current *vs.* voltage characteristics would appear. The different annealing temperatures (600 or 800°C) make it important to check out further the metal-silicon junctions to avoid any influence of a different degree of electrical activation of the dopants after the heat-treatments. To investigate the metal-silicon junctions, samples consisting of a silicon wafer with aluminum contacts on both sides were prepared with annealing at 600 or 800°C. The measurements on these devices showed no asymmetries, nonlinearities, or anomalous resistance values. Since the used wafers had one polished and one lapped side, one of the contacts of the reference samples is on the polished side, while the both contacts are on the lapped sides on the bonded samples. An influence of this difference would have been seen as an asymmetry in the current *vs.* voltage characteristic of the reference samples. No such asymmetry was observed. Based on these results it was concluded that the metal-silicon junctions can be neglected as a source of nonlinearities in the current *vs.* voltage characteristics of the present samples. Any nonlinearity present in the current *vs.* voltage characteristic of a bonded sample must thus be a result of the bonded interface.

In Fig. 4, the current density *vs.* voltage characteristics of four bonded samples are shown. The samples are representative for the four groups of samples processed with and without water rinse and annealed at 600 or 800°C. The current density was calculated using the geometric area of the samples, about 9 mm². The true area may be smaller as a result of micro-voids at the bonded interface, but no at-

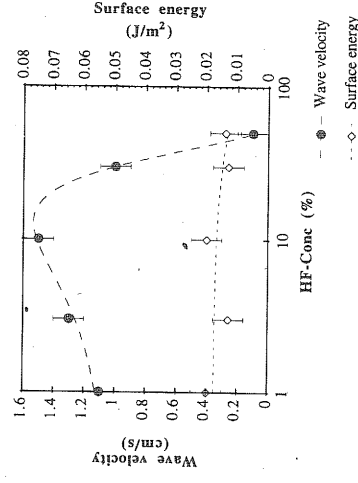


Fig. 2. The contact wave velocity and surface energy of the bond (at room temperature), for hydrophobic wafers etched in aqueous solutions of HF vs. the concentration of the HF-solution.

tempts to calculate a true area were made. All current density *vs.* voltage characteristics were symmetric with respect to the polarity of the applied bias. The dynamic resistance, dV/dI , as a function of the applied voltage was calculated, to enhance the sensitivity to small nonlinearities in the current density *vs.* voltage characteristics. Figure 5 demonstrates dV/dI *vs.* the applied voltage for the samples in Fig. 4. In Fig. 5 the difference between samples annealed at 600 and 800°C can be clearly seen. The observed nonlinearity at voltages smaller than approximately 0.5 V in the samples annealed at 800°C cannot be detected in the samples annealed at 600°C. The smaller absolute value of the current in the samples annealed at 800°C makes it more sensitive to noise and other measurement errors. Taking the derivative dV/dI further increases this sensitivity. As a result the curves of Fig. 5 corresponding to this group of samples show a more noisy behavior as compared to the group of samples annealed at 600°C. It was not possible to detect any influence of the bonded interface on the current density *vs.* voltage characteristic in the samples prepared at 600°C. This is true independently of whether the wafers were rinsed in water or not after the HF-dip. The current density *vs.* voltage characteristics of the samples prepared using an anneal at 800°C, exhibited a higher resistance as well as nonlinearities, as shown in Fig. 4 and 5. The results are summarized in Table I.

In Table I also the standard deviations of dV/dI are given. As can be seen, dV/dI showed a larger spread in the case of water-rinsed samples annealed at 800°C, as compared to the other groups of samples. The water rinse cannot be the only explanation to this, since the large difference in standard deviation between rinsed and nonrinsed samples can only be seen for the samples annealed at 800°C and not at 600°C. Probably some defects, introduced by the water

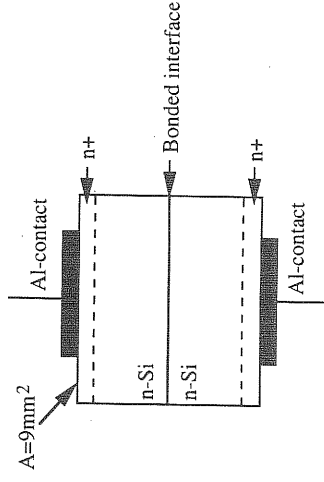


Fig. 3. Schematic drawing of a bonded unipolar Si/Si-junction. The wafers were etched in 10% HF, with and without subsequent water rinse, prior to bonding. The backs of the wafers are heavily doped with phosphorus to ensure ohmic contacts to aluminum. The area of the junction is 9 mm².

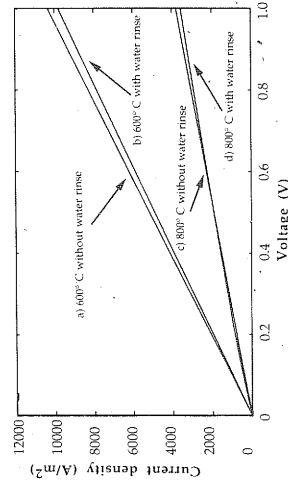


Fig. 4. Current density vs. voltage characteristics for four different bonded n-type/n-type samples: (a) sample prepared without water rinse and annealing at 600°C; (b) sample prepared with water rinse and annealing at 600°C; (c) sample prepared without water rinse and annealing at 800°C; (d) sample prepared with water rinse and annealing at 800°C.

rinse, become active between 600 and 800°C, which influence the electrical characteristics for the bonded junction.

To further elucidate the nature of the current transport, the current density across the samples was measured at a constant small voltage, while the temperature was changed from 50 to 300 K. In Fig. 6, Arrhenius plots for the different groups of samples are shown. At the lower temperatures, different activation energies, E_a , can be observed. For the samples annealed at 600°C the decrease with temperature in the current density, seen at low temperatures, is of the same order ($E_a \approx 0.04$ eV) as for the freeze-out of shallow donors in the silicon bulk.⁸ The decreasing current in these samples is thus a result of the decreasing number of ionized phosphorus atoms in the silicon bulk when the temperature is lowered. For the samples annealed at 800°C, on the other hand, the current starts to decrease at a higher temperature. This rules out the possibility of explaining the behavior by donor freeze-out. Also, the slope of the curve is too large to fit into this model. Obviously another explanation has to be found. If the current across these samples were controlled by thermal emission across a potential barrier at the bonded interface, one would expect such a temperature dependent current. The presence of a potential barrier in the samples annealed at 800°C but not in those annealed at 600°C correlates well to the observed presence of nonlinearities in Fig. 4 and 5. From the slope of the curve in Fig. 6 the activation energy is found to be about 0.1 eV, giving the fingerprint of a potential barrier of the approximate height 0.1 V at the bonded interface.

Discussion

Influences on the initial contact wave.—Etching and removal of the silicon surface oxide in an aqueous solution of hydrofluoric acid, results in hydrogen-termination of about 90% of the surface dangling bonds.⁹ The initial attraction between the surfaces, is believed to originate from van der Waals forces.¹⁰ As these forces do not reach far, the surface atoms of the two wafers must come very close to each other. Therefore, there are mainly two things that can

Table I. A summary of the results from the room temperature bonding observations and the current vs. voltage measurements, related to two process parameters: the water rinse subsequent to HF-etching (10% HF) and the anneal temperature. The dynamic resistance, dV/dI , and the anneal mean values taken at 1.0 V. The standard deviation, $s(dV/dI)$, represents statistics from six samples at 600°C, and 14 samples at 800°C. The activation energy, E_a , is calculated from Fig. 6 at low temperatures.

10% HF-etch and:	Annealing temp. (°C)	Spontaneous bonding?	dV/dI ($\mu\Omega\text{-m}^2$)	$s(dV/dI)$ ($\mu\Omega\text{-m}^2$)	E_a (eV)
No water rinse	600	Yes	106	11	≈ 0.04
Water rinse	600	No	116	14	≈ 0.04
No water rinse	800	Yes	263	39	≈ 0.1
Water rinse	800	No	345	137	≈ 0.1

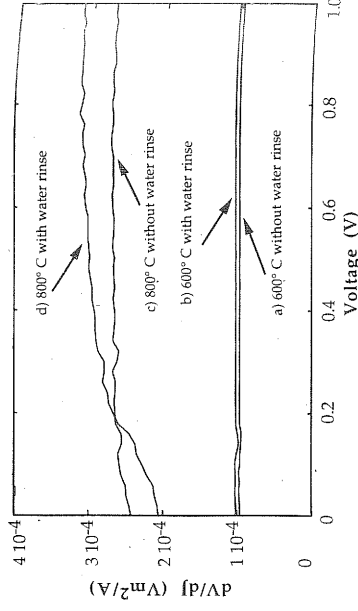


Fig. 5. The dynamic resistance (dV/dI) vs. the applied voltage for the four different bonded n-type/n-type samples of Fig. 4: (a) sample prepared without water rinse and annealing at 600°C; (b) sample prepared with water rinse and annealing at 600°C; (c) sample prepared without water rinse and annealing at 800°C; (d) sample prepared with water rinse and annealing at 800°C.

influence the initial contact wave. First, the surface roughness, on the atomic scale, is to be considered. A rough surface would prevent the spreading of the contact area. Second, any presence of submicron particles or macromolecules on the surfaces will have deleterious effects on the bonding behavior. In the case of surface particles, they will be the overwhelming reason why spontaneous bonding cannot be achieved, since they are considerably larger than the surface roughness.

The surface roughness is probably dependent on the HF concentration, which gives an explanation to the results presented in Fig. 2. The etch rate of silicon in aqueous HF-solutions is very small, but measurable, and has been measured to be higher in a diluted solution than in a highly concentrated solution.¹¹ An explanation is that the etching is believed to proceed in two steps: slow oxidation of the silicon surface by the hydroxyl ions (OH^-), and then a fast removal of the surface oxide by HF. Hence, the etch rate, and thus the resultant surface morphology, is depending on the OH^- -concentration.^{11,12} Hessel *et al.* have studied the influence of pH in the HF solution on the silicon surface morphology. They found that the etch rate of silicon in concentrated HF solutions (pH 1) is so small that the silicon surface is basically inert, while the roughness and topography of the original silicon/native-oxide interface is maintained.¹³ This might explain the observations made in this work, i.e., that the highly concentrated HF solution (49%, pH ≈ 1) only removes the native oxide, while the more diluted solution (having a pH of about 2) etches the

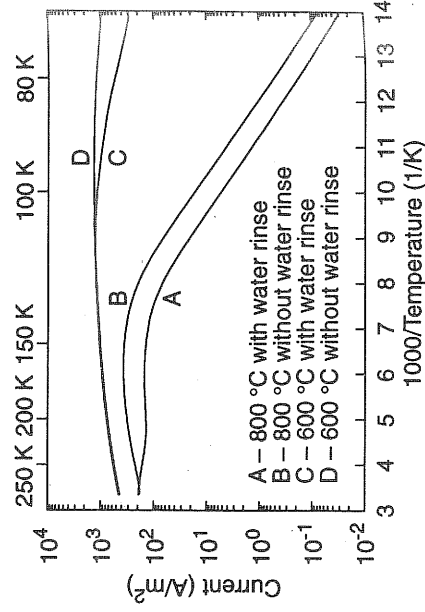


Fig. 6. The logarithm of the current density across bonded n-type/n-type samples vs. $1000/T$, measured at a constant voltage of 0.05 V: A, sample prepared with water rinse and annealing at 800°C; B, sample prepared without water rinse and annealing at 800°C; C, sample prepared with water rinse and annealing at 600°C; D, sample prepared without water rinse and annealing at 600°C.

Hydrophobic Si-wafer



current density *vs.* voltage characteristic at room temperature and a thermally activated current at lower temperatures. The characteristics of the 800°C samples show large similarities with the characteristics of hydrophilic samples reported in the literature.^{5,16} The disturbance of the current *vs.* voltage characteristic from the ideal case is, however, much smaller in this case as compared to hydrophilic samples. The reported experimental results for the samples annealed at 800°C can be explained by the presence of a potential barrier at the interface. The height of the potential barrier is about 0.1 V. As discussed in the literature,^{5,16} the potential barrier in bonded Si-Si interfaces is probably caused by interface states and charges. The origin of these states and charges can be structural as well as related to deep or shallow impurities. The presence of a barrier after annealing at 800°C but not after annealing at 600°C is most readily explained by the need of thermal activation of the dominating defect. The defect is thus not active after an anneal at 600°C but becomes active after annealing at 800°C. This behavior of the defects can for instance be compared to the occurrence of thermal donors and the so called "new donors" in SIMOX materials after an annealing at 450 and 750°C, respectively.¹⁷ In the 800°C annealing case the average dynamic resistance of the water-rinsed samples was higher, and the data showed a larger spread, as compared to the nonrinsed samples. This might be explained assuming that the presence of submicron particles, OH⁻ groups, or other coupled molecules, originating from the water rinse, gives rise to a larger amount of thermally activated defects in the bonding interface. The bonded surfaces are, however, hydrophobic for all samples, and the influence on the current transport is much smaller than in the case of bonding hydrophilic surfaces.

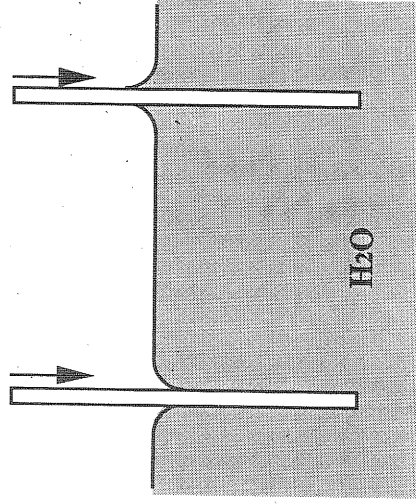


Fig. 7. An illustration of the different situations appearing at the air/liquid interface when immersing a hydrophobic and a hydrophilic silicon wafer in water. The water surface will extend down with the hydrophobic wafer, and thus give rise to particle contamination of the silicon surface. The hydrophilic wafer, in contrast, will slip by surface particles.

silicon surface isotropically, which in this case has a polishing effect.

Although the last HF processing is known to remove surface particles, it has been shown that when immersing a previously HF-treated wafer in DI water, or an HF solution again, the amount of submicron particles on the surface increases considerably.¹⁴ This was attributed to the fact, that when a hydrophobic wafer (unable to wet) passes the air/liquid interface, the liquid surface curves downward. As the wafer is immersed in the liquid, the liquid surface is extended down with the wafer. Particles on the liquid surface are therefore transferred and attached to the wafer surface. A hydrophilic wafer, in contrast, will slip by surface particles, due to the upwardly curved liquid surface.¹⁴ An illustration of this is given in Fig. 7.

Submicron particles on the water surface, originating from the surrounding air even in a clean-room environment, should consequently be the main reason of the observed nonspontaneous bonding of the water rinsed wafers. The hydrophobic wafers get contaminated with a large amount of particles at the very moment when they are immersed into the water bath. When the wafers are brought together, the submicron particles will obstruct the contact wave.

The nonrinsed wafers, on the other hand, are extremely clean and particle-free. The observed differences in bonding behavior for these samples are, according to the above, attributed to the surface roughness.

Electrical properties of bonded junctions.—In the case where a potential barrier is present at the bonded Si-Si interface, the current transport across the bonded junction will be detrimentally affected, resulting in a nonlinear current *vs.* voltage characteristic and/or a high resistance. The use of HF etching prior to wafer contacting (hydrophobic wafer surfaces) has earlier been shown to decrease considerably the potential barrier at bonded Si-Si interfaces, as compared to the case when the silicon wafers are covered with a thin native oxide (hydrophilic wafer surfaces) prior to wafer contacting.^{5,15,16} A model of the hydrophilic unipolar Si-Si junctions, based on the presence of interface states at the boundary between the wafers, causing a potential barrier of 0.2 to 0.5 V, has earlier been proposed.¹⁶ For the samples annealed at 600°C, no barrier could be detected by using current *vs.* voltage measurements, neither at room temperature nor at lower temperatures. In contrast, the current across the samples annealed at 800°C is restricted by a potential barrier, resulting in a nonlinear

Conclusions

Our results show that nearly ideal Si-Si junctions can be made by wafer bonding if the right pretreatment is performed before the bonding step. This method for forming deep buried junctions in silicon is an excellent, low thermal budget alternative to epitaxially grown silicon junctions.

We have shown that spontaneous bonding occurs between hydrophobic wafers etched in aqueous HF-solutions, provided no subsequent water rinse is performed. The highest contact wave velocity was received after etching in 10% HF-solution, without water rinse. The velocity in this case is almost as high as reported for hydrophilic wafers.

Unipolar Si-Si junctions with excellent electrical characteristics have been prepared both with and without wafer rinsing subsequent to the HF-etch, using an annealing temperature as low as 600°C. After annealing at 800°C, a small voltage-dependent dynamic resistance appeared and the current transport at low temperatures was found to be thermally activated. The dynamic resistance also showed a larger spread, indicating a lower reproducibility, for samples rinsed in water and annealed at 800°C.

The spontaneity of the initial bonding is important for process reliability and compatibility with a batch-process, as a spontaneous bonding makes the bonding step easier, and probably gives a lower void density. In many electronic applications, where a high interface density of electron states is intolerable, high quality bonded interfaces without any interfacial oxide and with a low density of interface states are of great interest.

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n-type/
wafer
annealed at
600°C;
at 600°C.

REFERENCES

1. C. Parkes, N. S. J. Mitchell, H. S. Gamble, and B. M. Armstrong, in *Proceedings of EPE-MADEP*, P. Ferraris, Editor, p. 47, Litografia GEDA, Torino, Italy (1991).
2. P. W. Barth, *Sensors Actuators*, **A21-23**, 919 (1990).
3. S. Bengtsson and O. Engström, *This Journal*, **137**, 2297 (1990).
4. G. A. C. M. Spierings and J. Haisma, in *Semiconductor Wafer Bonding: Science, Technology and Applications*, W. Gösele, T. Abe, J. Haisma, and M. A. Schmidt, PV 92-7, p. 18, The Electrochemical Society Proceedings Series, Pennington, NJ (1992).
5. S. Bengtsson and O. Engström, *J. Appl. Phys.*, **66**, 1231 (1989).
6. K. Ljungberg, A. Söderbärg, and Y. Bäcklund, *Appl. Phys. Lett.*, **62**, 1362 (1993).
7. W. P. Maszara, G. Goetz, A. Caviglia, and J. B. McKittrick, *J. Appl. Phys.*, **64**, 4943 (1988).
8. See for instance, S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed., Chap. 1.4, p. 26, John Wiley & Sons, Inc., New York (1981).
9. L. A. Zazzera and J. F. Moulder, *This Journal*, **136**, 484 (1989).
10. Y. Bäcklund, K. Ljungberg, and A. Söderbärg, *J. Microtech. Microeng.*, **2**, 158 (1992).
11. S. M. Hu and D. R. Kerr, *This Journal*, **14**, 414 (1967).
12. G. S. Higashi, Y. J. Chabal, G. W. Trucks, and K. Raghavachari, *Appl. Phys. Lett.*, **56**, 656 (1990).
13. H. E. Hessel, A. Felz, M. Reiter, U. Memmert, and R. J. Behm, *Chem. Phys. Lett.*, **186**, 275 (1991).
14. C. F. McConnell, in *Proceedings of First International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '92*, Leuven, Belgium, Sept. 17-19, 1992.
15. S. Bengtsson and O. Engström, *Jpn. J. Appl. Phys.*, **30**, 356 (1991).
16. S. Bengtsson, G. I. Andersson, M. O. Andersson, and O. Engström, *J. Appl. Phys.*, **72**, 124 (1992).
17. S. Cristoloveanu, J. Pumfrey, E. Scheid, P. L. F. Hemment, and R. P. Arrowsmith, *Electron. Lett.*, **21**, 802 (1985).

High-Selectivity and High-Deposition Rate Tungsten CVD Freed from Chamber Cleaning

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ABSTRACT

A chemical vapor deposition method for tungsten films using a chamber with a cold susceptor is proposed for attaining excellent selectivity and a cleaning-free process. High-rate selective deposition above 1.0 $\mu\text{m}/\text{min}$ using the reduction of tungsten hexafluoride by silane is achieved at a substrate temperature of 210°C by using a cold susceptor chilled by water at room temperature. No deposition of tungsten or by-products on the susceptor surface and the inner surface of the chamber is observed, indicating that the newly developed system is free from cleaning. The deposited tungsten film has the alpha-type structure. The lattice constant of the tungsten is changed by the deposition temperature and the flow ratio of silane to tungsten hexafluoride.

Selective tungsten deposition by chemical vapor deposition (CVD) has played a very important role as a technique for improving planarization in the fabrication of ultralarge scale integrated circuit (ULSI) devices. The selective deposition by low pressure CVD is an established process in the laboratory, but some problems remain to be solved in the mass-production line. The most serious problem is the loss in selectivity during tungsten CVD. It is generally accepted that there is strong correlation between the chamber characteristics and the selectivity performance of the selective tungsten CVD. The maximum thickness of tungsten selectively deposited in the CVD system with a hot-wall chamber has been reported to be about 2000 Å,¹ and the filling ability is not enough for the deep contact hole and deep via hole. Recently, the loss in selectivity has been considerably corrected by utilizing the cold-wall chamber²⁻⁵ and the pretreatment using halogen-based plasma for silicon dioxide surfaces.^{6,7} However, the problem has not been solved perfectly even in the cold wall chamber. Furthermore, the mechanism for the loss in selectivity has not yet been described. It is now known that the tungsten deposition on the interior of the chamber deteriorates the selectivity performance.⁸ Thus, undesirable deposition on the interior of the chamber has been a substantial problem. No deposition on the interior of the chamber is essential in order to maintain the satisfactory selective deposition performance. To avoid this undesirable deposition, primary attention must be focused on the chamber design.

* Electrochemical Society Active Member.

Another matter concerned with this undesirable deposition on the interior of the chamber is that the cold-wall chamber systems have required chamber cleaning. Periodic chamber cleaning using halogen-based plasmas has been widely employed in cold-wall chamber systems. However, the plasma process for chamber cleaning causes loss in selectivity, particle generation, chamber damage, and low throughput. Therefore, a CVD method without deposition on the whole interior of the chamber for the elimination of chamber cleaning is inevitably required.

In this paper, we describe a CVD method freed from the deposition on the whole interior of the chamber. To attain no deposition on the interior of the chamber, a cold susceptor is utilized in this CVD approach. High-rate selective deposition is achieved, which suggests that this newly developed chamber system has the potential for single-wafer processing without chamber cleaning. In addition, an adsorption mechanism of a by-product of the reaction on the thermally grown silicon dioxide surface is discussed.

Experimental

Figure 1 shows the schematic diagram of the CVD chamber with a cold susceptor. We made appropriate modifications to the epitaxial silicon film deposition reactor^{9,10} enabling the selective deposition of tungsten. The substrate was set faceup on the susceptor by the loadlock system with the electrostatic chuck. The substrate was preferentially heated by irradiation of the collimated light of a Xe lamp on the front side of the substrate. The diameter of the light of the Xe lamp was confined by the size of the quartz win-

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Fig. 1