marked decreases in the gate voltages required for a given charge compared to Al_2O_3, SiO_2. This is largely due to the much lower barrier height (1.3 volts)[7] compared to SiO_2 ($\approx$ 4.0 volts).[8]

It is noted that the field in $I(1)$ for appreciable charge storage is in the 10^7 V/cm range. When the outer gate voltage is removed, the field in $I(1)$ due to the stored charge on the inner gate is only 10^6 V/cm or so corresponding to 5×10^{12} charges/cm^2, a large enough charge to detect easily. Since the transport across $I(1)$ is highly sensitive to the field, (2a) and (2b), no charges flow back. The charge loss is actually controlled by the dielectric relaxation time of the sandwich structure,[9] which is very long. When it is desired to discharge the floating gate quickly, it is necessary to apply to the outer gate a voltage about equal in magnitude but opposite in polarity to the voltage which was used for charging. It is evident that net positive charges (loss of electrons) can also be stored in the floating gate if the discharging gate voltages are appropriately chosen in magnitude and duration.

It was mentioned that the stored-charge density of 5×10^{12}/cm^2 was sufficient for easy detection. One of the detection or read-out schemes is to use the surface field effect transistor (MOSFET or IGFET) first fabricated and described by Kahng and Atalla[10] in 1960. For inversion at a silicon surface, the charge required is only about 2×10^{11}/cm^2 for 1 ohm-cm n-type silicon. However, surface-state charges at the silicon-silicon dioxide interface may be as high as 10^{12}/cm^2, depending on the fabrication techniques used. For this reason we have chosen 5×10^{12}/cm^2 as the stored charge required for easy detection. When the Insulated Gate Field Effect Transistor (IGFET) principle is used for read-out, $M(1)$ is now replaced by silicon. This requires a slight correction in the calculation of charge flow through the insulator, but the major features of the results are not expected to be altered significantly. It is to be noted that about one half of the stored charge can be active in creation of the inversion layer since the other half resides near the $M(2)$-$I(2)$ interface due to Colombic repulsion.

To check the feasibility, a floating gate device has been fabricated using an IGFET as shown in Fig. 3(a). The substrate is an n-type silicon, 1 ohm-cm, and ⟨111⟩ oriented. $I(1)$ is a 50 Å SiO_2 thermally grown in a dry oxygen furnace. $M(2)$ and $I(2)$ are Zr (1000 Å) and ZrO_2 (1000 Å), respectively. $M(3)$ and the ohmic contact metals are aluminum deposited in a vacuum system. Fig. 3(b) is another version of the floating gate device using a thin film transistor (TFT) structure.[11]

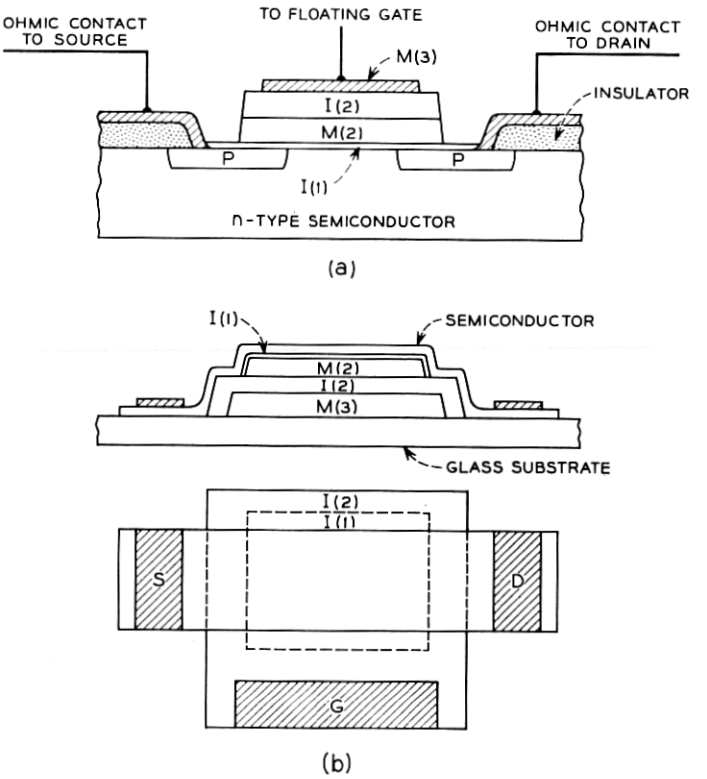
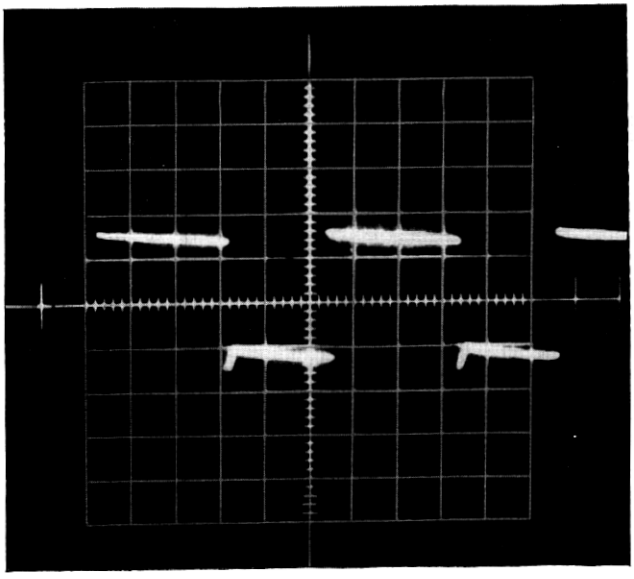
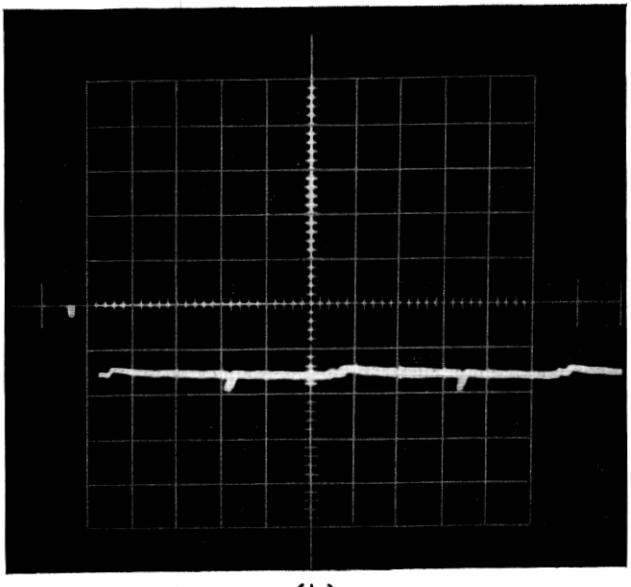


Fig. 3 — (a) Schematic diagram of a floating gate device using an IGFET. The numbers indicated correspond to those shown in Fig. 1. (b) Schematic diagram of a floating gate device using thin film transistor structure.

The IGFET-type floating gate devices have been tested in a pulsing circuit. Because of the relatively thick insulator layers, large voltages ($\approx$ 50 V) and long pulse width ($\approx$ 0.5 μs) have to be applied in order to store $\approx 5 \times 10^{12}$ charges/cm^2. Fig. 4 shows the experimental results. A positive pulse of 50 volts is first applied to the gate electrode, and 60 ms later a negative pulse of 50 volts is applied. Then the pulsing cycle repeats. In Fig. 4(a) the pulse widths are 0.5 μs. One notes that when the positive pulse is applied, a sufficient amount of charge is stored in the floating gate so that the silicon surface is inverted; a conducting channel is thus formed, and the channel current is "on." It can be seen that the channel current decreases only slightly at the end of 60 ms. When the negative pulse is applied, the stored charge is eliminated, and also the channel. The channel current reduces to its



(a)



(b)

Fig. 4 — Experimental results of the channel current of a IGFET-type floating gate device. A positive voltage pulse, V_1, with pulse width W_1, is first applied to the gate, and 60 ms later a negative pulse V_2 with pulse width W_2 is applied. Then the pulsing cycle repeats. Horizontal scale: 20 ms/div. Vertical scale: 0.1 ma/div. (a) $V_1 = V_2 = 50$ volts, $W_1 = W_2 = 0.5$ μs. (b) $V_1 = V_2 = 40$ volts, $W_1 = W_2 = 0.5$ μs.

"off" state. Fig. 4(b) shows results for pulses with the same widths but smaller amplitude (40 V). Since the stored charge is a strong function of the pulse amplitude, only a very small amount of charge is stored, too small to cause inversion. For non-leaky units, the memory holding time of longer than one hour has been observed.

It is clear that a modified IGFET such as a TFT can be used for read-out, as shown in Fig. 3(b). For an academic study of device operation, the floating gate can be partially exposed and a potential probe can be placed nearby.

In conclusion, it has been demonstrated that the controlled field emission to the buried "floating" gate may be capacitively induced by pulsing the outer gate electrode. This combination can therefore, be used as a memory device, with holding time as long as the dielectric relaxation time of the gate structure and with continuous nondestructive read-out capability. There seems to be no inherent reason why read-in read-out cannot be performed in a very short time, say in the nanosecond range or even shorter.

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REFERENCES

1. Shockley, W., and Pearson, G. L., Phys. Rev., *74*, 1948, p. 232.
2. Ross, I. M., U. S. Patent 2,791,760, issued May 7, 1957.
3. Jona, F. and Shirane, G., *Ferroelectric Crystals*, MacMillan Co., 1962.
4. Heyman, P. M. and Heilmeier, G. H., Proc. IEEE, *54*, 1966, p. 842.
5. Mead, C. A., Proc. IRE, *48*, 1960, p. 359.
6. Simmons, J. G., J. Appl. Phys., *34*, 1963, p. 1793.
7. Sze, S. M., Current Transport and Maximum Dielectric Strength of Silicon Nitride Films, J. Appl. Phys., June, 1967.
8. Williams, R., Phys. Rev., *140*, 1965, A569.
9. Kahng, D., Semipermanent Memory Using Capacitor Charge Storage and IGFET Read-out, B.S.T.J., this issue, pp. 1296–1300.
10. Kahng, D. and Atalla, M. M., Silicon-Silicon Dioxide Field Induced Surface Devices, presented at the IRE-AIEE Device Res. Conf., Carnegie Inst. Tech., Pittsburgh. Pa., June 1960.
11. Weimer, P. K., An Evaporated Thin Film Triode, presented at the IRE-AIEE Device Res. Conf., Stanford University, Stanford, Calif., June 1961.

Semipermanent Memory Using Capacitor Charge Storage and IGFET Read-out

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One of the earliest computers used capacitors as its memory.[1] A mechanical means was used for both read-in and read-out operations. Electronic accessing was used in conjunction with vacuum tube or solid-state diodes in relatively modern computers such as the SEAC computer.[2] Capacitor storage is rarely used at present since magnetic memories meet the modern computer requirements much better. The inherent difficulty with capacitor storage was the limited holding time since a nonlinear resistor with small enough leakage currents to allow useful memory holding time was then not readily available. The old capacitor memory was charged through a diode with slow recovery time and with leakage current of 10^{-10} amp at best and required a large capacitor for any appreciable holding time. Furthermore, the read-out was usually destructive.

The capacitor storage merits re-examination in view of the advanced solid-state devices and technology now available. Coupled with an Insulated Gate Field Effect Transistor (IGFET),[3] the read-out can be nondestructive. Integrated circuit techniques may prove superior to the current magnetic memories for some applications where infrequent recycling is permissible. The inherent speed should be much faster than that of magnetic units.

Consider a capacitor C in series with a nonlinear element as shown in Fig. 1. The capacitor may represent the gate capacity of the IGFET plus any external capacitor in parallel with the gate capacitor. When a positive voltage pulse with amplitude V and duration τ is applied at the nonlinear element terminal, it can be shown that the stored charge $Q(\tau)$ and the decay time constant τ_e, defined as the time required to reach $1/e$ value of the initial stored charge Q_o, can be calculated for various nonlinear resistors.

I. POWER-LAW RESISTORS

The I-V characteristics are given by

$$I = KV_n^m, \tag{1}$$

then

$$Q(\tau) = C\left[V - \left(\frac{1}{V^{(m-1)}} + K(m-1)\frac{\tau}{C}\right)^{-1/(m-1)}\right] \tag{2}$$

and

$$\begin{aligned} \tau_e &= \frac{C^m}{(m-1)K}\frac{1}{Q_0^{(m-1)}}(e^{(m-1)} - 1) \\ &= \frac{(e^{(m-1)} - 1)}{(m-1)}\frac{Q_0}{I_0}, \end{aligned} \tag{3}$$

where I_0 is the discharge current at the termination of charging. It is clear from (2) that m $\geqq$ 1 for physically meaningful $Q(\tau)$. For a long holding time, (3) tells us that the nonlinearity of the resistor should be large. These equations would describe the behavior of the storage unit comprising a space-charge-limited-current diode.[4] If traps are present, only a simple modification is needed in the analysis. Structures comprising photosensitive space-charge-limited-current diodes such as CdS diodes should allow optical read-in operations which might be advantageous for certain applications such as a vidicon.

II. TUNNEL SANDWICH DIODES

For this nonlinear element, the circuit in Fig. 1 should be modified to include the shunt capacitance of the tunnel sandwich. Thus, at the instance of pulse application, the voltage divides between the two capacitors. The I-V relationship for Fowler-Nordheim type tunneling is

$$I = KV_n^2 e^{-V_0/V_n}. \tag{4}$$

With the appropriate initial conditions, the stored charge $Q(\tau)$ is given by

$$Q(\tau) = C\left[V - \alpha V_0/\ln\left(e^{\alpha V_0/V} + \frac{KV_0}{C}\tau\right)\right], \tag{5}$$

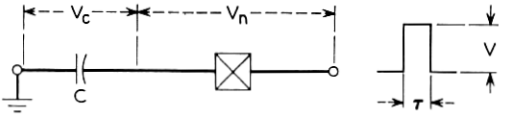

Fig. 1 — A capacitor being charged through a nonlinear resistor.

where α is defined as unity plus the ratio of the shunt capacitance of the tunnel sandwich, C_n to the charging capacitor, namely $\alpha = 1 + (C_n/C)$.

The discharge time constant τ_e can also be shown to be

$$\tau_e = \frac{\frac{\alpha C}{KV_0}\left(e^{(\alpha CV_0/Q_0)(e-1)} - 1\right)}{e^{\alpha CV_0/Q_0}} = \tau_c e^{(\alpha CV_0/Q_0)(e-2)}. \tag{6}$$

It is clear that charging time required for adequately large Q is very short, allowing fast read-in operation. The decay time can be seen to be large for tunneling across well-known insulators such as SiO_2 and Al_2O_3. Therefore, the decay is not controlled by (6) but rather by the dielectric relaxation time of the insulators used for the entire assembly including the IGFET gate material. The dielectric relaxation time of the best inorganic insulators is of the order of one day at room temperatures. However, certain organic insulators are known to have theoretical dielectric relaxation times of many years. Performance of a memory cell incorporating a tunnel sandwich diode is described in more detail elsewhere.[5]

III. SCHOTTKY BARRIER DIODES

For charging through a rectifier, Schottky barrier diodes are preferred over pn junction diodes since Schottky barriers are majority carrier devices and hence fast recovery is achievable.[6] I-V characteristics may be represented by

$$I = I_s(e^{\beta V} - 1). \tag{7}$$

For charging, we may neglect the unity in the bracket in (7), and the stored charge can be shown to be

$$Q(\tau) = C\left[V - \frac{1}{\beta}\ln\left(\frac{\tau}{\tau_c} + e^{-\beta V}\right)^{-1}\right], \tag{8}$$

where

$$\tau_c = \frac{C}{\beta I_s}.$$

For decay, it is easy to show

$$\tau_e = \frac{Q_0}{I_s}(1 - e^{-1}). \tag{9}$$

Fig. 2 shows the stored charge Q computed from (8) as a function of pulse duration for several pulse amplitudes. The characteristic time constant τ_c is not much less than 1 sec for a typical configuration ($C < 10^{10}$ Fd, $I_s > 10^{-12}$ amp). Therefore, it is seen that the stored charge is proportional to the pulse amplitude for sufficiently large V. This suggests that the device may be used as a multi-level storage unit.

The combination of Schottky barrier diodes and the IGFET is shown in Fig. 3. A similar structure has been fabricated and tested. The holding time was of the order of 10 sec when the charging was done by 15 volts pulse in agreement with (9) since the IGFET gate capacitance was about 10^{-12} Fd and I_s of the diode was 10^{-12} amp (measured at 10 volts reverse bias). The maximum pulse amplitude before the breakdown of the gate insulator was about 30 volts, allowing a longer holding time of about 30 seconds. The read-in time was less than 10^{-7} second and the reverse breakdown of the diode was used to turn the IGFET off, which also took less than 10^{-7} second.

A memory featuring nondestructive read-out, access times in the

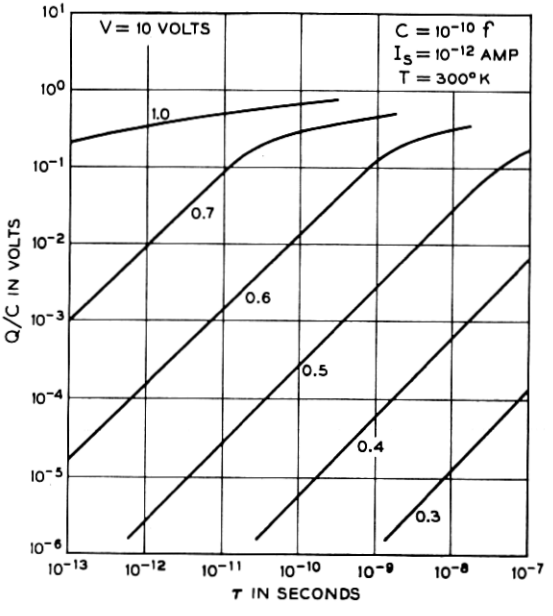

Fig. 2 — Theoretical stored charge/storing capacitance (the floating potential) as a function of time for charging through a Schottky barrier diode.

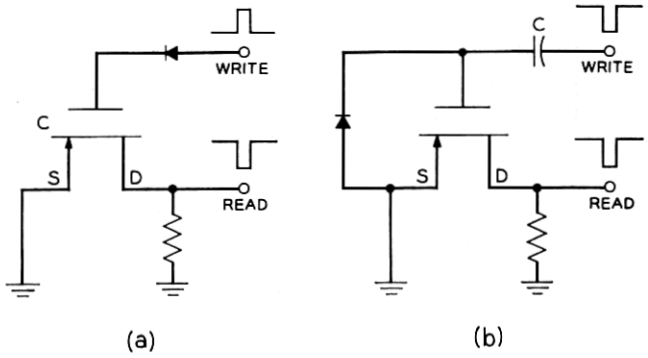

Fig. 3 — Combination of the capacitor storage unit with a p-channel IGFET for read-out. (a) Series connection, read-in should be positive. (b) Parallel connection, read-in should be negative.

submicrosecond range, and holding times of many seconds should find many applications. An integrated structure incorporating Schottky barrier diodes and IGFETs is readily obtainable with modern solid-state technology.

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REFERENCES

1. Richards, R. K., *Electronic Digital Systems,* John Wiley & Sons, Inc., New York, 1966, credits J. V. Atanasoff and his associates for the first capacitor memory bank constructed 1938–1942.
2. Holt, A. W., *Computer Handbook,* edited by H. D. Huskey and G. A. Koran, The Maple Press Co., York, Pa., 1962, Diode-Capacitor Memory System, Sect. 12.9.
3. Kahng, D. and Atalla, M. M., Silicon-Silicon Dioxide Field Induced Surface Devices, presented at the IRE-AIEE Device Research Conference, Carnegie Institute of Technology, Pittsburgh, Pa., June, 1960.
4. Rose, A., Phys. Rev., *97,* 1955, p. 1538.
5. Kahng, D. and Sze, S. M., A Floating Gate and its Application to Memory Devices, B.S.T.J., this issue, pp. 1288–1295.
6. Kahng, D. and D'Asaro, L. A., Gold-Epitaxial Silicon High-Frequency Diodes, B.S.T.J., *43,* 1964, pp. 225–232.