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CHARGE ACCUMULATION AND MOBILITY IN THIN DIELECTRIC MOS TRANSISTORS

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Abstract—A study of the turn-on of very thin dielectric MOS devices from subthreshold to strong inversion is described. A functional form has been found for the derivative of channel charge with respect to gate voltage, the derivative of channel charge with respect to distance along the channel, and the electric field along the channel in this transition region. A method to extract electron mobility versus gate voltage independent of any arbitrarily defined threshold voltage has been shown. Measured data on the electron mobility vs gate voltage for 100Å gate dielectric MOS devices are reported.

NOTATION

C_{ox}	gate dielectric capacitance
Q_N	channel charge
Q_B	bulk charge
Q_s	total semiconductor charge
Ψ_s	surface potential
ϕ_F	Fermi potential
V_G	gate-to-source voltage
V_{FB}	flat band voltage
V_D	drain-to-source voltage
$V_{T2\phi F}$	classical threshold voltage
V_{TEXT}	extrapolated threshold voltage
E_X	electric field along channel
W	width of device gate
L	length of device gate
μ	mobility of electrons
I_D	drain current
$\frac{KT}{q}$	thermal voltage

INTRODUCTION

In order to scale MOS devices down to gate lengths in the submicron range, the gate capacitance must be increased to retain long-channel device characteristics[1]. It has been shown that as the insulator thickness decreases, the mobile channel charge does not vary linearly with gate voltage, as had been conventionally assumed[2, 3]. This is due to the fact that the channel capacitance is comparable in value to the dielectric capacitance until $V_G \gg V_{T2\phi F}$. We have found, using two dimensional simulation[4], that in order to validate the assumption that the electric field along the channel is equal to V_D/L for very low drain voltage, the gate voltage must be approx. 0.5 V above threshold. We have also studied the dependence of the diffusion current term, (dQ_N/dx), on gate voltage in the weak inversion region. In this region, again for very low drain voltage, the diffusion current term changes from being exponentially dependent on V_G to becoming a constant independent of V_G. The width of this transition region is approx. 0.5 V. Because a significant portion of the region of operation of properly scaled MOS devices will be at voltages near threshold, these effects must be considered and understood in the evaluation and modeling of device performance. We have found that these effects can strongly influence the experimental extraction of the effective mobility of electrons in the channel.

Two objectives are addressed by this work. The first is to develop an understanding of the transition region from subthreshold to strong inversion with very low drain bias in thin dielectric MOS devices. In particular, the physical quantities studied are the mobile channel charge, Q_N, the derivative of mobile charge with respect to gate voltage, dQ_N/dV_G, the derivative of mobile charge with respect to distance along the channel, dQ_N/dx, and the electric field along the channel, Ex. The second objective is to demonstrate a technique to measure the mobility of channel electrons independent of any arbitrarily defined threshold voltage. This can be accomplished with proper understanding of the transition region.

In the first section of this paper, we discuss the results of two-dimensional simulation of the transition region. In the second section we show how channel electron mobility can be extracted from measurable quantities. The third and fourth sections provide a basis for the theory of the measurement and the experimental set-up used to carry out the measurement, respectively. Finally, in the discussion section, the assumptions used in the measurement technique and their effect on the reported results are pointed out. We also show a comparison to a commonly used mobility measurement technique.

1. 2-D SIMULATION STUDY OF TRANSITION REGION

We start with the equation for drain current in an MOS device to be

$$\frac{I_D}{W} = Q_N \mu E_x - \frac{KT}{q} \mu \frac{dQ_N}{dx}. \tag{1}$$

From this equation it is clear that to determine the mobility as a function of gate voltage, we must be able to accurately determine I_D, Q_N, dQ_N/dx and Ex. We have

used two dimensional computer simulation to examine each of these quantities in the gate bias range from subthreshold to strong inversion with very low drain voltage. This simulation is based on a two dimensional solution of the current transport equation coupled with Poisson's equation. The lateral device dimensions are sufficiently large to eliminate any geometry effects.

Figure 1 shows the mobile charge calculated from the integrated channel capacitance compared to the mobile charge calculated using the conventional assumption that the mobile charge is linear with gate voltage above threshold with a slope of *Cox*. In this case threshold is defined as the gate voltage necessary to make $\Psi_s = 2\phi_F$. The non-linearity in the mobile charge adds a significant error in the expected channel charge in the device as a function of gate voltage. This nonlinearity comes from the fact that the derivative of the mobile charge with respect to gate voltage, dQ_N/dV_G, does not equal Cox immediately at threshold. An increase in V_G on the order of 0.5 V above threshold is necessary for dQ_N/dV_G to be about 90% of its maximum value *Cox*. The transition of dQ_N/dV_G from zero to *Cox* is plotted on a normalized scale in Fig. 2.

The electric field along the channel also goes through a transition region. The gate voltage must be much greater than threshold before the electric field reaches its maximum value of V_D/L. Figure 3 shows a plot of the normalized electric field along the channel vs gate voltage, and again we see that the gate voltage must be 0.5 V above threshold for the electric field to be 90% of its maximum value. This result is valid at any point along the channel assuming that the electric field is constant. With a drain voltage less than KT/q, the assumption of a constant electric field along the channel is valid for all gate voltages. This is illustrated in Fig. 4 where a plot of the electric field along the channel with a drain voltage of 10 mV, and the gate voltage as a parameter, is presented.

Referring to Appendix 2 we have shown the conditions under which the derivative of the mobile charge with respect to distance along the channel, dQ_N/dx, increases asymtotically to a value of $Cox * V_D/L$ when the gate voltage is much greater than threshold with a drain bias of of 10 mV. Figure 5 shows the results of simulation for dQ_N/dx vs gate voltage. Again we see that the gate voltage must be 0.5 V above threshold in order for this quantity to be 90% of its maximum value.

In this section, we have used 2D simulation to show that the transitions from zero to the respective maximum

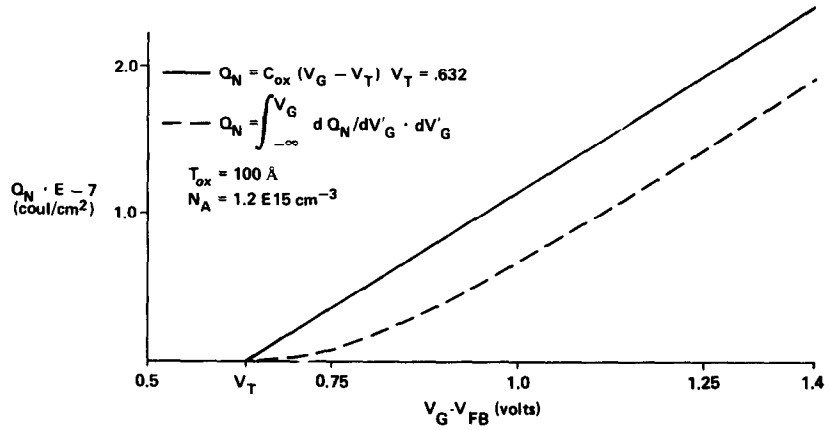

Fig. 1. Calculated channel charge vs gate voltage using (a) conventional assumptions (solid line) and (b) exact 2D model (dotted line).

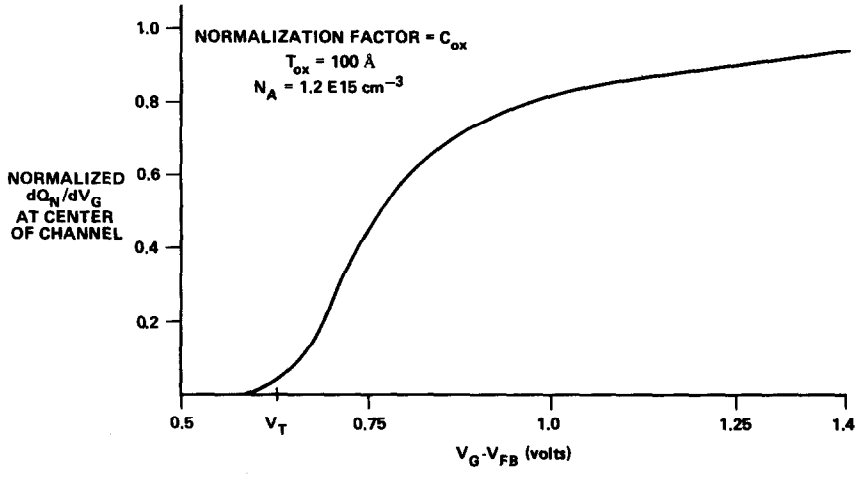

Fig. 2. Calculated derivative of channel charge with respect to gate voltage vs gate voltage.

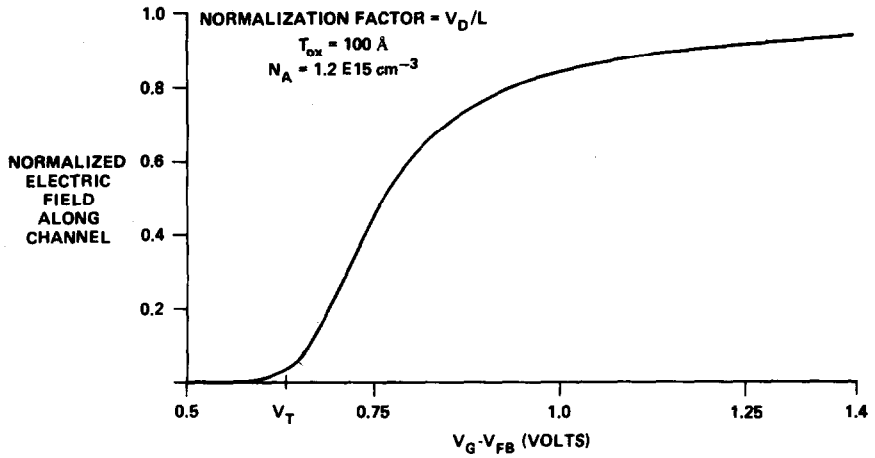

Fig. 3. Calculated electric field along channel vs gate voltage.

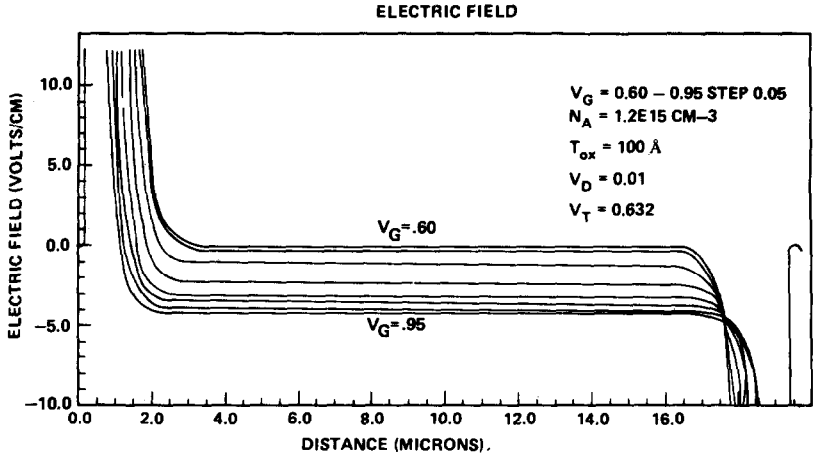

Fig. 4. Calculated electric field along channel vs position along channel. The electric field is constant at any given gate voltage due to the low drain voltage of 10 mV.

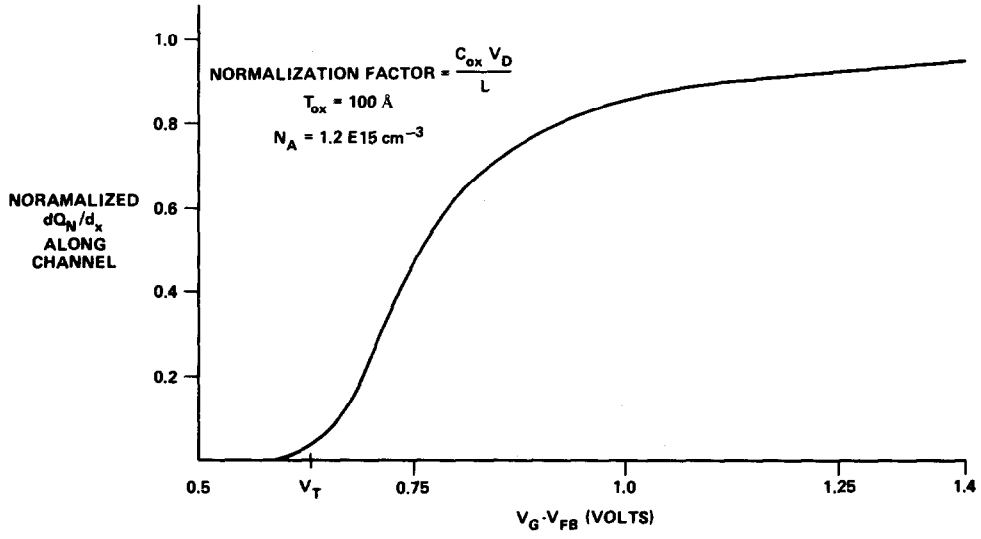

Fig. 5. Calculated derivative of channel charge with respect to distance along the channel vs gate voltage.

values of dQ_N/dV_G, dQ_N/dx, and Ex, follow the same functional dependence on gate voltage. This can be easily observed by comparing Figs. 2, 3 and 5. For a given doping concentration and gate dielectric thickness, these quantities track each other to within 10%. Although not presented here, we have observed this for doping concentrations ranging from 1E15 to 1E17 cm^{-3} and gate dielectric thickness ranging 100–1000 Å. Two other points have been observed from these simulation results. First, the width of the transition region is on the order of 0.5 V over the range of parameters studied. Second, the classical threshold voltage of $\Psi_s = 2\phi_F$ is located near the beginning of the transition region. The three significant quantities discussed are less than 5% of their maximum value at a gate voltage corresponding to the classical threshold.

2. EXTRACTION OF MOBILITY FROM MEASURED QUANTITIES

Using the results of our discussion in Section 1, mobility can be extracted vs gate voltage independent of any arbitrarily defined threshold if we measure the derivative of mobile charge with respect to gate voltage, dQ_N/dV_G, and the drain current, I_D, as a function of gate voltage with a very low drain bias of 10 mV. Since $V_D < KT/q$, the variations along the channel of Q_N, dQ_N/dx and Ex are small compared to their respective magnitudes. Therefore, we assumed that these quantities are nearly constant along the channel. This assumption has been verified by two dimensional simulation.

We start with the result derived in the appendix

$$\frac{dQ_N}{dV_G} = \frac{Cox\, dQ_N/d\psi_s}{Cox + dQ_s/d\psi_s} \tag{2}$$

and let

$$F(V_G) = \frac{dQ_N/d\psi_s}{Cox + dQ_s/d\psi_s}. \tag{3}$$

The function F is zero when the channel capacitance, $dQ_N/d\Psi_s$, is zero and increases to a maximum value of 1.0 when the channel capacitance plus the bulk capacitance, $dQ_s/d\Psi_s$, is much greater than Cox. We have shown in Section 1 that dQ_N/dx, and the electric field along the channel go from zero to their respective maximum values following the function F. From the measurement of dQ_N/dV_G the function F can be found. Thus, the electric field along the channel and the derivative of mobile charge with respect to distance along the channel as a function of gate voltage are known.

$$E(V_G) = \frac{V_D}{L} F(V_G) \tag{4}$$

$$\frac{dQ_N}{dx}(V_G) = \frac{Cox\, V_D}{L} F(V_G). \tag{5}$$

It should be noted that both eqns 4 and 5 are independent of position along the channel since $V_D < KT/q$. Additionally, the measurement of dQ_N/dV_G yields the total mobile charge in the channel as a function of gate voltage by:

$$Q_N(V_G) = \int_{-\infty}^{V_G} [dQ_N/dV_G'] \, dV_G'. \tag{6}$$

Therefore, referring to eqn (1), all of the factors needed to determine mobility at any gate voltage can be obtained by a measurement of dQ_N/dV_G and I_D, vs gate voltage at a low (10 mV) drain bias.

3. THEORY OF MEASUREMENT

A "split" C-V measurement[5] scheme was used to obtain the change in mobile charge with respect to gate voltage, dQ_N/dV_G, and the change in bulk charge with respect to gate voltage, dQ_B/dV_G. Shown in Fig. 6 is a schematic representation of the measurement, an equivalent circuit model and a representation of the measured results. The current I_1 is the displacement current flowing out of the source and drain and I_2 is the displacement current flowing out of the substrate when a ramp voltage is applied to the gate.

To show that I_1 and I_2 are proportional to the change in mobile and bulk charge respectively, we start with

$$I_1 = \frac{dQ_N}{d\psi_s}\frac{d\psi_s}{dt} \tag{7}$$

and

$$\psi_s = V_G - \frac{Q_s}{C_{ox}} - V_{FB} \tag{8}$$

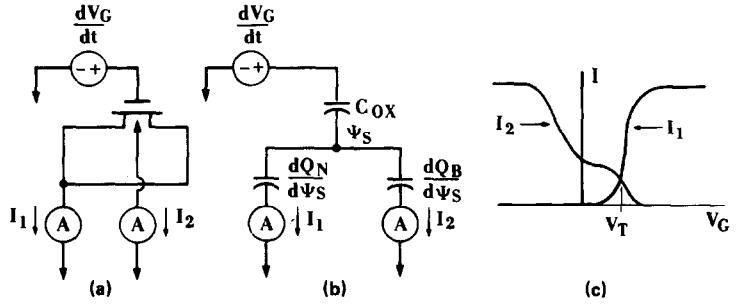

Fig. 6. Description of "split C-V" measurement: (a) schematic representation; (b) equivalent circuit model and (c) qualitative experimental result.

Differentiating (8) and applying the chain rule results in

$$\frac{d\psi_s}{dt} = \frac{dV_G}{dt} - \frac{dQ_s}{dV_G}\frac{dV_G}{dt}\frac{1}{C_{ox}}. \quad (9)$$

Substituting (9) into (7) yields

$$I_1 = \frac{dV_G}{dt}\left[\frac{dQ_N}{d\psi_s} - \frac{dQ_N}{d\psi_s}\frac{dQ_s}{dV_G}\frac{1}{C_{ox}}\right]. \quad (10)$$

Substituting the expression for (dQ_s/dV_G) derived in the appendix into (10) and rearranging gives

$$I_1 = \frac{dV_G}{dt}\frac{\frac{dQ_N}{d\psi_s}\left(C_{ox}+\frac{dQ_W}{d\psi_s}+\frac{dQ_B}{d\psi_s}\right) - \frac{dQ_N}{d\psi_s}\left(\frac{dQ_N}{d\psi_s}+\frac{dQ_B}{d\psi_s}\right)}{C_{ox}+\frac{dQ_N}{d\psi_s}+\frac{dQ_B}{d\psi_s}}. \quad (11)$$

Therefore,

$$I_1 = \frac{dV_G}{dt}\left[\frac{C_{ox}\frac{dQ_N}{d\psi_s}}{C_{ox}+\frac{dQ_N}{d\psi_s}+\frac{dQ_B}{d\psi_s}}\right] \quad (12)$$

and substituting the expression for (dQ_N/dV_G) derived in the appendix:

$$I_1 = \frac{dV_G}{dt}\frac{dQ_N}{dV_G}. \quad (13)$$

In a similar manner

$$I_2 = \frac{dV_G}{dt}\left[\frac{C_{ox}\frac{dQ_B}{d\psi_s}}{C_{ox}+\frac{dQ_N}{d\psi_s}+\frac{dQ_B}{d\psi_s}}\right] = \frac{dV_G}{dt}\frac{dQ_B}{dV_G}. \quad (14)$$

4. EXPERIMENTAL SETUP AND DEVICE FABRICATION

A semi-automated test system using an HP9845 desktop calculator controlling an HP4140B picoammeter with a built in ramping voltage source was used to measure the devices. A ramp voltage of 0.1 V/sec was selected. This rate has proven to be slow enough to ignore the resistance of the channel and yet fast enough to generate enough current for an accurate measurement. The capacitances measured were on the order of 30 pF, giving currents of 3pA with the ramp rate used. A carefully designed, low noise, shielded test setup capable of achieving better than 0.1pA resolution was necessary to obtain meaningful results.

Very thin (100 Å) oxide, n-channel transistors were fabricated on p-type ⟨100⟩ silicon substrates. Effective channel doping concentrations of 4E16, 8E16, and 2E17 cm^{-3} were used to observe their effect on the electron mobility. The gate oxide was grown in a 0.63% TCE and oxygen ambient at 850°C for 30 min, followed by a nitrogen anneal. Transitors were fabricated using a standard four mask polysilicon gate technology with local oxidation to provide isolation between devices. The transistors measured had a gate width and length of 100 microns to eliminate geometrical effects.

5. RESULTS AND DISCUSSION

A typical split C–V measurement curve for a 100 Å oxide device is shown in Fig. 7. On the same device the drain current vs gate voltage with a drain bias of 10 mV is measured. The split C–V measurements are integrated as outlined in Section 2 to yield a graph of mobile charge in the channel as a function of gate voltage. Figure 8 shows the mobile charge, Q_N as a function of gate voltage for the various bulk doping concentrations. The channel electron mobility was extracted from the data as outlined in Section 2. A plot of mobility vs gate drive, $V_G - V_{T2\phi F}$, for the devices measured is shown in Fig. 9. The threshold voltage used in calculating the gate drive was the classical $\Psi_s = 2\phi_F$ point which corresponds to the gate voltage at which [6]

$$\frac{dQ_N}{dV_G} = \frac{dQ_B}{dV_G}. \quad (15)$$

Note that this threshold voltage was used to normalize the gate drive among the devices compared, and is not used in the calculation of mobility.

Qualitatively, the dependence on gate voltage of all the devices is the same. Near threshold the mobility of all devices measured decreases. This is an artifact of the measurement assumption and will be explained later. As the gate voltage is increased the mobility rises to a peak and begins to fall. This degradation is due to the increased surface field supplied by the gate voltage. The lightly doped channel regions have a higher peak mobility than the more heavily doped devices. This reduction with increased channel doping concentration has been observed and reported by several authors [7, 8]. It has been explained by showing that devices with a lower doping concentration have a lower surface field and therefore lower surface scattering.

The measurement of mobility using the charge accumulation technique described in this paper has been compared to the more conventional technique which uses only a drain current measurement. The conventional technique assumes that the mobile charge is equal to Cox $(V_G - V_{TEXT})$ where V_{TEXT} is obtained by extrapolating the I_D vs V_G curve back to the gate-to-source voltage axis. Referring to Fig. 7 this extrapolated threshold is approx. 100 mV higher than the classical threshold of $\Psi_s = 2\phi_F$. This is true over all doping concentrations measured. Two other assumptions made by the conventional technique are that the electric field along the channel is equal to V_D/L and that diffusion current can

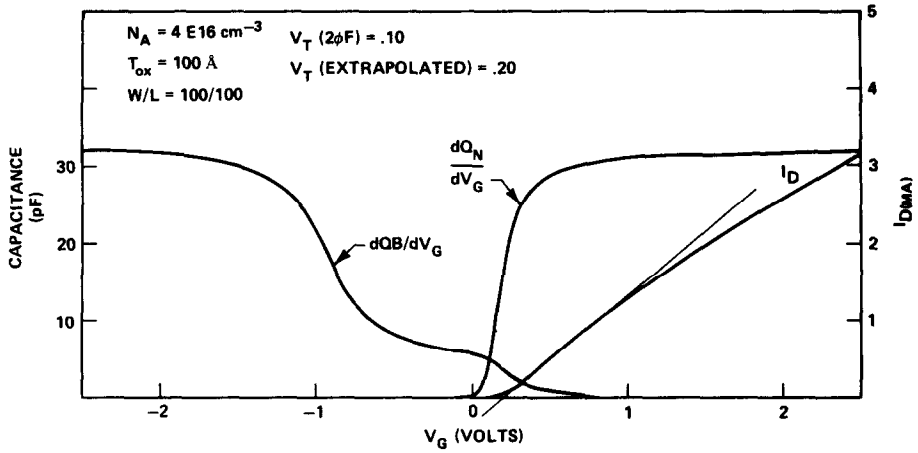

Fig. 7. Measured capacitance and drain current vs gate voltage for 100 Å oxide device.

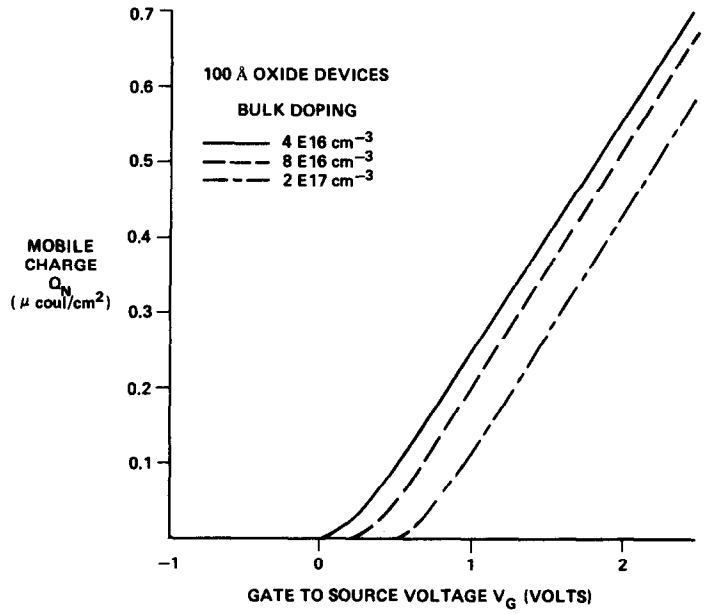

Fig. 8. Measured mobile charge vs gate voltage derived from eqn (6) for 100 Å oxide devices.

be ignored for any gate voltage above the extrapolated threshold. Since the extrapolated threshold is 100 mV above the classical threshold point, part of the transition region is not addressed by the conventional technique. The end result shown in Fig. 10 is that the mobility measured by the conventional technique is about 10% lower at 0.5 V above the classical threshold. Even with all the assumptions in the conventional technique the difference is small because they have a cancelling effect. The calculation of mobile charge and electric field tend to lower the extracted mobility; while ignoring the diffusion current component and the use of the extrapolated threshold tend to raise it. Since all four assumptions become valid as $V_G \gg V_{TEXT}$, the extracted mobility of both techniques tend to approach each other. Although the final result is not dramatic from a device modeling point of view, we feel that a greater understanding of the turn on region of MOS devices has been provided.

Our technique has one built-in assumption in that the fast surface state density is not taken into account. Figure 11 qualtitatively explains the effects of surface states on the extracted mobility. First, the presence of surface states tends to increase the measured dQ_N/dV_G at any given gate voltage. This translates to an increase in the F function which results in a lower extracted mobility. Second, the integrated mobile charge will include the charge trapped in fast surface states. Because this charge is not moved along the channel by the electric field, it does not contribute to the measured drain cur-

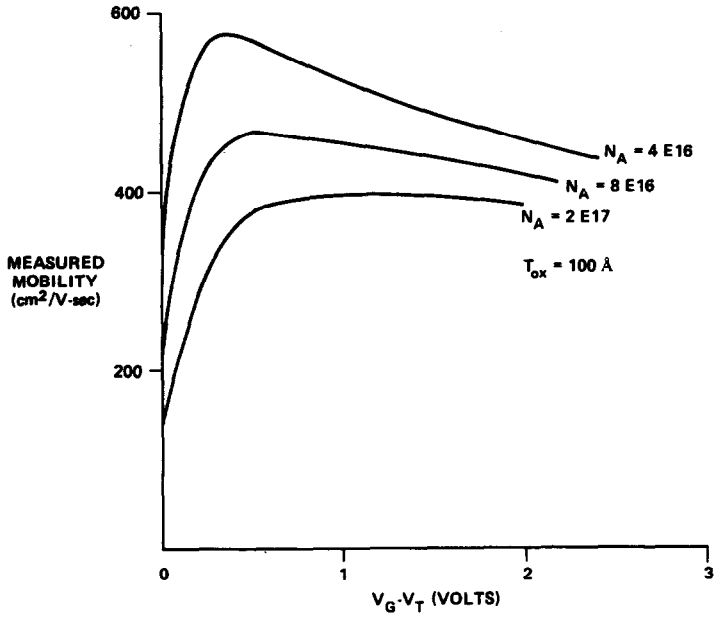

Fig. 9. Measured electron mobility vs gate drive for 100 Å oxide devices using method described in Section 2.

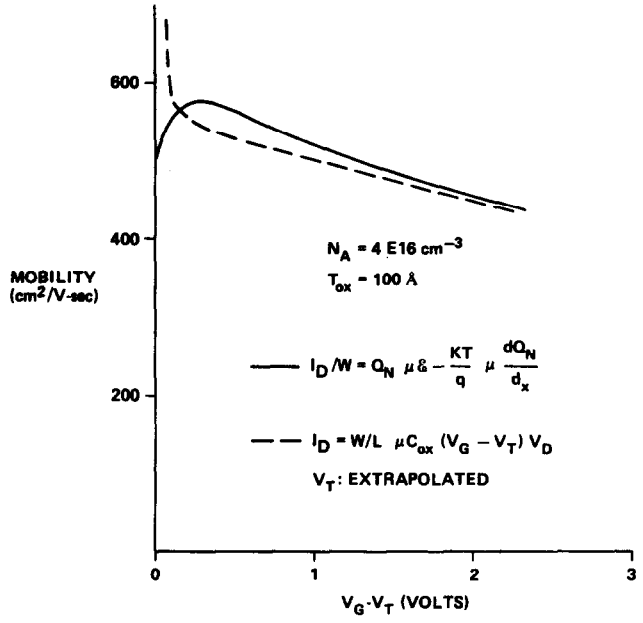

Fig. 10. Measured mobility for a 100 Å oxide device using different techniques: (a) the conventional technique and (b) charge accumulation technique (see text for explanations).

rent. Therefore, the extracted mobility is again lowered. Both of these effects are not important when the gate voltage is sufficiently high.

Typical values of interface state density vs surface potential[9] were used to determine the effect on electron mobility as the gate voltage approaches the classical threshold. For a channel doping of 4E16 cm^{-3} the mobility extracted at the classical threshold is 440 cm^{-2}/V sec when these typical values of interface state density are included. Raising the density by a factor of two yields a mobility at the classical threshold of 1000 cm^2/V sec. Thus, no conclusion can be made about what the channel electron mobility is from the classical threshold point to about 0.25 V above threshold unless the interface state density is carefully measured as a function of surface potential on the transistor which is being characterized.

EFFECT OF SURFACE STATES

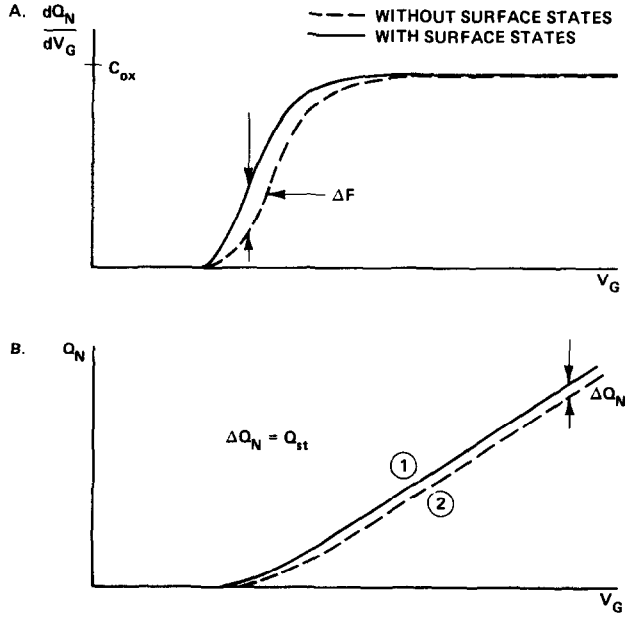

Fig. 11. Effect of surface states on (a) measurement of dQ_N/dV_G vs gate voltage and (b) determination of mobile charge vs gate voltage.

CONCLUSIONS

We have experimentally verified the non-linear dependence of channel charge on gate voltage near the classical threshold for very thin dielectric MOS devices by using the split C–V technique. This non-linear region is a significant portion of the device operating range and results in a lower transconductance than is predicted by classical scaling theory.

We have found a functional form for the transition of the derivative of mobile charge with respect to gate voltage from zero to its maximum value *Cox*. We have shown that this same functional form is obeyed by the electric field along the channel and the derivative of mobile charge with respect to distance along the channel. This transition region starts at the classical threshold voltage and has a width on the order of 0.5 V. It was also found that the extrapolated threshold from the drain current vs gate voltage curve is approximately 100 mV higher than the classical threshold definition.

Finally we have used this understanding of the turn-on of thin dielectric MOS devices to extract the mobility of channel electrons in 100 Å oxide devices independent of an arbitrarily defined threshold voltage.

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APPENDIX 1

In this section we derive expressions for the channel, bulk, and total semiconductor capacitance.

Starting with

$$\Psi_s = V_G - \frac{Q_s}{C_{ox}} \tag{A1. 1}$$

differentiating with respect to V_G and using the chain rule

$$\frac{d\psi}{dV_G} = 1 - \frac{dQ_s}{d\psi_s}\frac{d\psi_s}{dV_G}\frac{1}{C_{ox}} \tag{A1. 2}$$

rearranging

$$\frac{d\psi_s}{dV_G}\left(1 + \frac{dQ_s}{d\psi_s}\frac{1}{C_{ox}}\right) = 1 \tag{A1.3}$$

$$\frac{d\psi_s}{dV_G} = \frac{C_{ox}}{C_{ox} + \frac{dQ_s}{d\psi_s}}. \tag{A1. 4}$$

Now

$$Q_s = Q_N + Q_B \tag{A1. 5}$$

differentiating with respect to ψ_s we obtain

$$\frac{dQ_s}{d\psi_s} = \frac{dQ_N}{d\psi_s} + \frac{dQ_B}{d\psi_s}. \tag{A1. 6}$$

Substituting A.6 into A.4

$$\frac{d\psi_s}{dV_G} = \frac{C_{ox}}{C_{ox} + \frac{dQ_N}{d\psi_s} + \frac{dQ_B}{d\psi_s}} \tag{A1.7}$$

Therefore using A1.7

Channel capacitance

$$\frac{dQ_N}{dV_G} = \frac{dQ_N}{d\psi_s}\frac{d\psi_s}{dV_G} = \frac{\frac{dQ_N}{d\psi_s} C_{ox}}{C_{ox} + \frac{dQ_N}{d\psi_s} + \frac{dQ_B}{d\psi_s}} \tag{A1.8}$$

Bulk capacitance

$$\frac{dQ_B}{dV_G} = \frac{dQ_B}{d\psi_s}\frac{d\psi_s}{dV_G} = \frac{\frac{dQ_B}{d\psi_s} C_{ox}}{C_{ox} + \frac{dQ_N}{d\psi_s} + \frac{dQ_B}{d\psi_s}} \tag{A1.9}$$

Total semiconductor capacitance

$$\frac{dQ_s}{dV_G} = \frac{dQ_s}{d\psi_s}\frac{d\psi_s}{dV_G} = \frac{\frac{dQ_s}{d\psi_s} C_{ox}}{C_{ox} + \frac{dQ_N}{d\psi_s} + \frac{dQ_B}{d\psi_s}} \tag{A1.10}$$

APPENDIX 2

To prove that dQn/dx approaches $(Cox * V_D/L)$ for large gate drive, we start with:

$$V_G = \Psi_s + Qs/Cox \tag{A2.1}$$

$$\frac{dQ_s}{dx} = -Cox\, d\Psi s/dx \tag{A2.2}$$

now

$$Ex = -d\Psi_s/dx \tag{A2.3}$$

$$\therefore dQ_s/dx = dQ_B/dx + dQ_N/dx = Cox\, Ex. \tag{A2.4}$$

To show the conditions under which dQ_N/dx is large compared to dQ_B/dx:

$$Q_B \cong (2\epsilon_s q N_A \Psi_s)^{1/2} \tag{A2.5}$$

$$\frac{dQ_B}{dx} = \left(\frac{\epsilon_s q N_A}{2\Psi_s}\right)^{1/2}\frac{d\Psi_s}{dx} = \left(\frac{\epsilon_s q N_A}{2\Psi_s}\right)^{1/2} Ex \tag{A2.6}$$

$\therefore$ From (A2.4) and (A2.6) if

$$Cox \gg \left(\frac{\epsilon_s q N_A}{2\Psi_s}\right)^{1/2} \quad \text{then} \quad \frac{dQ_N}{dx} \gg \frac{dQ_B}{dx} \tag{A2.7}$$

Under this condition and assuming large gate drive such that $Ex \approx V_D/L$

$$\frac{dQ_N}{dx} \cong \frac{Cox\, V_D}{L} \tag{A2.8}$$