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Integration of a silicon nanowire array into a photovoltaic device

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ABSTRACT

Silicon nanowire arrays grown by chemical vapour deposition were successfully integrated into functional photovoltaic devices. A crucial planarization step, achieved by embedding the nanowires in a spin-on glass matrix and subsequent polishing of the front surface, allowed to deposit a continuous and uniform conductive film on top of the nanowire array, and thus to form a high-quality front electrical contact. The silicon nanowire array solar cells fabricated using this process exhibited a parasitic series resistance as low as 5 Ω.cm², which is a clear improvement compared to the recent literature.

INTRODUCTION

Using nanostructures is a promising route for third-generation photovoltaics [1]. In particular, silicon nanowires (SiNWs) grown by chemical vapour deposition (CVD) have been considered as building blocks for radial junction solar cells [2], which could enable energy conversion efficiencies comparable with conventional wafer-based solar cells, while reducing processing costs. Furthermore, quantum confinement effects in SiNWs could be employed for fabricating all-silicon multi-junction solar cells, with efficiencies exceeding the Shockley-Queisser limit for single-junction cells [3].

Promising results have been reported for SiNW array solar cells by Tsakalakos *et al.* [4,5] and Stelzner *et al.* [6]. However, the energy conversion efficiency obtained so far is about 0.1% [4-6], which is low compared to the typical performances of conventional wafer-based devices. One of the possible causes for such modest performances is the presence of a very high parasitic series resistance.

Here, we propose an approach for integrating CVD-grown SiNW arrays into solar cells with low parasitic series resistance.

EXPERIMENT

The process used in this work for integrating SiNW arrays into solar cells is presented in figures 1 and 2. We focus on a simple device structure, consisting of *n*-type SiNWs grown on a *p*-type silicon substrate. The *n*-type SiNWs were prepared by CVD via the gold-catalysed

vapour-liquid-solid method [7, 8], on (100)-oriented silicon substrates of *p*-type conductivity (14-22 Ω.cm). Silane (SiH_4) and phosphine (PH_3) were used as the silicon precursor and the phosphorous *n*-type dopant precursor, respectively. The PH_3/ SiH_4 ratio was 2×10^{-3}, corresponding to a nominal phosphorous concentration of 1×10^{20} cm^{-3}. Electrical resistance measurements of individual SiNWs, performed by scanning spreading resistance microscopy, were consistent with this nominal doping density.

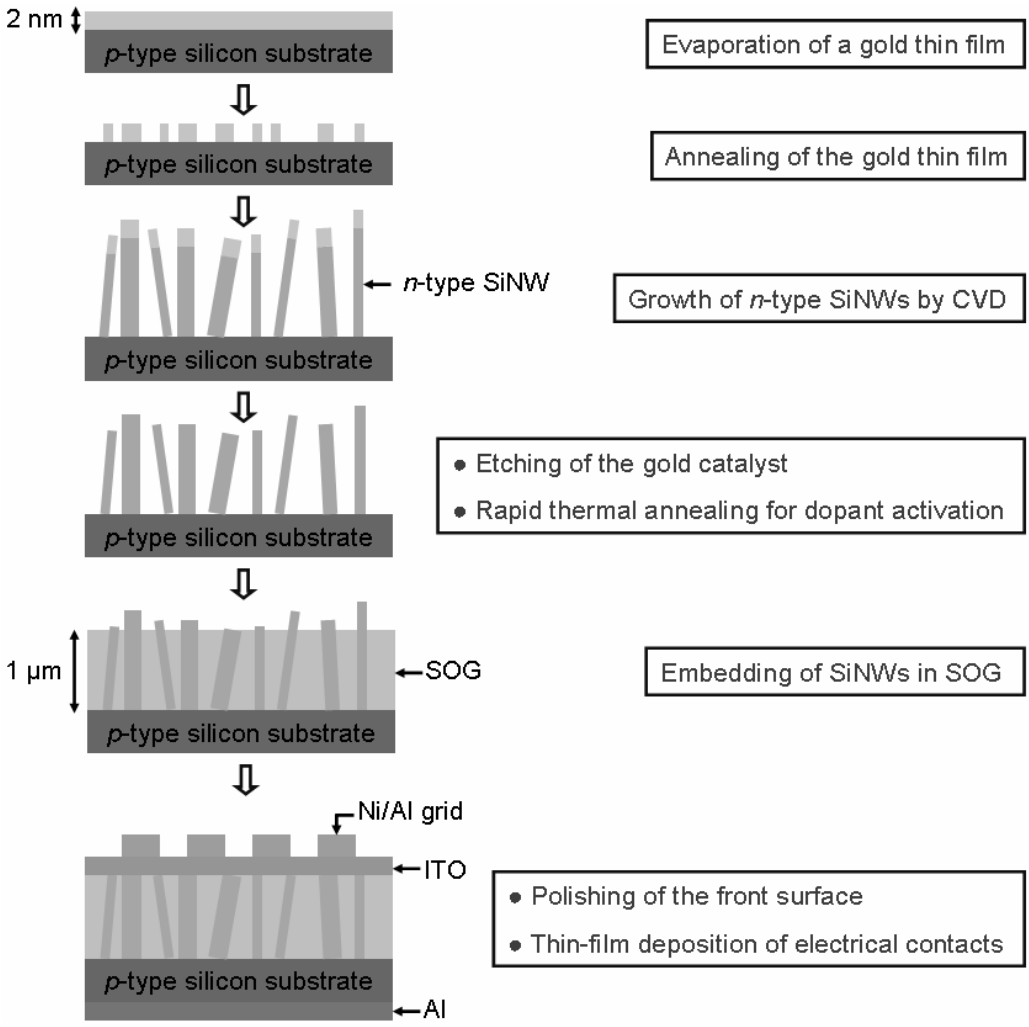

Figure 1. Schematic presentation of the process for integrating SiNW arrays into photovoltaic devices.

After the CVD growth of SiNWs, the gold catalyst was etched in a KI/I_2 solution, and the doping impurities were activated by rapid thermal annealing at 750°C for 5 min. The SiNWs were then embedded in a methylsiloxane SOG matrix, and the front surface was polished. An aluminium back electrical contact was deposited by sputtering, and annealed at 400°C in forming gas (4% of H_2 diluted in N_2). An indium-tin oxide (ITO) front electrical contact was then deposited by sputtering on the planarized SOG surface. As shown in figure 2, this ITO layer is uniform and continuous. Finally, a Ni/Al front contact grid was deposited on top of the ITO electrode, by electron-beam evaporation through a mask.

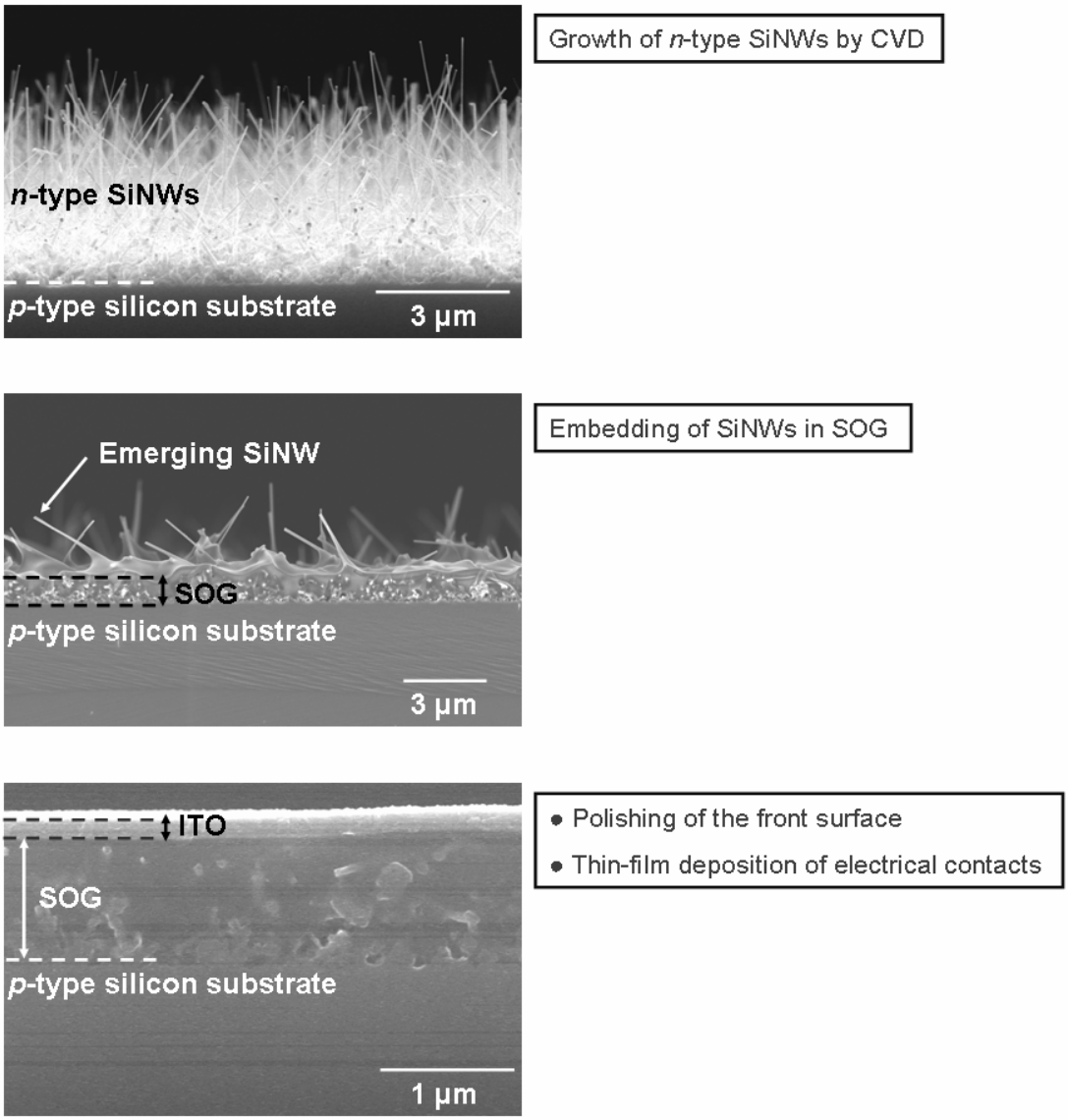

Figure 2. Cross-section scanning electron microscopy images of a SiNW array at various steps of the process presented in figure 1.

The fabricated SiNW array solar cells were mounted using silver paint onto a copper-coated board. Devices were illuminated by halogen lamps, and current-voltage characteristics were recorded by using Kelvin probes. During measurements, device temperature was regulated at 25°C. The halogen lamp spectrum used for our experiments is slightly different from the standard AM1.5G spectrum. However, it was experimentally checked that for our SiNW array solar cells illuminated at 100 mW/cm², the relative difference in energy conversion efficiency between the halogen lamp spectrum and the AM1.5G spectrum is less than 10%.

RESULTS AND DISCUSSION

Figure 3 shows the dark and light current-voltage characteristics of a SiNW array solar cell, fabricated following the process presented in figure 1. The device active area is of the order of 1 cm². A clear rectifying effect is observed in the dark, with power generation under illumination. For an illumination intensity of 100 mW/cm², the short-circuit current is 17 mA/cm^2, the open-circuit voltage is 250 mV, the fill factor is 44%, leading to an energy conversion efficiency of 1.9%. The solar cell behaviour is ascribed to the *pn* junction formed between the *n*-type SiNWs and the *p*-type silicon substrate. It was checked that devices consisting of *p*-type SiNWs grown on *p*-type silicon substrates do not exhibit a rectifying effect.

The current-voltage characteristics shown in figure 3 become linear for $U > +300$ mV, the slope corresponding to the parasitic series resistance R_S. It is found that $R_S \approx 5$ Ω.cm². This value is slightly larger than that of typical industrial silicon wafer solar cells ($R_S \approx 2$ Ω.cm²), but much lower than that of CVD-grown SiNW array solar cells reported in the recent literature: Tsakalakos *et al.* obtained an R_S value of several 10 Ω.cm² as it can be seen in figure 1 of Ref. [5], and Stelzner *et al.* obtained an R_S value of the order of 150 Ω.cm² as it can be seen in figure 3(a) of Ref. [6]. This important reduction of the parasitic series resistance is probably due to the fact that our process includes a planarization step of the SiNW array, allowing to deposit a continuous and uniform conductive layer on top of the SiNWs.

We performed measurements of the sheet resistance R_{sh} of the ITO thin film and of the specific contact resistance ρ_C between the ITO and the Ni/Al front contact grid, by employing the transmission line method. We found $R_{sh} \approx 30$ Ω/□ and $\rho_C \approx 3\times10^{-3}$ Ω.cm². Using these values, the contribution of the front electrical contact to the parasitic series resistance of our SiNW array solar cell was calculated to be about 1.5 Ω.cm². The difference with the experimental value $R_S \approx 5$ Ω.cm² cannot be explained by the SiNW array resistance (estimated to be of the order of 10^{-4} Ω.cm²), but can be ascribed to the contact resistance between the SiNWs and the ITO layer.

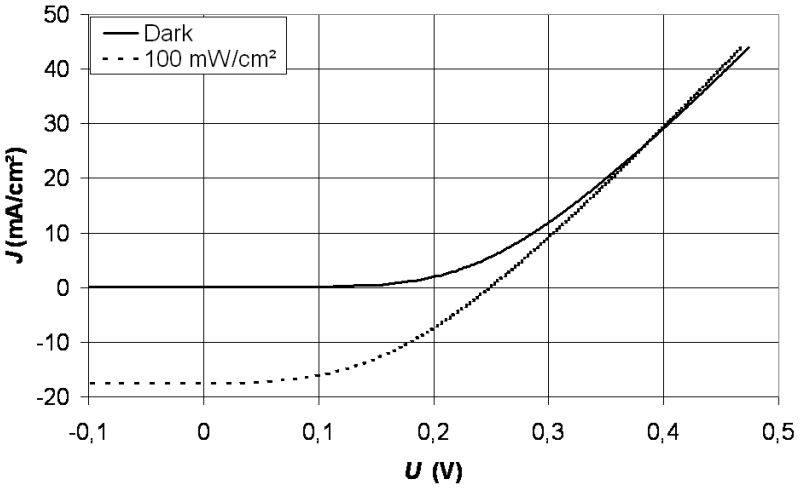

Figure 3. Dark and light current-voltage characteristics of a SiNW array solar cell, fabricated following the process presented in figure 1. For an illumination intensity of 100 mW/cm², the short-circuit current is 17 mA/cm^2, the open-circuit voltage is 250 mV, the fill factor is 44%, leading to an energy conversion efficiency of 1.9%. The *J-U* characteristics become linear for $U > +300$ mV, the slope corresponding to the parasitic series resistance R_S. It is found that $R_S \approx 5$ Ω.cm².

CONCLUSIONS

A novel process was developed for integrating CVD-grown SiNW arrays into functional photovoltaic devices. A crucial planarization step, achieved by embedding the SiNWs in a SOG matrix and subsequent polishing of the front surface, allowed to deposit a continuous and uniform ITO layer on top of the SiNW array, and thus to form a high-quality front electrical contact. The SiNW array solar cells fabricated using this process exhibited a parasitic series resistance as low as 5 Ω.cm², which is a clear improvement compared to the recent literature. Future works for obtaining even lower series resistance will focus on improving the contact resistance between the SiNWs and the ITO layer.

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