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Regrowth of 3C-SiC on CMP Treated 3C-SiC/Si Epitaxial Layers

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Abstract. In this work, we have investigated the 3C-SiC re-growth on planarized 3C-SiC epitaxial layers, grown on (001)Si, after the application of a chemical mechanical polishing (CMP) process. A specific polishing process was developed for 3C-SiC to achieve a flat, high-quality surface. The interface between the deposited 3C-SiC and the polished 3C-SiC on Si film was studied by TEM characterization to determine if defects appear at this interface. It was observed that no additional defects were nucleated at the interface. The resulting re-grown film roughness, as a function of film thickness, was studied and is reported along with recommendations for future work.

Introduction

Cubic SiC (i.e., 3C-SiC) is an attractive candidate for many applications due to the ability to growth single-crystal films on low-cost, large-diameter Si substrates. However 3C-SiC growth on Si is well known to produce rough surfaces due to the large lattice mismatch (> 20%) between 3C-SiC and (001)Si. This mismatch results in crystallographic defects that propagate along the <111> direction when growth on Si is performed. While the resulting film is single-crystal, the rough surface morphology is not optimal for subsequent device processing, such as silicon oxide growth for MOS-based devices or for further epitaxial growth. Planarization of the surface has been used by Capano et. al [1] to process 3C-SiC MOSFET's, but as a last step before device processing. One of the drawbacks of this approach is that a large quantity of the best quality 3C-SiC is removed by the chemical-mechanical polishing (CMP) process. This is because the film quality improves with growth time due to defect annihilation along the <111> directions. The re-growth of 3C-SiC, on a planarized seed film of 3C-SiC, might be the best approach to realize a device-quality layer for a MOSFET made from 3C-SiC.

Experimental

In this work we report on a process to planarize 3C-SiC on Si epitaxial films grown under low-pressure CVD (LPCVD) conditions at USF on two inch (2") (001)Si wafers in an inductively-heated SiC reactor. The growth process has been described elsewhere [2] and involves a standard dual-precursor process using silane and propane diluted in a hydrogen carrier. The process pressure was 150 Torr for all experiments conducted with a growth temperature ~ 1380 °C.

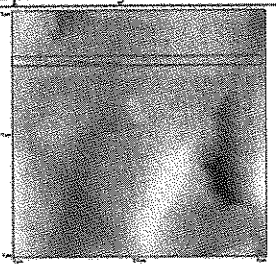
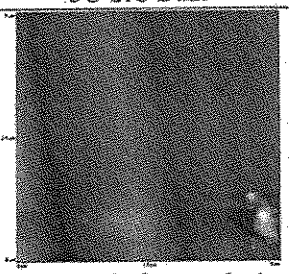
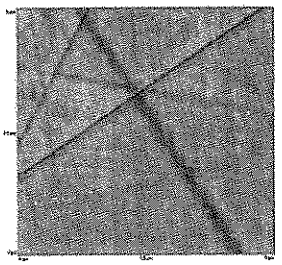
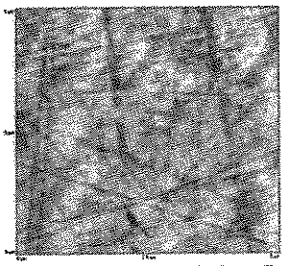
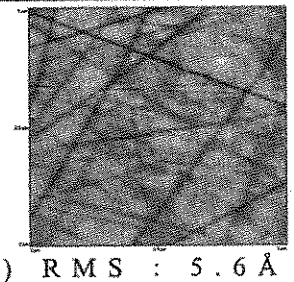
At NOVASiC, the 3C-SiC surfaces were studied with AFM and optical (Nomarski) microscopy and the surface root mean square (RMS) roughness was measured at each step of the process (epi growth, CMP and epi-regrowth).

Results and discussion

Epitaxial growth. Two inch diameter (001)Si substrates were first RCA cleaned and an epitaxial layer of 3C-SiC grown at USF under the above conditions. The epitaxial layer thickness was approximately 4 μm. Two wafers were processed in this manner and sent to NOVASiC for subsequent CMP planarization. The RMS roughness, as determined by AFM, was approximately 23 Å, as shown in Fig. 1(a).

Polishing. The goal of polishing is to obtain the lowest roughness with an absence of subsurface damage [3]. Mechanical polishing reduces the roughness and planarises the surface. After the mechanical polishing, the RMS roughness, as determined by AFM for a 5x5 μm^2 area, was 4.2Å (Fig. 1(b)). However mechanical polishing generates scratches and subsurface damage. NOVASiC has developed a CMP process for hexagonal SiC called StepSiC® which was tested for 3C-SiC as a starting point in the process development. Unfortunately when this process was applied to cubic SiC, the surface was scratched and the RMS roughness was higher than expected, at 5.6Å (Fig. 1(f)).

The CMP process developed in this work for 3C reduced the roughness from 23 Å to 2.3Å (Fig. 1(c)). In comparison, the best tuned CMP process on 3C-SiC bulk gives an RMS roughness equal to 3.3Å (Fig. 1(g)).

	Epitaxial layer of 3C-SiC	3C-SiC Bulk
As received	 a) R M S : 2 3 Å	 d) R M S : 3 1 Å
Mechanical polishing	 b) RMS : 4.2Å	 e) R M S : 6 . 7 Å
Chemical Mechanical Polishing Hexagonal SiC: StepSiC® [4]		 f) R M S : 5 . 6 Å :

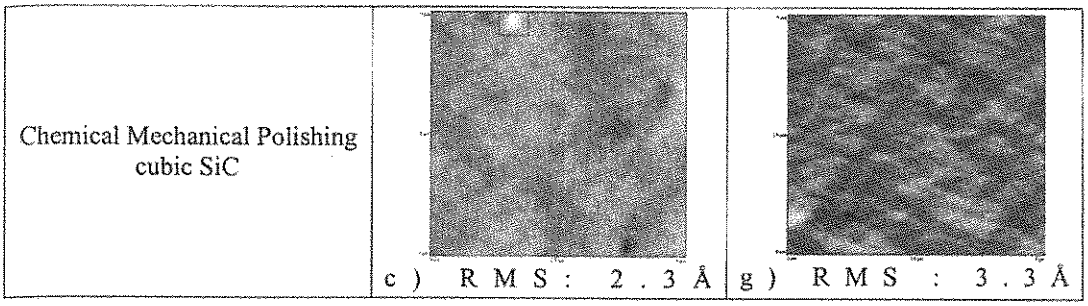


Figure 1 AFM data on 3C-SiC epitaxial layer on Si (100) ((a) as received, (b) after mechanical polishing and (c) after CMP) vs 3C-SiC bulk ((d) as received, (e) after mechanical polishing ,(f) after CMP "StepSiC®" – especially dedicated to hexagonal SiC - and (g) after CMP 3C). Data taken in non-contact tapping mode, scan size 5x5 μm², with an AutoProbe M5 tool.

Epitaxial regrowth. The first wafer, USF-03-227, was selected for epitaxial regrowth and the surface roughness was 23 Å after initial 3C growth and was improved to 2.3 Å after CMP processing. After CMP processing, the samples were returned to USF where they were diced into 1 cm squares for further processing. After an RCA clean, three samples were loaded into the epi reactor in sequence and homoepitaxial growth conducted under the following conditions: Si/C = 0.3, T ~ 1380 °C, P=150 Torr and for 30, 60 and 120 minutes so as to study the film morphology vs regrown film thickness. The resulting surface roughness was 15.9, 20.9 and 27.6 Å, respectively. Fig. 2 shows AFM images taken on sample USF-04-055A (60 min regrowth) at each step of the process. While the best result was for the thinnest regrown film, this sample was selected to show an intermediate result. In addition, SEM study of the surface indicated that the mosaic nature of the film was also altered compared with the original pre-CMP morphology, with larger terraces which might indicate a more optimal epi surface morphology for subsequent device processing.

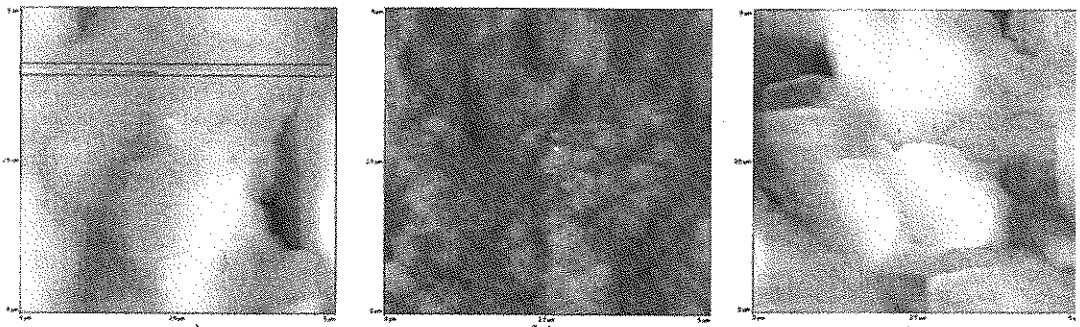
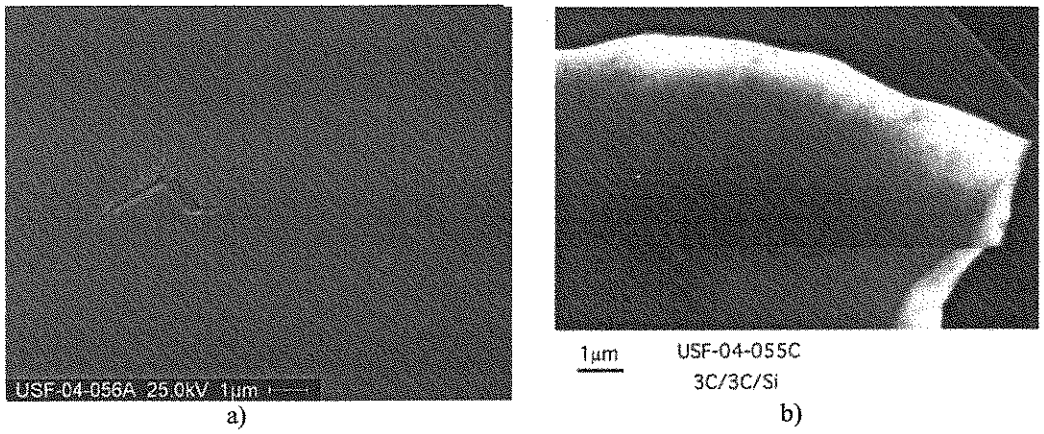


Figure 2 AFM data taken after (a) initial 3C-SiC on Si epi growth (USF-03-227), (b) CMP treatment and (c) re-growth of 3C-SiC on 3C-SiC (USF-04-055A). Surface RMS roughness is 23 Å, 2.3Å, and 20.9 Å, respectively. Data taken in tapping mode, scan size 5x5 μm².

Fig. 3(a) shows the resulting morphology for the thickest regrown film, USF-04-056A (2 hour regrowth). The sample was also studied using TEM to determine the defect structure at the regrowth interface, as shown in Fig. 3(b). This preliminary TEM analysis does not reveal the nucleation of extended defects at this interface. It should be noted, however, that the data reported here are very preliminary and have resulted from the first re-growth experiments. As a result, the current 3C-SiC homoepitaxial growth process is far from optimized.



a) b)

Figure 3 (a) Plan-view SEM micrograph of USF-04-056A after 120 min. of re-growth. (b) Cross-section TEM micrograph of the same sample showing a re-growth film thickness of ~ 3 μm and no additional defects nucleated at the re-growth interface.

Conclusion

The first trials of 3C-SiC homoepitaxial growth on chemical-mechanical polished 3C-SiC epilayer do not show the nucleation of extended defects at the regrowth interface. Further TEM analysis on these samples are needed to confirm this result. In the mean time, additional polishing runs will be performed in an effort to continue to decrease the surface roughness ; complementary measurements of the film using TEM, μRaman, etc. are planned in order to quantify the subsurface damage.

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