HIGH SPEED, LOW NOISE, FINE RESOLUTION TDI CCD IMAGERS

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ABSTRACT

It is well demonstrated that the CCD TDI mode of operation provides increased photosensitivity, relative to a linear CCD array, without the sacrifice of spatial resolution.

However, in order to utilize the advantages which the TDI mode of operation offers, attention should be given to the CCD TDI design and tradeoffs which exist between the pixel pitch, dead space between pixels in the horizontal direction, high speed, high photosensitivity, high spatial resolution and wide dynamic range. For example, a 2000 pixel TDI with an MTF of 0.5 will have an effective spatial resolution of only 1000 pixels. Other tradeoffs also are present, such as high speed versus power dissipation which exist both in the array and in the on-chip output video amplifier. Further, noise considerations exist at the video on-chip output amplifier. These include high speed which demands high bandwidth, Johnson noise, 1/f noise, reset noise, and output signal charge to voltage sensitivity.

In this paper we shall describe the novel approach which we used in the design of a 2048 × 96 TDI CCD imager. We shall show how we addressed successfully these design tradeoffs and issues. Details about the analysis and design of a high speed on-chip output amplifier will also be presented. In addition, we shall explain how the use of buried channel MOSFET's enabled us to address and solve the power dissipation, speed, and noise issues.

1. INTRODUCTION

A number of Time-delay-and-integration image sensors are reported in the literature [1-6]. These arrays use basically the frame transfer organization with the entire array exposed to illumination. One major recognised advantage of the TDI imager is that it can operate at extremely low light levels. Signal level increases as the number of TDI stages increases while the total noise level increases as by the square root of the number of stages.

Many area arrays including an array of 748 × 96 photoelements [7] used for electronic message systems operating at high speed have been described. Arrays of 2048 × 96 TDI focal plane arrays were reported by Bradley and Ibrahim [8] for use in electronic low light level surveillance systems. This array showed excellent performance except of limiting dynamic range due to signal ghosting. Most recently Schlig [9] reported a TDI 2048 × 32 photoelements operating at low light levels and high speed.

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Design goals common to many imaging devices include large photocharge packets to minimize shot noise, large output signal voltage excursions (before voltage amplification) to retain the excellent noise performance of CCD, and high clocking frequency capability to maximize the scanning speed. Also, the application of fine-line lithography is highly desirable to minimize the large chip sizes that characterize many imaging devices. To some extent, these goals are incompatible, dictating compromises. These issues apply to linear, area and as well to TDI optical imaging devices.

A Time-delay-and-integration mode of operation of a CCD imager provides increased sensitivity without the sacrifice of spatial resolution or data rate. The advantages of the TDI mode were extensively highlighted by Barbe et al [1,2,10]. A major advantage of the TDI mode is that the exposure time is increased by a factor (M) which is equal to the number of TDI stages, without affecting the geometrical resolution. This improves the low-light level capability without degrading the spatial resolution or data rate.

However, more specifically, in order to utilize the advantages which the TDI mode of operation offers, attention should be given to the CCD TDI design. Design trade-offs exist between:

(i) the imager architecture
(ii) pixel pitch
(iii) high speed
(iv) high photosensitivity
(v) low noise
(vi) wide dynamic range.

In addition, spatial resolution related issues include:

(i) geometry of the integration aperture
(ii) discrete nature of the charge motion
(iii) signal charge transfer efficiency
(iv) degree to which the average speed of the charge packets is matched to the speed of the scene which moves across the TDI imager.

Such issues were not addressed previously in the literature. In the design of our TDI CCD imagers we took into account these issues.

In our present paper we address some of these design tradeoff issues and highlight the important design considerations. This work was done as part of a development effort in the introduction of a family of new advanced CCD TDI image sensors and cameras. For the sake of clarity we shall deal only with the 2048×96 CCD TDI image sensor.

2. ARCHITECTURE

The basic architecture of the TDI 2048×96 imager is shown in Figure 1. There are 2048 active photoelements in the horizontal direction. On either side of the array there are dark isolation inactive pixels which are used to collect undesirable dark leakage current and also allow the first and last active pixels of the TDI imager to have identical responsivity characteristics as the rest of the pixels. In the vertical direction there are 96 pixels. We refer to these as M TDI stages. These are the summing TDI stages. Thus, the signal n_{sig} from a single photoelement site is given by:

$$n_{sig} = \sum_{i=1}^{96} n_{i.} \quad (1)$$

The total noise (n_{nt}) from the TDI section of the imager is given by:

$$n_{nt} = \left[\sum_{i=1}^{96} n_{ni}\right]^{1/2} \quad (2)$$

Figure 2 shows in more detail the TDI section of the imager. The basic photoelement is made up of four clock regions. The signal charge which is always shifted in the TDI vertical direction is synchronised with the velocity of the object. We could easily regard the TDI imager as been made up of 2048 illuminated shift registers which are 96 bits long. Each column in the vertical direction is electrically isolated from each other. As the signal is being shifted down in the verical direction and since the clock shift rate is synchronised with the velocity of the object, the signal grows as is shifted down in the vertical direction. We can regard this as equivalent of having an effective photoelement which is 96 times the area of the single photoelement unit. Effectively we increase the photocollective pel area without degrading the spatial resolution. This is explained later. Further, we also increase the integration time which is equivalent to the total shift time of M TDI stages.

We designed three versions of the 2048 × 96 imager.

(i) An imager with eight taped outputs and bidirectional,
(ii) An imager version with eight taped outputs and unidirectional.
(iii) A version of the same imager with a single output.

2.1. Tapped Bidirectional

The video signal of the 2048 by 96 TDI stages imager is readout by a horizontal readout shift register which consists of eight outputs. Each output section of the shift register reads out 256 photoelements at a rate of up to 25 MHz. The signal charge of the TDI stages can be shifted either vertically downwards or upwards at a command of an external clock. This property enables the TDI imager to scan in a bidirectional mode without the need of an additional scan delay. This architecture is displayed in Figure 1.

2.2. Tapped Unidirectional

The imager consists of 2048 by 96 TDI stages. In this architecture there is a CCD readout shift register with eight ouputs which are present only at the lower end of the TDI imager.Each output reads out 256 photoelements at a rate of up to 25 MHz.

2.3. Single output

In this 2048 × 96 TDI imager there is only one readout shift register of 2048 bits long at the lower side of the imager. Its output video rate can be up to 25 MHz.

2.4. Photoelement pitch size

A TDI imager with a small pixel size can use low cost lenses. In our present design, in both the horizontal andvertical dire ctions we have the pixel size at 13 microns center to center. Small photoelement pixel size makes the illuminator cheaper. For example for a TDI imager which has 26 × 26 microns pixel size it needs four times higher illumination power relative to our imager. For such a large pixel size, removal of heat generated by the illuminator becomes a problem.

2.5. On Chip Output Video amplifier

All the TDI imager architectures employ a buffer output video amplifier at the end of each CCD readout shift register. In order to reduce the 1/f noise source we developed a fully buried channel two stage source follower amplifier. We minimized the Johnson noise by optimizing the width of the buried channel MOSFET's. The design of such an amplifier was aided by the buried channel MOSFET model developed by Van der Tol and Chamberlain [11]. This amplifier which is attached to the floating signal charge sensing diffusion is further optimised to reduce the KTC noise (Equation (3)) and improve the charge to voltage signal conversion. To achieve this we developed special low doped source drain buried channel MOSFET devices.

$$n_{nKTC} = \left[\frac{KTC}{q}\right]^{1/2}. \tag{3}$$

2.6. Fine resolution and MTF

For improved MTF which is a measure of spatial resolution we require to have the movement of the signal charge in the TDI direction as continous as possible. Figure 3 shows the MTF due to charge motion as a function of the clocking scheme in the TDI section. It can be seen that with a four phase clocking scheme the MTF and hence the fine resolution is highest. At the Nyquist frequency with four phase MTF =0.974. While for three phase the MTF = 0.955 and for two phase the MTF = 0.900. In our TDI designs we use four phase clocking for optimum fine resolution.

Fine resolution is also determined by the charge transfer efficiency of the readout shift register. In our designs we use profiled buried channel CCD shift registers for high fringing fields and high charge transfer efficiency. We used the computer simulation program WATMOS [12] for two and three dimensional simulations of the channel potentials and signal charge positioning. Other more advanced simulation tools are also available in our laboratory [13]. Our channel potential maximum is 0.95 μm deep. For elimination of image lag from frame to frame we use complete charge transfer mode of operation. We eliminated completely the possibility of a bucket-brigate effect [14] either during operation in the CCD and at the output readout section. With a speed of 25 MHz output rate we achieve a trasfer charge inefficiency of $\varepsilon = 1\times10^{-5}$. With overlapping polysilicon gates there is always the possibility of the existence of deep potential wells in the space between the two polysilicon interelectrodes. Such problem would manifest itself in poor charge transfer efficiency, reduced dynamic range and degredation of the modulation transfer function (MTF). In our CCD technology we eliminate these undesirable effects by introducing impurity profiling.

3. SIGNAL CHARGE SENSING OUTPUT STRUCTURE OF THE TDI IMAGERS

The conventional CCD floating diffusion output device is well documented in the literature [15]. This sensing scheme is extensively used in CCD optical imaging devices. The KTC noise offered by this structure is usally high relative to the other noise components of the CCD image sensor. Further, for proper operation of its reset transistor, the potential of the drain must be greater than the potential of the buried channel corresponding to the reset level. In practice this condition is met only for a fractional-volt signal at the floating diffusion. It is not met for a wide range of buried channel designs. To overcome this problem Schlig and Chamberlain [16] developed and reported an novel output structure shown in Figure 4. This output stucture avoids undue restrictions on the buried channel design by skimming the signal charge from the floating diffusion into a virtual drain which is at a higher potential than the actual drain. The virtual drain is the empty potential well induced under two successive CCD electrodes which follow the reset gate in sequence along the register. The virtual drain is isolated

from the drain diffusion by a drain gate. The electrodes of the virtual drain receive two of the four serial clock phases, which pump the charge over the on-level potential barrier beneath the drain gate. Thus, the drain potential need only be larger than the upper tolerance limit of the off-level under the drain gate, which is the lowest potential of the CCD channel.

The lower limit of the floating potential swing, which occurs when the floating diffusion contains the maximum signal charge, is extended to the channel off-level by using a pulsed set gate in place of the usual DC barrier gate before the floating diffusion. The set pulse gate is identical to the drain gate pulse, and can be applied to both gates by direct internal connection.

The Schlig-Chamberlain output sensing structure is an excellent improvement of the conventional sensing diffusion scheme, however the improvement is achieved at the expense of a need of extra clocking pulse. In our TDI imagers we conceived a new output stucture which is an improvement on both the conventional and the Schlig-Chamberlain output structure. In our new output sensing structure we employ profiled low doped donor regions in order to decrease the local electric fields, and most important to decrease and minimize the KTC and 1/f noise of the output sensing structure. In our sensing device the effective capacitance of the signal charge node is significantly reduced relative to the other sensing devices.

4. NOISE SOURCES, DYNAMIC RANGE AND TDI GAIN

The dynamic range of the TDI imager is defined as the maximum signal charge divided by the total rms noise equivalent electrons. The maximum photoelement signal charge capability depends on the size of the pixel, the effective CCD storage gate capacitance and the available channel potential swing. Four phase clocking operation in the TDI section enable us to optimize the maximum signal charge per photosite. We can achieve up to 500×10^3 signal electrons per pixel. The total rms noise includes components such as, the dark leakage current component which is given by

$$\left[\frac{MA\tau_t}{q} \left\{ \frac{qn_iW}{2\tau} + \frac{qD_n}{L_n} \frac{n_i^2}{N_A} + \frac{qS_on_i}{2} \right\} \right]^{1/2} . \tag{4}$$

In our CCD TDI image sensors this component comes to a total rms value of 1 electron at room temperature.

The rms bulk trapping noise in the profiled CCD shift register is given by

$$\left[\frac{m}{14} AL_D \left(1 - e^{-\frac{\tau}{\tau_e}} \right) e^{-\frac{\tau}{\tau_e}} \right]^{1/2} . \tag{5}$$

The total rms noise due to the bulk states and charge transfer inefficiency is 6 electrons, at room temperature.

The Johnson noise associated with the sensing diffusion of the CCD readout shift register depends on the effective sensing diffusion capacitance and is given by:

$$\left[\frac{KTC_{on}}{q^2} \right]^{1/2} . \tag{6}$$

In our 2048×96 TDI imager this component is 12 electrons.

The rms output amplifier noise is given by:

$$\left[\frac{C_{on}^2}{q^2}\,\frac{4KT\alpha\Delta B}{g_m}\right]^{1/2}. \tag{7}$$

Our amplifier has a total noise of 15 electrons. All the symbols have their usual meaning.

The geometric sum of all these noise components gives the total noise of the TDI imager comes to a total rms noise at room temperature of 20 electrons.

The dynamic range of the imager depends on the transfer function and linearity of the output amplifier and the total noise. Further, as the number of TDI stages increases the dynamic range of the imager decreases. A plot of the imager dynamic range as a function of the number of TDI stages is shown in Figure 5. In our 2048 × 96 imager we achieve a dynamic range of 7000.

4.1. TDI sensitivity gain

In Figure 6, we show the sensitivity improvement factor as a function of the number of TDI stages. The ideal sensitivity improvement factor would correspond to the number of TDI stages. However, this sensitivity gain factor decreases depending on the design and more specifically on the total noise of the imager. In our 2048 × 96 CCD TDI imager we get a sensitivity gain factor within 3% of the number of TDI stages. In our imager, the total noise is only 20 electrons.

5. Conclusions

We developed and used a novel approach in the design of a family of TDI CCD image sensors. We addressed succesfully a number of design trade-off issues and we realized an optimum 2048 × 96 CCD TDI imager. Optimized the dynamic range of the imager, its MTF for fine resolution, minimized its total noise and maximized its total TDI sensitivity gain. Such optimum imager enables the user to fully utilize the advantages which the TDI mode of operation offers. Also, because of the small pixel pitch and small imager chip size the user is able to use low cost optics.

6. Acknowledgements

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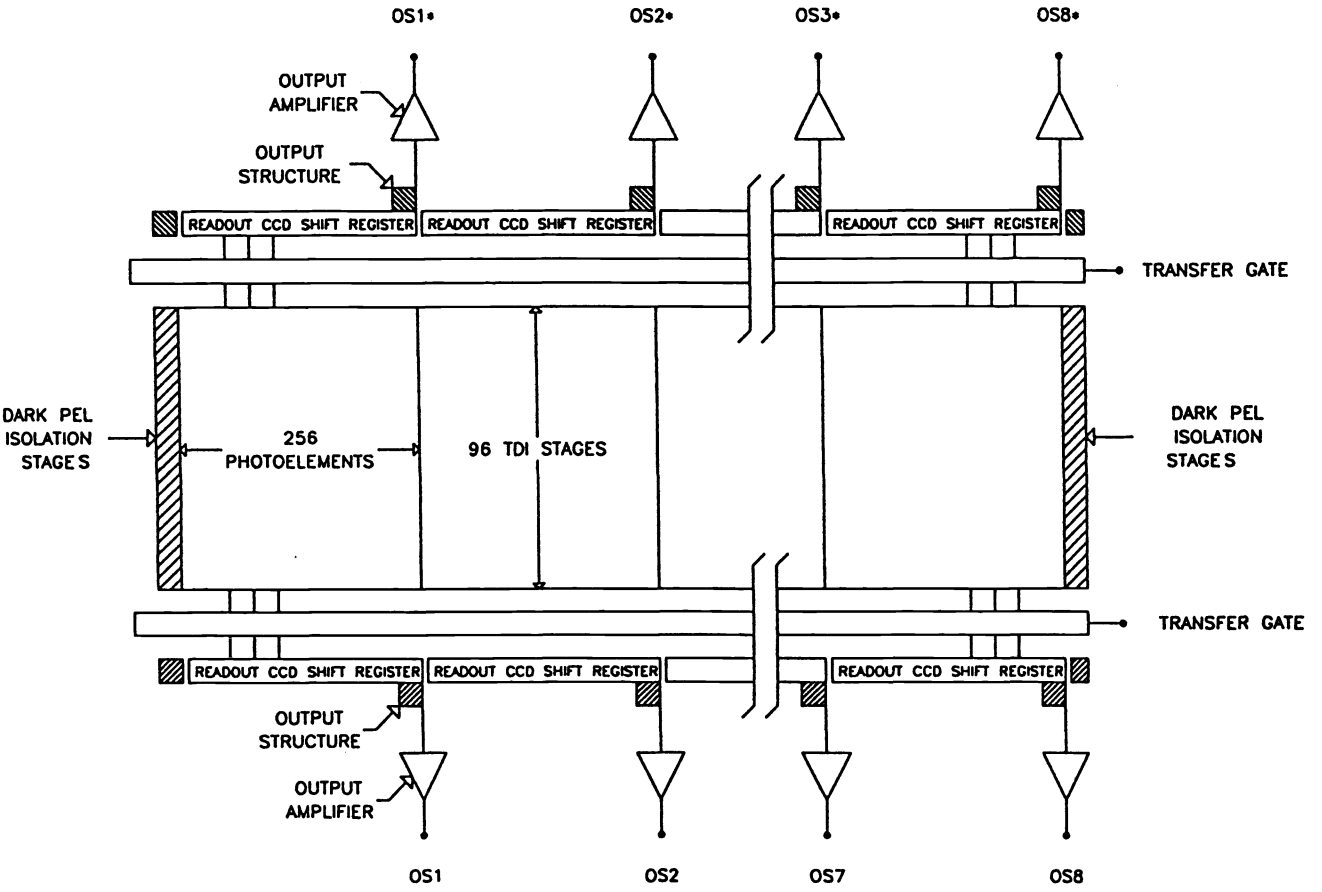

Figure 1: Architechure of a bidirectional 2048×96 TDI CCD image sensor.

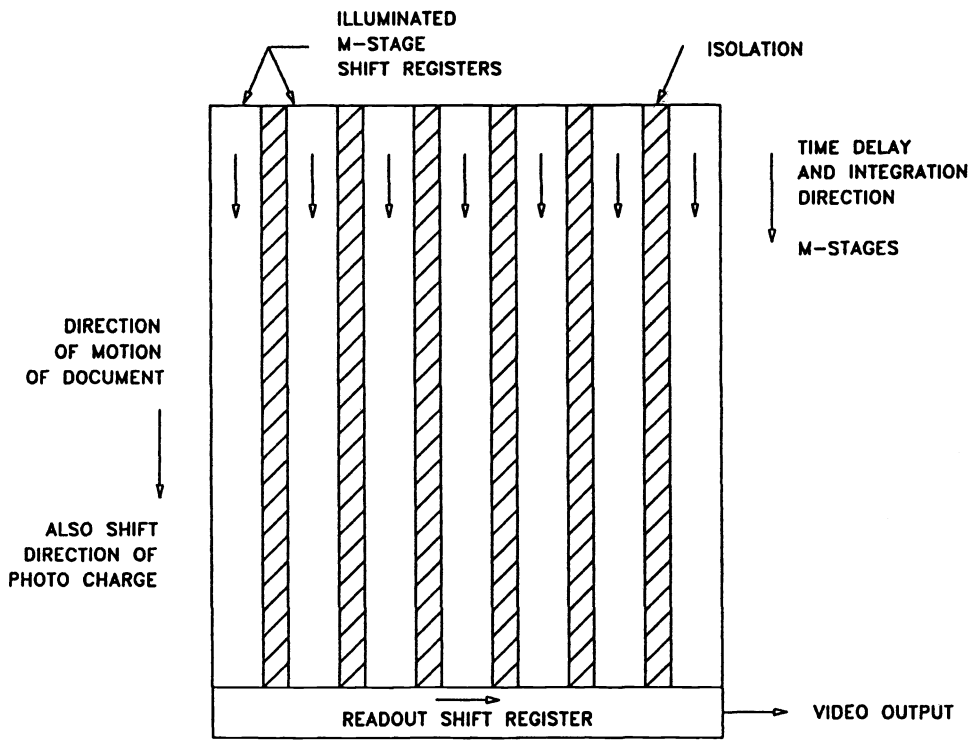

Figure 2: Organization of a CCD Time-Delay-and-Integration imager, showing the signal charge movement direction. Each basic photoelement is made up of ϕ_1, ϕ_2, ϕ_3, and ϕ_4 regions.

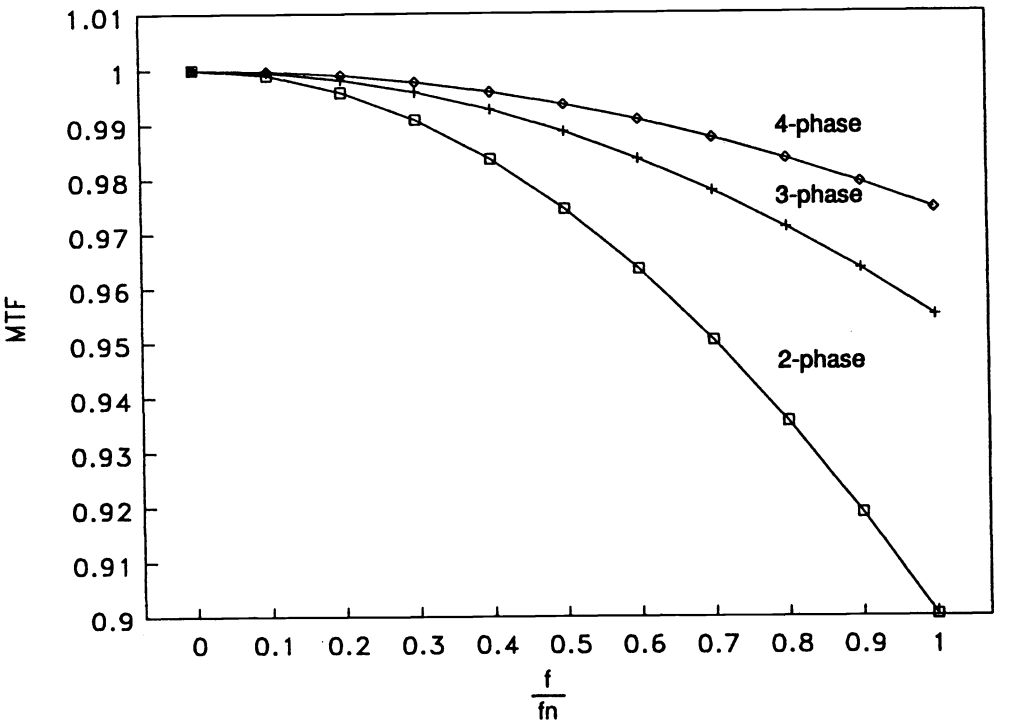

Figure 3: Effect of the noncontinuous motion of the signal charge on the modulation transfer function. 4-phase provides more continuous motion of signal charge relative to 2-phase.

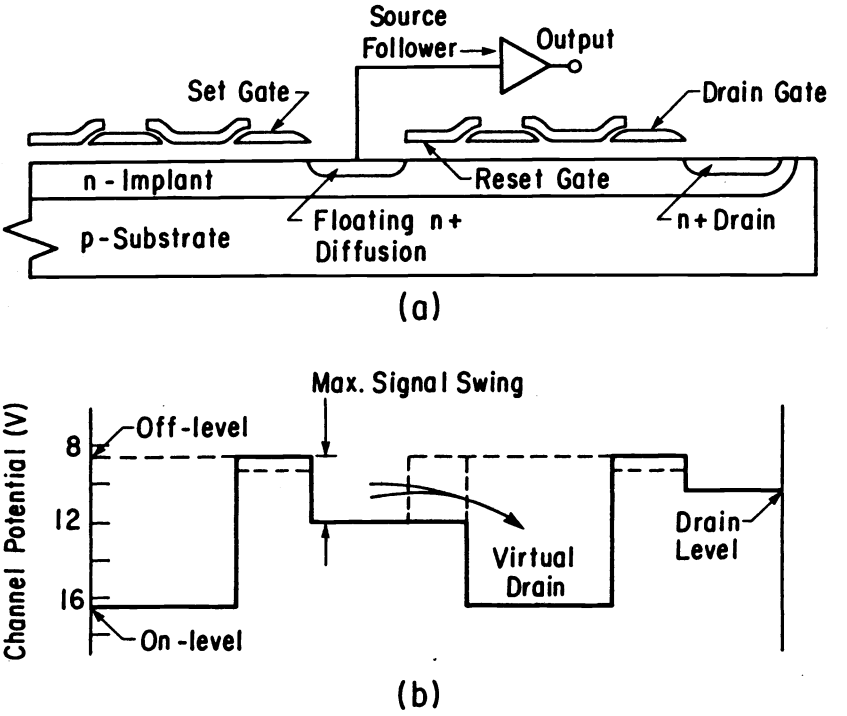

Figure 4: The Schlig-Chamberlain high speed large signal swing CCD output structure[16].

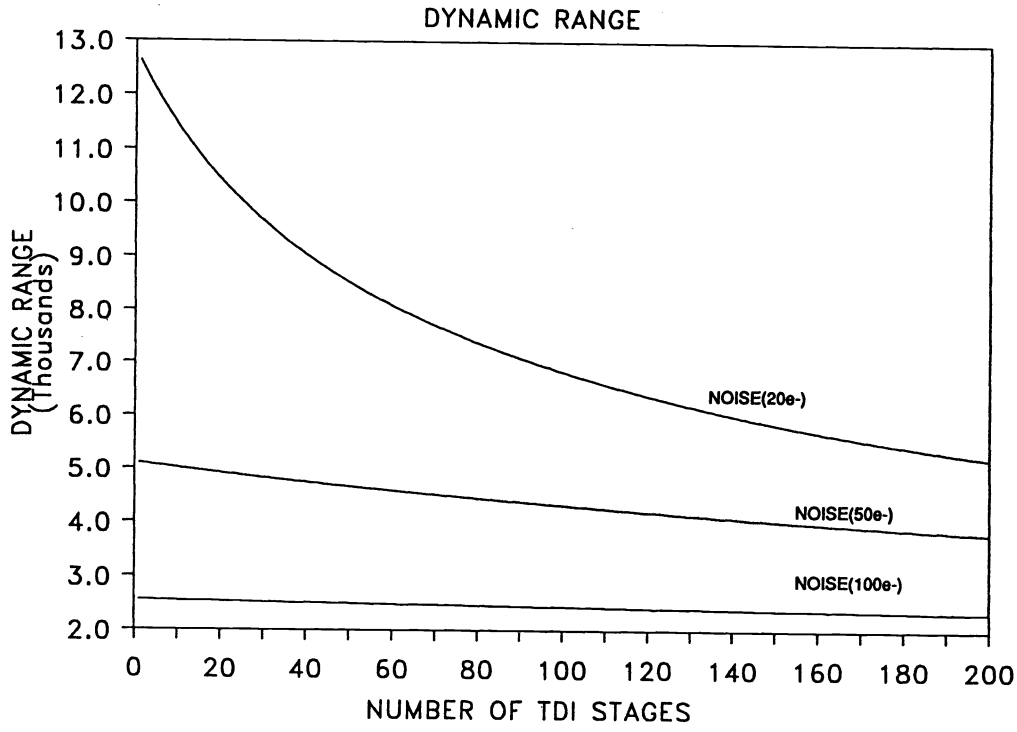

Figure 5: Dynamic range of the 2048 × 96 TDI imager as a function of the total rms electron imager noise. Our imager has 20 noise electrons.

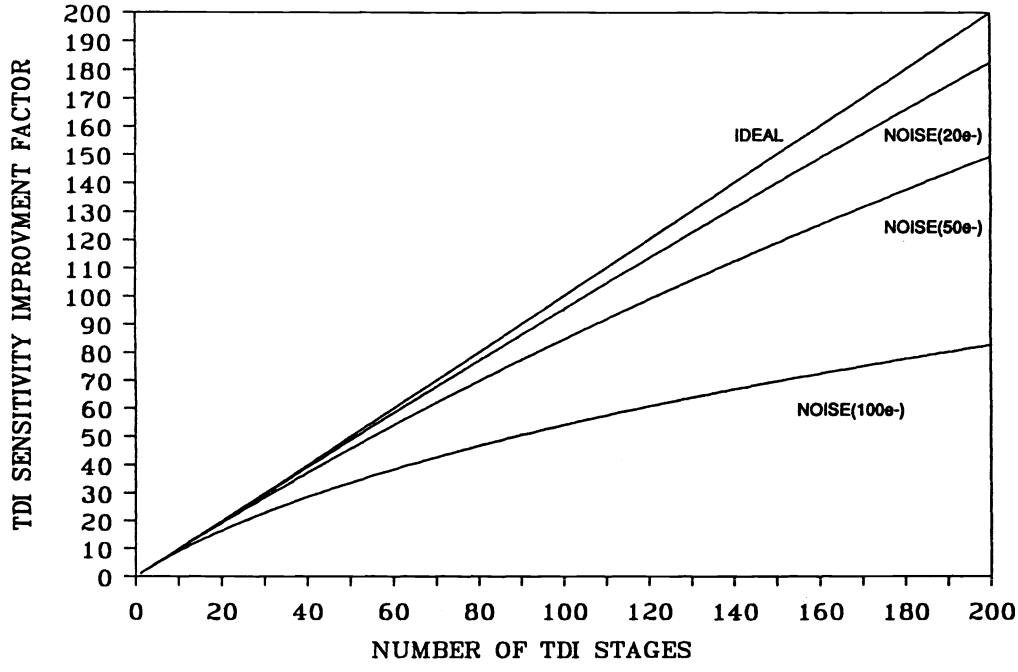

Figure 6: TDI sensitivity improvement as a function of the number of TDI summing stages. Our 2048 × 96 imager has 20 noise electrons and achieves a sensitivity improvement within 3% of the ideal.