Oxide Nanoelectronics on Demand

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Electronic confinement at nanoscale dimensions remains a central means of science and technology. We demonstrate nanoscale lateral confinement of a quasi–two-dimensional electron gas at a lanthanum aluminate–strontium titanate interface. Control of this confinement using an atomic force microscope lithography technique enabled us to create tunnel junctions and field-effect transistors with characteristic dimensions as small as 2 nanometers. These electronic devices can be modified or erased without the need for complex lithographic procedures. Our on-demand nanoelectronics fabrication platform has the potential for widespread technological application.

Controlling electronic confinement in the solid state is increasingly challenging as the dimensionality and size scale are reduced. Bottom-up approaches to nanoelectronics use self-assembly and templated synthesis; examples include junctions between self-assembled molecule layers (*1*, *2*), metallic and semiconducting quantum dots, carbon nanotubes (*3*–*6*), nanowires, and nanocrystals (*7*, *8*). Top-down approaches retain the lithographic design motif used extensively at micrometer and submicrometer scales and make use of tools such as electron-beam lithography, atomic force microscopy (AFM) (*9*), nanoimprint lithography (*10*), dip-pen nanolithography (*11*), and scanning tunneling microscopy (*12*). Among the top-down approaches, those that begin from modulation-doped semiconductor heterostructures have led to profound scientific discoveries (*13*, *14*).

The interface between polar and nonpolar semiconducting oxides displays remarkable properties reminiscent of modulation-doped semiconductors (*15*–*21*). When the thickness of the polar insulator (e.g., $LaAlO_3$) exceeds a critical value (d_c = 3 unit cell), because of the polarization discontinuity at the interface, the potential difference across $LaAlO_3$ will generate a "polarization catastrophe" and induce the formation of a quasi–two-dimensional electron gas (q-2DEG) at the interface joining the two insulators (*17*). In addition to the key role played by the polar discontinuity, there is evidence that, when present, oxygen vacancies in the $SrTiO_3$ also contribute to the formation of the electron gas (*22*, *23*).

We focus on $LaAlO_3$-$SrTiO_3$ heterostructures. Because of the large conduction-band offset between $LaAlO_3$ and $SrTiO_3$, the q-2DEG is confined largely within the first few unit cells of $SrTiO_3$ (*22*, *24*), with very little penetration into the $LaAlO_3$ layer (*25*). Electric fields have been used to control the metal-insulator transition at room temperature (*17*) and the superconductor-insulator transition at cryogenic temperatures (*21*). Further in-plane confinement of the q-2DEG has been achieved by lithographically modulating the thickness of the crystalline $LaAlO_3$ layer (*26*). Control over the metal-insulator transition at scales of <4 nm was demonstrated by means of a conducting AFM probe (*24*). This latter method forms the basis for the results reported below.

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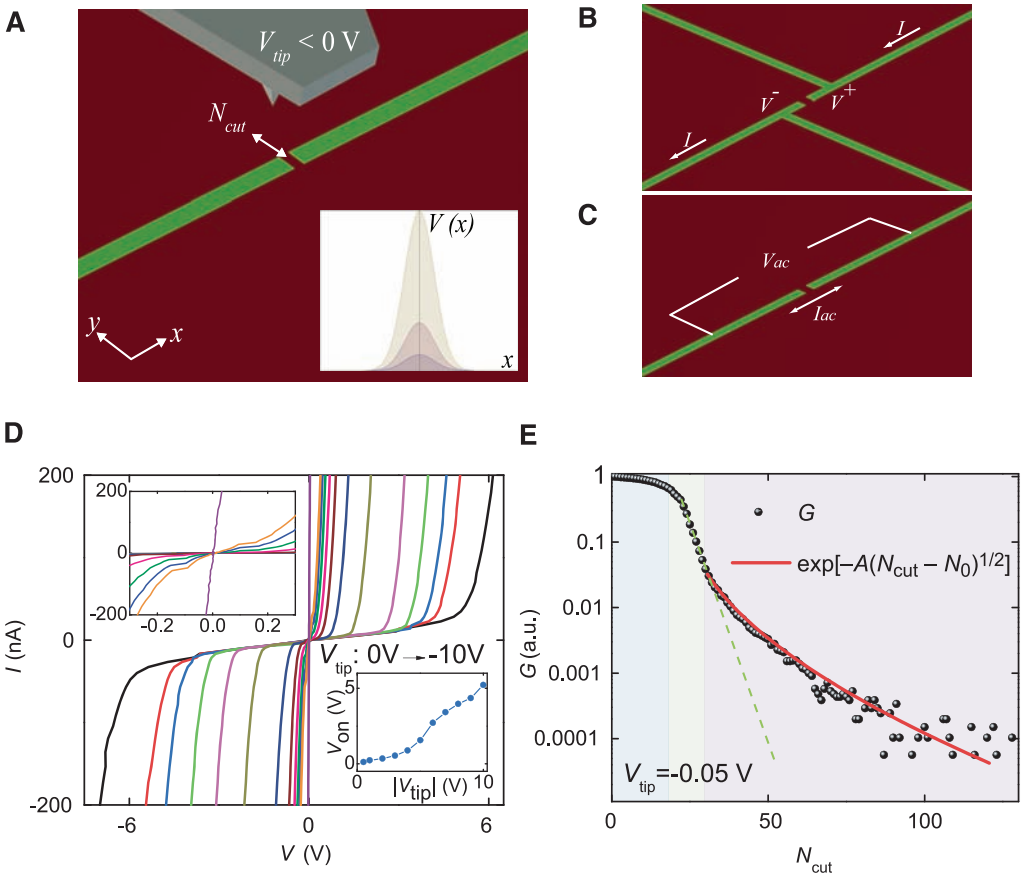

Fig. 1. Creation of nanoscale tunnel barriers. (**A**) Sketch illustrating how a potential barrier is created by scanning a negatively biased AFM probe. Inset: Sketch of the barrier potential. Either increasing the magnitude of negative tip bias (V_{tip}) or scanning across the wire for a greater number of cuts (N_{cut}) with the same tip bias will increase the height of the barrier potential $V(x)$. (**B**) Illustration of structure used for four-probe measurement (**C**) Sketch of two-probe ac measurement scheme. (**D**) *I-V* characteristics of an uncut wire section 2 μm long and 12 nm wide (V_{tip} = 0 V), and the same section with various potential barriers in the middle created with different negative tip bias (V_{tip} = –0.5 V, –1 V, –2 V, …, –10 V). The upper inset shows the conductance of the uncut wire (slope of the *I-V* curve) to be 6.8 μS. The lower inset shows the turn-on voltage of the nanowire section with a potential barrier as a function of the V_{tip} that is used to create the barrier. (**E**) Conductance of a wire 12 nm wide, with a potential barrier at the middle written with V_{tip} = –0.05 V, measured as the number of cuts N_{cut} increases (i.e., barrier height increases). The green dashed line shows an exponentially decaying conductance G as a function of barrier height, $G \propto \exp[-A'N_{cut}]$, which is typical for thermal activated hopping. The red solid line shows a reference curve following behavior, $G \propto \exp[-A(N_{cut} - N_0)^{1/2}]$ as expected by us for tunneling, with best-fit parameters A = 0.99, N_0 = 17.2.

Writing and erasing. On the basis of the experimental finding that nanoscale conducting regions can be created and erased using voltages applied by a conducting AFM probe (*24*), various multiterminal devices have been constructed. The structure investigated here consists of nominally 3.3 unit cell thick $LaAlO_3$ films grown on $SrTiO_3$ [see (*27*) for fabrication and measurement details]. A conducting AFM tip is scanned along a programmed trajectory $x(t)$, $y(t)$ with a voltage $V_{tip}(t)$ applied to the tip. Positive tip voltages above a threshold $V_{tip} > V_t \sim 2$ to 3 V produce conducting regions at the $LaAlO_3$-$SrTiO_3$ interface directly below the area of contact. The lateral size δx of this conducting nanoregion increases monotonically with tip bias. Typical values are $\delta x = 2.1$ nm and 12 nm at $V_{tip} = +3$ V and +10 V, respectively (fig. S2, A and B). Subsequent erasure of the structures can be induced by scanning with a negative voltage or by illuminating with light of photon energy $E > E_g$ (band gap of $SrTiO_3 \sim 3.2$ eV) (*17*, *18*). Structures can be written and erased hundreds of times without observable degradation (fig. S2C). All of the structures described here are written within the same working area; similar structures have been created and measured for other electrode sets, with consistent results.

Designer potential barriers. The writing and erasing process allows for a remarkable versatility in producing quantum mechanical tunneling barriers (Fig. 1A). The transport properties of these tunnel barriers are investigated in two different experiments. Both begin with nanowires (width $w \sim 12$ nm) written with a positive tip voltage $V_{tip} = +10$ V. In the first study, a four-terminal transport measurement is performed. A current (I) is sourced from two leads, while a second pair of sense leads is used to measure the voltage (V) across a section $L = 2$ μm at the middle of the nanowire (Fig. 1B). As prepared, the nanowire is well-conducting (resistance $R_0 = 147$ kilohms, corresponding to a conductivity $\sigma = 6.8$ μS) (Fig. 1D, upper inset). This conductivity together with the nanowire's aspect ratio (length/width = 160) yield a sheet conductance $\sigma_S = 1.1 \times 10^{-3}$ S, which is ~200 times that of the unstructured sample with $LaAlO_3$ film thickness exceeding d_c [$\sigma_S^{film} \approx 2 \times 10^{-5}$ S (*17*)].

A negatively biased tip ($V_{tip} < 0$ V) is then scanned across the wire. *I-V* curves are acquired after each pass of the tip. Scanning with a negative bias restores the insulating state, presumably by shifting the local density of states in the $SrTiO_3$ upward in energy (*24*), thus providing a barrier to conduction (Fig. 1A, inset). The tip bias starts at $V_{tip} = -0.5$ V and then increases linearly in absolute numbers (–1 V, –2 V, –3 V, …, –10 V). All these *I-V* characteristics are highly nonlinear (Fig. 1D), showing vanishing conductance at zero bias, and a turn-on voltage V_{on} (defined as the voltage for which the current exceeds 10 nA) that increases monotonically with tip voltage (Fig. 1D, lower inset). A small residual conductance (4.1 nS) is observed, which is independent of V_{tip} and hence is associated not with the nanowire and tunnel barrier but with an overall parallel background conductance of the heterostructure.

In the second study, an AFM tip is scanned repeatedly across a nanowire with relatively small fixed bias $V_{tip} = -50$ mV (Fig. 1A). An alternating voltage ($V_{ac} = 1$ mV) is applied across the nanowire (Fig. 1C) and the resulting in-phase ac current I_{ac} is detected with a lock-in amplifier. With each pass of the AFM tip, conductance $G = I_{ac}/V_{ac}$ decreases monotonically, exhibiting three qualitatively distinct regimes (Fig. 1E). For $N_{cut} < 10$, we observe that the conductance reduces only slightly with each pass. For $10 < N_{cut} < 25$, the behavior transitions to one in which the conductance decays approximately exponentially with N_{cut}. For $N_{cut} > 25$, we observe a clear deviation from this straight exponential fall-off. We propose that the AFM probe is gradually increasing the potential barrier between the nanowire leads (*24*). Although this process must eventually saturate for large N_{cut}, for the regime explored the potential appears to scale linearly with N_{cut}, as suggested by the observed dependence of the conductance with N_{cut} over many experiments (Fig. 1E). Along the center of the wire, the induced potential after N_{cut} passes is therefore described by an effective potential: $V_N(x) = V_0 + N_{cut}V_b(x)$, where $V_b(x)$ is a sharply peaked (~2 nm wide) function of position. The conductance of the nanowire measured as a function of N_{cut} (Fig. 1E) shows evidence for a crossover from a highly conducting regime ($N_{cut} < 10$) to an exponential thermal hopping regime ($10 < N_{cut} < 25$) to one dominated by quantum mechanical tunneling through the barrier ($N_{cut} > 25$). The latter nonexponential form is consistent with a tunneling probability $t \propto \exp[-A'(V - E_F)^{1/2}]$ (where A' is a material-dependent constant, and E_F is the Fermi energy), as can be seen by a comparison with the functional dependence $G \propto \exp[-A(N_{cut} - N_0)^{1/2}]$ (where G is the conductance across the barrier, and A and N_0 are dimensionless fitting parameters). We conclude that the barrier written by the AFM tip acts as a tunnel junction that interrupts the written nanowires.

SketchFET. The ability to produce ultrathin potential barriers in nanowires enables the creation of field-effect devices with strongly nonlinear characteristics. We demonstrate two families of such devices. Both begin with a "T-junction" of nanowire leads written with $V_{tip} = 10$ V ($w \sim 12$ nm)

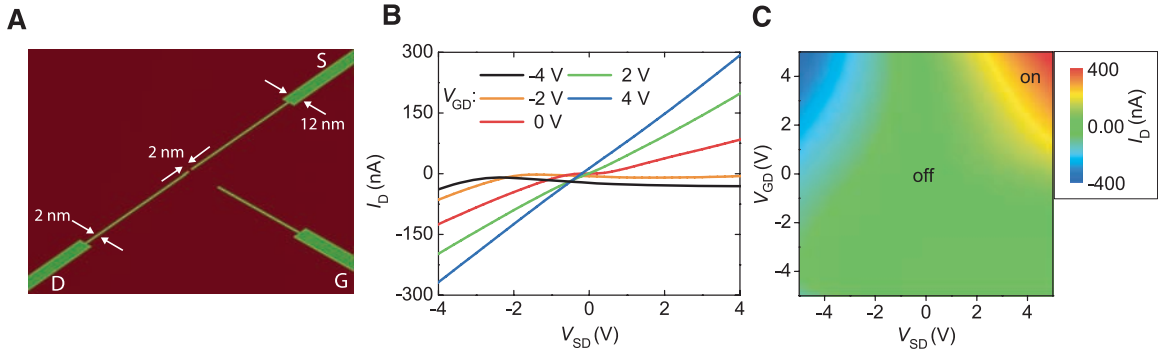

Fig. 2. SketchFET device. (**A**) Schematic diagram of SketchFET structure. S, source electrode; D, drain electrode; G, gate electrode. (**B**) *I-V* characteristic between source and drain for different gate biases $V_{GD} = -4$ V, –2 V, 0 V, 2 V, and 4 V. (**C**) Intensity plot of I_D (V_{SD}, V_{GD}).

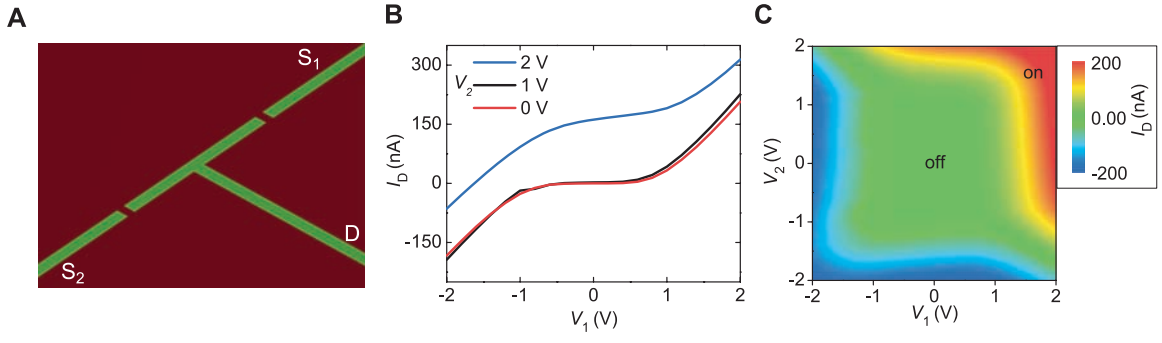

Fig. 3. Double-junction device. (**A**) Schematic of a double-junction structure. (**B**) *I-V* characteristic between source 1 and drain for different source biases $V_2 = 0$ V, 1 V, and 2 V. (**C**) Intensity plot of $I_D(V_1, V_2)$.

(fig. S3A). As constructed, the T-junction behaves as a simple resistive network (fig. S3B).

The creation of the first device (Fig. 2A) begins with erasing the central region (within 1 μm from the center) of a T-junction of source, gate, and drain electrodes and then reconnecting the channels with V_{tip} = 3 V (w ~ 2 nm), followed by a subtractive step in which the AFM probe is scanned under negative bias (V_{tip} = –3 V), starting from the center of the junction across the source-drain channel and moving a gap distance g_2 = 50 nm along the direction of the gate electrode. This step also creates a barrier g_1 = 2 nm between source and drain. The asymmetry in the two gaps (fig. S4A) enables the gate electrode to modulate the source-drain conductance with minimal gate leakage current. We refer to this device as a SketchFET (sketch-defined electronic transport within a complex-oxide heterostructure field-effect transistor).

Transport measurements of this SketchFET are performed by monitoring the drain current I_D as a function of the source and gate voltages (V_{SD} and V_{GD}, respectively). Both V_{SD} and V_{GD} are referenced to the drain, which is held at virtual ground. At zero gate bias, the I-V characteristic between source and drain is highly nonlinear and nonconducting at small $|V_{SD}|$ (Fig. 2B). A positive gate bias $V_{GD} > 0$ lowers the potential barrier for electrons in the source and gate leads. With V_{GD} large enough (≥4 V in this specific device), the barrier eventually disappears. In this regime, ohmic behavior between source and drain is observed. The field effect in this case is nonhysteretic, in contrast to field effects induced by the AFM probe (*24*). At negative gate biases the nonlinearity is enhanced, and a gate-tunable negative-differential resistance (NDR) is observed for $V_{SD} > -2.5$ V. When a sufficiently large gate bias is applied, a small gate leakage current I_{GD} also contributes to the total drain current I_D (fig. S4A). The NDR regime is associated with this gate leakage current (see below).

By increasing the source-drain gap (g_1 = 12 nm) of the SketchFET (fig. S5), the source-drain characteristic becomes more symmetric. This structure requires a larger positive gate bias to switch the channel on. Tunneling through such a wide barrier width is highly unusual, but it is assisted by the triangular nature of the tunneling barrier under large applied fields (on the order of MV/cm), and the barrier width is renormalized by the large dielectric constant of $SrTiO_3$ (ε ~ 300 at room temperature).

One of the most important technological applications of FETs is making logic elements. The applied values of V_{SD} and V_{GD} can be interpreted as "on" (>4 V) or "off" (<4 V) input states of a logic device; the measured values of I_D can be understood as "on" (>200 nA) or "off" (<200 nA) output states. A full exploration of $I_D(V_{SD}, V_{GD})$ reveals an "AND" functionality (e.g., output is "on" only when both inputs are "on") (Fig. 2C). Because of the nonlinear character of the junction, the resultant drain current when both V_{SD} and V_{GD} are "on" is ~3 times the sum of the individual contributions when only one input is "on": I_D(4 V, 4 V) ~ 3[I_D(4 V, 0 V) + I_D(0 V, 4 V)], which yields a promising on-off current ratio.

Frequency response. One gauge of the performance of a transistor is its ability to modulate or amplify signals at high frequencies, as quantified by the cutoff frequency f_T. We characterized the frequency dependence of the SketchFET described in Fig. 2 using a heterodyne circuit that incorporates the SketchFET as a frequency mixer. The experimental arrangement is shown schematically in fig. S6A.

The results of this heterodyne measurement over a frequency range 3 kHz to 15 MHz show that the SketchFET operates at frequencies in excess of 5 MHz. In the measurement setup used, this frequency is most likely limited by the large (~megohm) resistance of the three leads connecting to the device. The high mobility of the channel and the fact that the I-V characteristics are far from saturation

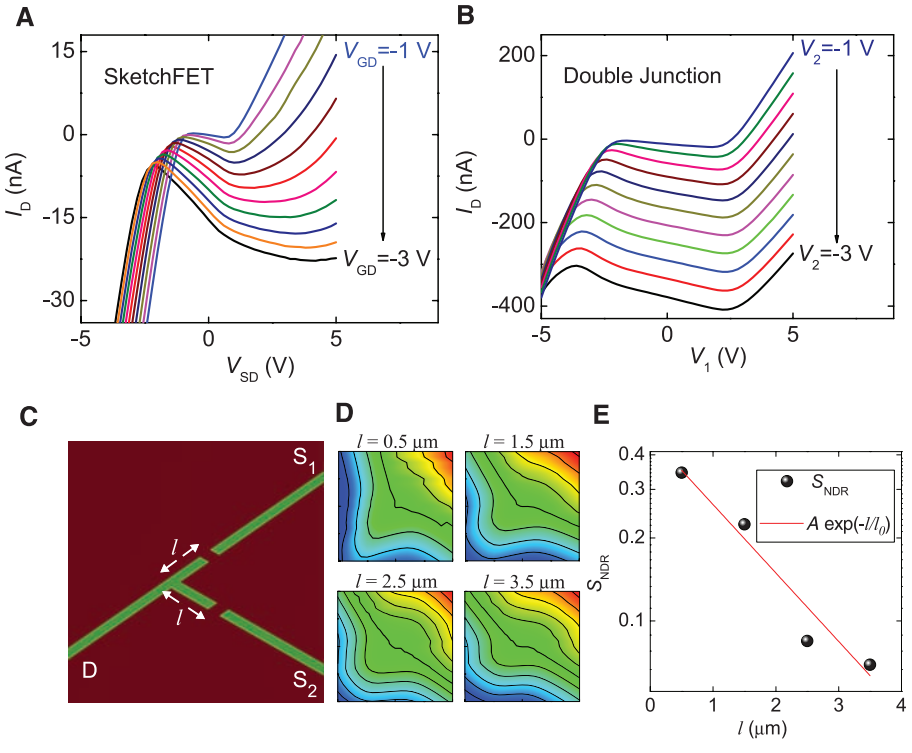

Fig. 4. Negative differential resistance (NDR). (**A**) NDR observed in SketchFET structure. Gate bias V_{GD} ranges from –1 V to –3 V with steps of –0.2 V. (**B**) NDR observed in double-junction structure with a junction separation of 5 μm. Source bias V_2 ranges from –1 V to –3 V with steps of –0.2 V. (**C**) Schematic of a structure of two perpendicular junctions with a distance l from the junction center. (**D**) For structures with l = 0.5 μm, 1.5 μm, 2.5 μm, and 3.5 μm, drain current I_D is plotted as V_1 and V_2 is varied from –2 V to 2 V. Contours are spaced 100 nA apart. (**E**) Coupling strength S_{NDR} = max[$-(\partial I_D/dV_1)/(\partial I_D/dV_2)$], equivalent to largest contour line slope, plotted as a function of l (black dots) fitted with exponential decay function A exp($-l/l_0$), with best-fit parameters A = 0.47, l_0 = 1.75 μm.

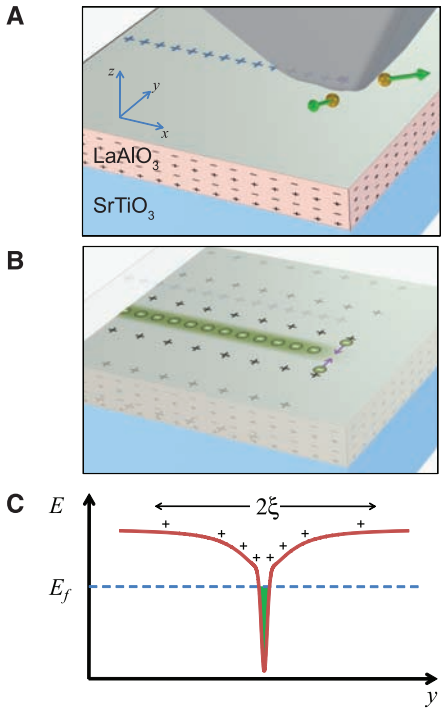

Fig. 5. Lateral modulation doping of nanowires. (**A**) AFM tip moving left to right above $LaAlO_3$-$SrTiO_3$ heterostructure, removing oxygen-containing ions and locally changing the charge state of the surface. (**B**) View of same structure revealing the conducting nanowire formed at the interface. Electrons screen the surface charges by ionizing nearby states in the $SrTiO_3$ (lateral modulation doping) as well as from the top surface. (**C**) Illustration of potential profile across the nanowire. Modulation doping occurs over a screening length ξ on the order of micrometers; E_f describes the Fermi energy.

in the conducting regime suggest that f_T of the SketchFET, without the large lead resistances, could extend into the gigahertz regime.

Double junction. The fabrication of a second family of structures begins by patterning the T-junction, followed by two erasure steps in which a negatively biased AFM probe (V_{tip} = –10 V) scans across two of the leads (Fig. 3A). The result is a device with two comparable tunneling gaps separated by a distance l from the intersection. The *I-V* characteristic of each junction is shown in fig. S4B. The electrodes connected by these two sections are labeled S_1 and S_2; the third electrode is labeled as "drain" (D). Transport experiments to measure the drain current as a function of the voltages V_1 and V_2 applied to S_1 and S_2, respectively [$I_D(V_1, V_2)$]. performed using the methods described above. Positive values of V_2 have little effect on the *I-V* characteristic between S_1 and D (Fig. 3B), and vice versa. Negative values of V_2 can induce NDR in the channel between S_1 and D. A full exploration of $I_D(V_1, V_2)$ reveals an "OR" functionality (e.g., drain output is "on" when either one of the source inputs is on) (Fig. 3C), which is not surprising given the topology of the junctions. We refer to this structure as a double junction.

Negative differential resistance. A qualitative explanation of the SketchFET NDR (Fig. 4A) originates from the fact that for a three-terminal junction each nanowire exhibits a field effect on the other two. When $|V_{SD}|$ is small, conductivity between source and drain is greatly suppressed; I_D is mainly composed of current from the negatively biased gate. Increasing V_{SD} will improve the conductivity between gate and drain and will drive more negative gate current to the drain, which manifests itself as NDR. When $|V_{SD}|$ is large enough, the drain current I_D is dominated by current flowing from the source, and the NDR vanishes.

For the double-junction structure, the origin of the NDR (Fig. 4B) is less straightforward. To study the nature of the coupling, we created a family of double-junction structures and characterized them for various distances l between the junctions and the center of the T-intersection (Fig. 4C). The normalized magnitude of NDR is quantified as $-(\partial I_D/dV_1)/(\partial I_D/dV_2)$, which can be visualized as the slope of contour lines in a two-dimensional plot of $I_D(V_1, V_2)$. Smaller values of l resulted in stronger coupling between the two junctions (Fig. 4D), manifested as a larger NDR effect. The coupling strength—given by the maximum NDR observed, $S_{NDR} = \max[-(\partial I_D/dV_1)/(\partial I_D/dV_2)]$—is calculated as a function of junction separation (Fig. 4E). An approximately exponential decay of this coupling strength is observed, with a fitted decay length l_0 = 1.75 μm.

The long-range coupling of tunnel junctions is consistent with the observation that the sheet conductance of the nanowires is two orders of magnitude larger than for unpatterned interfaces. A possible explanation of where these extra electrons come from, consistent with both observations, is sketched in Fig. 5. The writing process is assumed to create positively charged regions (e.g., oxygen vacancies) on the top $LaAlO_3$ surface (Fig. 5A) (*24*). Directly below, at the $LaAlO_3$-$SrTiO_3$ interface, electrons screen this positive charge (Fig. 5B). These electrons can come from two sources: either from the top $LaAlO_3$ surface, or from weakly bound donor states (associated with defects in the $SrTiO_3$) that become ionized over a length scale ξ in the range of several micrometers (Fig. 5C). This screening is a type of lateral modulation doping that can produce a considerably higher electron density relative to planar unpatterned q-2DEG as well as a lateral potential profile much wider than the real conductive nanowire region. Experiments in which many parallel wires are connected show saturation of the net conductance toward the unpatterned q-2DEG value, again consistent with this picture of lateral modulation doping.

The high conductance of the 12-nm wires, produced by the large (~100 MV/cm) transient electric field of the AFM probe, is metastable and prone to partial relaxation toward the unpatterned q-2DEG value on a time scale that depends on the ambient environmental conditions. Experiments performed on a SketchFET stored under vacuum conditions (fig. S8) show a nonexponential decay of the overall conductance (dominated by that of the 12-nm leads) toward a steady-state value that is comparable to the sheet conductance of the unpatterned film. No discernible degradation in the SketchFET switching performance was observed over a 9-day period. The extreme sensitivity of electron tunneling to barrier thickness demonstrates that the SketchFET and related structures are stable at length scales that are small relative to their feature size (e.g., 2-nm gap) and at time scales considerably longer than the observation period.

Concluding remarks and outlook. The nanoscale structures patterned above are representative of a versatile family of nanoelectronic devices operating at the interface between a polar and a nonpolar oxide insulator. The conducting nanostructures have dimensions comparable to those of single-walled carbon nanotubes, yet they can be freely patterned and repeatedly modified. Their ultimate suitability for logic and memory applications will depend on a variety of factors, such as the mobilities of the charge carriers, how effectively power dissipation can be minimized, and whether this system can be integrated with silicon. The devices demonstrated here suggest many other possible applications and research directions.

With sufficient control it may be possible to demonstrate single-electron effects such as Coulomb blockade, resonant tunneling, or single-electron transistor behavior, possibly at room temperature. At low temperatures, strongly correlated electron behavior associated with low dimensionality (i.e., Luttinger liquid behavior) may also be accessible. The discovery and control of superconductivity at the $LaAlO_3$-$SrTiO_3$ interface (*20*, *21*) provides a possible avenue for exploration of mesoscopic superconducting phenomena.

A 2-nm nanowire carrying 100 nA of current will produce an in-plane magnetic field $B \sim 10$ G at the top surface of the $LaAlO_3$. These magnetic fields are large enough to excite and detect spin waves in nearby magnetic nanostructures, and if the frequency response can be improved, it may be possible to sketch current loops around nanoscale samples for nuclear magnetic resonance or electron spin resonance experiments. On-site amplification of these small signals might be possible with SketchFET-based preamplifiers.

The tunnel junctions at the center of the SketchFETs may be optimized to be sensitive to the charge or oxidation state of the $LaAlO_3$ surface above. The active area is <5 nm^2, allowing for high spatial selectivity for a variety of biological and chemical sensing applications.

The $LaAlO_3$-$SrTiO_3$ system is sufficiently versatile to allow basic materials physics questions to be addressed. Previously we showed (*24*) that the measured width of written nanowires places a strong constraint on the thickness of the q-2DEG layer. Four-terminal resistance measurements were performed on nanowires by creating nanowire sense leads. The experiments with double junctions provide new quantitative evidence for in-plane modulation doping. Such self-referential measurements will continue to be useful in learning more about this fascinating material system.

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Figs. S1 to S8

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REPORTS

Macroscopic 10-Terabit–per–Square-Inch Arrays from Block Copolymers with Lateral Order

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Generating laterally ordered, ultradense, macroscopic arrays of nanoscopic elements will revolutionize the microelectronic and storage industries. We used faceted surfaces of commercially available sapphire wafers to guide the self-assembly of block copolymer microdomains into oriented arrays with quasi–long-range crystalline order over arbitrarily large wafer surfaces. Ordered arrays of cylindrical microdomains 3 nanometers in diameter, with areal densities in excess of 10 terabits per square inch, were produced. The sawtoothed substrate topography provides directional guidance to the self-assembly of the block copolymer, which is tolerant of surface defects, such as dislocations. The lateral ordering and lattice orientation of the single-grain arrays of microdomains are maintained over the entire surface. The approach described is parallel, applicable to different substrates and block copolymers, and opens a versatile route toward ultrahigh-density systems.

Producing a surface with an ultradense array of addressable nanoscopic elements that is perfectly ordered over macroscopic length scales is a formidable challenge. The self-assembly of block copolymers (BCPs), two chemically dissimilar polymers joined together, is emerging as a promising route to generate templates and scaffolds for the fabrication of nanostructured materials and offers a potential solution to this challenge (*1*–*3*). Despite the substantial advances that have been made to enhance the lateral ordering of the BCP microdomains in thin films, achieving perfect order over macroscopic length scales has not been possible (*4*–*7*). In thin films, BCPs self-assemble into grains, tens of microns in size, of laterally ordered nanoscopic microdomains. Electron beam (e-beam) lithography is a serial writing process, and although slow, has been successfully used to produce nanoscopic chemical or topographic surface patterns that can be used to guide the self-assembly of BCPs (*4*, *5*, *8*, *9*). However, even though the self-assembly of BCPs can correct errors in the patterns, perfect ordering over large areas has not yet been achieved. Nanoimprint lithography (*10*, *11*), on the other hand, is a parallel patterning process but requires a perfect master to replicate. We show that most of these limitations can be overcome by capitalizing on a well-established surface reconstruction of commercially available single-crystalline wafers to generate nanoscopic surface facets that can guide the self-assembly of BCPs into a highly ordered, single-grain array of nanoscopic elements with a well-defined orientation over large areas.

Large, defect-free single-crystalline wafers, such as silicon or sapphire, with a well-defined orientation of the crystal lattice are commercially available (*12*–*14*). By the cutting of single crystals along specific crystallographic planes, unstable surfaces can be produced that, upon heating, reconstruct, generating crystal facets that form a sawtooth topography, where the orientation of the ridges formed by the sawtooth persists over the entire surface (*13*, *14*). Sapphire (α-Al_2O_3), cut along the $(10\bar{1}0)$ or M plane, is used as an example, although the concept applies to other single-crystalline materials. The surface reconstruction is shown schematically in Fig. 1 along with atomic force microscopy (AFM) images of a freshly cut and a faceted sapphire surface (*13*, *14*). Initially the surface is featureless. Upon annealing, the surface reconstructs and crystalline facets form a sawtooth pattern on the surface. With the sapphire substrates used in this study, the pitch of the sawtooth was varied from 160 to 24 nm, with peak-to-valley heights or amplitudes ranging from 20 to 3 nm by being annealed in air at temperatures from 1300° to 1500°C for 24 hours [supporting online material (SOM), section S1]. Crystallographic registry of the facets over macroscopic distances is ensured, because the sapphire is a single crystal (*14*). There are, though, dislocations and an ~26% variation in the pitch, randomly located across the surface.

Five different polystyrene-*block*-poly(ethylene oxides) (PS-*b*-PEOs), with number-average molecular weights (M_n) from 7 to 43.0 kg/mol, polystyrene-*block*-poly(2-vinylpyridine) (PS-*b*-P2VP) (M_n = 19.5 kg/mol), and PS-*b*-P4VP (M_n = 19 kg/mol), all with narrow molecular weight distributions and minor volume fractions of ~0.3, were used (SOM, section S1). In the bulk, these BCPs microphase-separate into hexagonal arrays of cylindrical microdomains of PEO, P2VP or P4VP in a PS matrix. Thin films of the BCPs were spin-coated onto the faceted surfaces, which were cleaned with oxygen plasma (SOM, section S1).

Shown in Fig. 1E is a solvent-annealed, 24-nm-thick (as measured on a flat surface) film of PS-*b*-PEO (M_n = 43.0 kg/mol) on a sapphire surface, with facets having an average pitch of 130 nm and amplitude of 14 nm. Upon solvent annealing, the film is sufficiently thin that the copolymer is entrained into and confined within the regions between the facets. The solvent annealing process orients and orders the PS-*b*-PEO (*15*), but the average period is 23 nm, much less than the 29.5-nm period seen for this copolymer solvent annealed on a smooth surface. Consequently, the confinement causes a reduction in the fundamental period of the copolymer, as seen in studies of copolymers confined between planar surfaces (*16*–*18*) or within lithographically generated surface patterns (*19*). The facets essentially isolate strips of the copolymer across the surface.

With increasing film thickness, the amount of copolymer within each sawtooth increases, effectively reducing the amount of lateral confinement, which gives rise to the observed increase in the repeat period of the copolymer (SOM, section S2). When the film is sufficiently thick, as shown in Fig. 1F for a 34-nm-thick film of the same copolymer on a surface with facets having a pitch of 100 nm and amplitude of 10 nm, solvent annealing generates a single hexagonal array of cylindrical microdomains oriented normal to the film surface, with an average period of

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