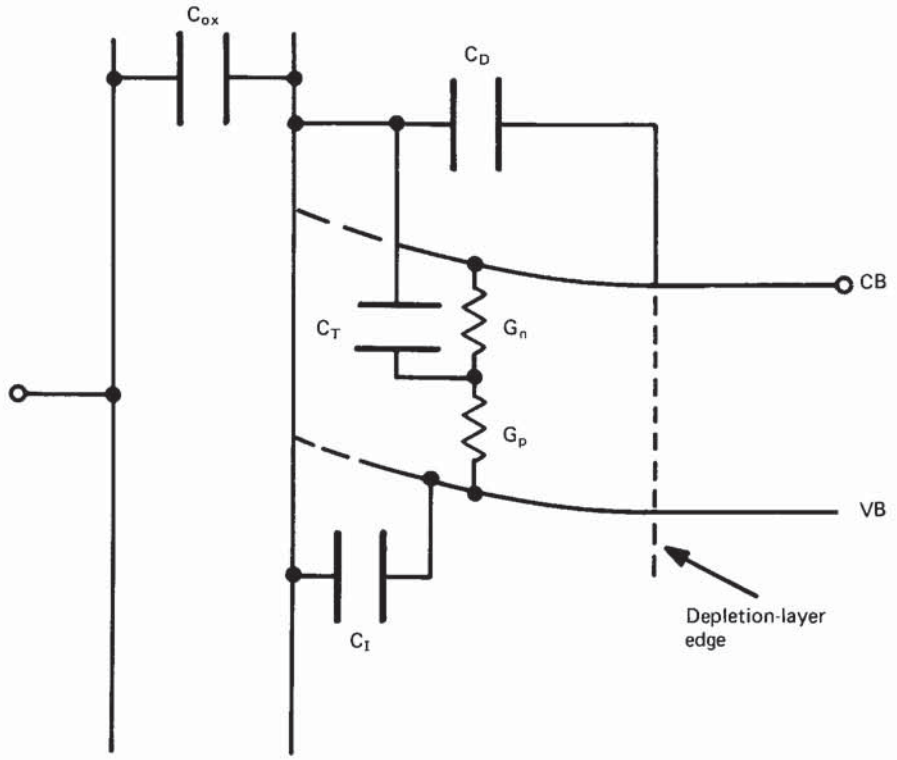

Figure 56. Equivalent circuit of n-substrate MOS capacitor with single-energy interface levels. C_{ox}, C_D, C_T and C_I represent the capacitances associated with the oxide, the depletion region, the traps and the inversion layer respectively. G_n and G_p represent the loss associated with the trapping of carriers from the bands into the interface states. In depletion G_p and C_I are small and can be ignored. Open circles denote external terminals. After Nicollian and Brews (1982).

To aid insight into the main concepts involved, we shall initially assume that all interface traps have the same energy level. The equivalent circuit for a device with an n-type substrate is shown in figure 56. In depletion, G_p and C_I are very small and can be ignored. For a single-level interface trap in depletion, the equivalent parallel conductance G_P and capacitance C_P (figure 58 (*b*)) are given by

$$G_P/\omega = C_T\omega\tau[1 + (\omega\tau)^2]^{-1}, \tag{7.12a}$$

$$C_P = C_T[1 + (\omega\tau)^2]^{-1} + C_D, \tag{7.12b}$$

where $\tau = C_T/G_n = f/\sigma vn$. In figure 57 we show the behaviour of G_P/ω for a single-level interface trap.

Single-energy-level interface traps are not observed in device-grade interfaces. What is observed are many interface trap levels so closely spaced in energy within the silicon band gap that they cannot be distinguished in the measurement as separate levels. For a distribution of interface trap levels in depletion, the equivalent circuit of figure 56 becomes the equivalent circuit of figure 58 (*a*). The equivalent parallel

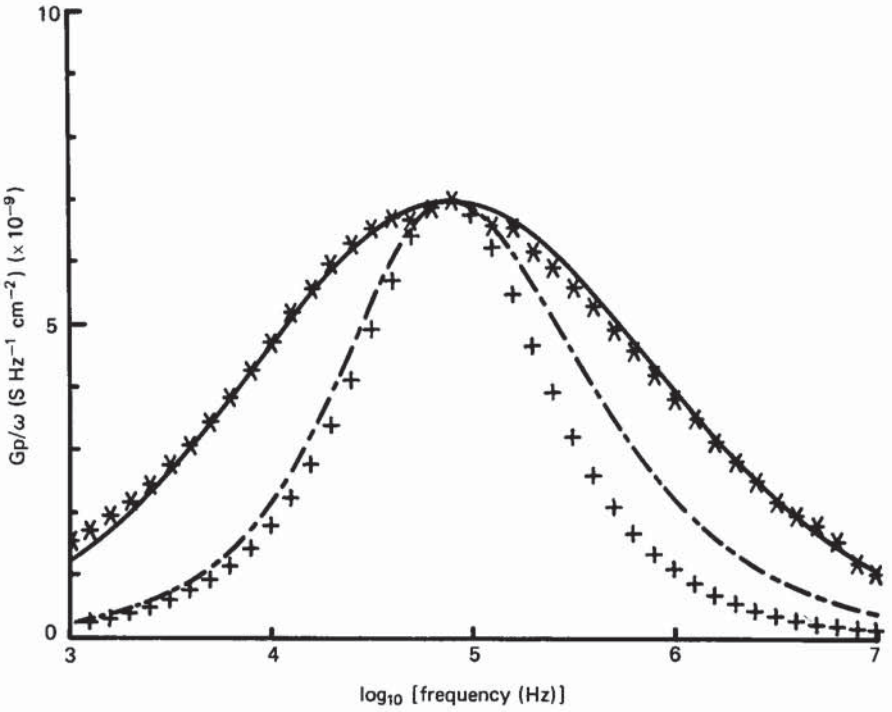

Figure 57. Equivalent parallel conductance G_P/ω against frequency for n-substrate MOS capacitor in depletion. (+) Single-level interface traps based on equation (7.12*a*). The values of τ and C_T have been adjusted such that the theoretical peak fits the observed peak. The dot–dashed line shows G_P/ω resulting from a distribution of interface trap levels based on equation (7.13*b*). The values of τ_n and C_{it} have been adjusted to fit the observed peak. The measured values are represented by stars and the continuous line is the fit based on equation (7.14). The capture cross-section is $5{\cdot}26 \times 10^{-16}\,\mathrm{cm}^2$, $D_{it} = 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ and potential fluctuations $\sigma_s = 1{\cdot}69kT$. Figure courtesy of S. Collins.

capacitance and conductance are now given by

$$C_P = C_D + C_{it}(\omega\tau_n)^{-1} \tan^{-1}\omega\tau_n, \qquad (7.13a)$$

$$G_P/\omega = C_{it}(2\omega\tau_n)^{-1} \ln [1 + (\omega\tau_n)^2], \qquad (7.13b)$$

where $\tau_n = (\sigma v n)^{-1}$. The behaviour of G_P/ω as a function of ω is also shown in figure 57.

Figure 57 shows that, although an experimental G–ω curve follows the trends predicted by equations (7.12*a*) and (7.13*b*), it is much broader than expected. Two models have been proposed to explain the observed time-constant dispersion. The first model invokes a distribution of band bending over the interfacial plane caused by a random distribution of discrete charges in the oxide: small variations in potential will produce large variations in τ_n since the latter is exponentially dependent on the band bending ϕ_s. The second model assumes a spread of capture probabilities related to the defects being distributed into the oxide. Model 1 was proposed by Nicollian and Goetzberger (1967) and has been widely used to interpret G–ω data. Model 2 was proposed by Prier (1967) on the basis of the model of Heiman and Warfield (1965).

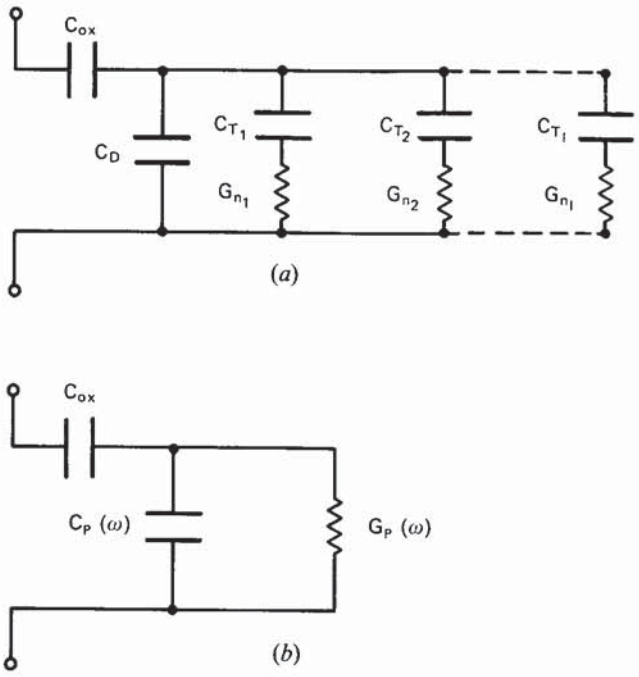

Figure 58. (*a*) Equivalent circuit for a distribution of interface levels across the silicon band gap in n-substrate MOS capacitor. (*b*) Lumped parallel equivalent of circuit in (*a*). After Nicollian and Brews (1982).

The main argument against model 2 is the experimental observation of a symmetric peak in the measured loss, whereas model 2 predicts a frequency-independent loss for a uniform distribution of trapping centres in the oxide. We shall consider this point further in section 7.3. Assuming a Gaussian distribution of potential fluctuations, we find that equation (7.13*b*) becomes

$$\frac{G_P}{\omega} = \frac{qD_{it}(2\pi\sigma_s^2)^{-1/2}}{2\omega\tau_n}\int_{-\infty}^{\infty}\exp\left(-\frac{\eta^2}{2\sigma_s^2}\right)\exp(-\eta)\ln[1+(\omega\tau_n)^2\exp(2\eta)]\,d\eta, \tag{7.14}$$

where $\eta = \phi_s - \langle\phi_s\rangle$ represents the band bending and σ_s is a parameter that describes the width of the measured curve. Through the fitting of expression (7.14) to the experimental data (see figure 57) one can determine the cross-section, interface-state density and band-bending fluctuations.

The conventional view of interface states is that at a given position in the band gap they have a *single* well defined cross-section. The width of the measured G_P/ω curve arises from surface-potential fluctuations. This is at variance with the results of noise measurements, which indicate the presence of defect states with cross-sections and trapping time constants spanning many decades. This apparent paradox is discussed in the next section.

7.3. *Observation of '1/f-noise' states in conductance measurements on MOS structures*

As we have seen, carrier trapping into localized defects in the oxide close to the Si/SiO_2 interface generates RTSs in the drain current and hence $1/f$ noise.

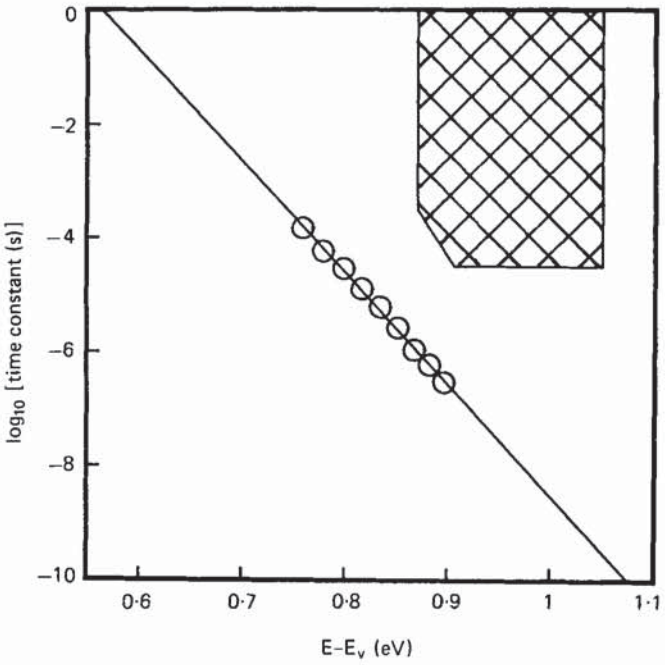

Figure 59. The measured time constant against surface Fermi level in the upper half of the band gap. The cross-hatched area shows the region to which noise measurements typically have access. O shows the interface-state loss peak from G_P/ω measurements; the data correspond to the capacitor shown in figure 61 (*a*). After Uren *et al.* (1989a).

The cross-hatched area on figure 59 depicts the time and energy windows in which the RTSs are measured in our n-channel (p-substrate) devices in both weak and strong inversion; the straight line depicts the peak time constant of interface states measured with the conductance technique on n-substrate capacitors in depletion. Thus the techniques look in different time windows. To get a $1/f$ spectrum requires a uniform distribution of trap time constants on a log time scale. In figure 59 this corresponds to a uniform distribution along any vertical line within the cross-hatched area.

The question that now needs to be addressed is the following: Are the defect states responsible for $1/f$ noise observable in the conductance technique? Eaton and Sah (1972) found a marked asymmetry in their measured conductance spectrum, which they ascribed to the long time constants arising from carrier tunnelling from interface states into defect states in the oxide. They noted that this mechanism would also cause $1/f$ noise. Unfortunately, their samples were sufficiently non-standard that their work has been totally overlooked. They used oxides 8 nm thick, with interface-state densities of about $10^{13}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, and the experiments were carried out at low temperatures. Since in the early 1980s the accepted experimental evidence pointed to only a single, symmetrical broad peak in G–ω data and the origins of $1/f$ noise in MOSFETs were still uncertain, Ngai and Liu (1982) concluded that $1/f$ noise could not be caused by carrier trapping and must therefore be due to some form of dielectric-loss mechanism.

An alternative way of formulating the problem is to ask whether the time constants (cross-sections) of the $1/f$ states shown in figure 59 extend to shorter times to meet the

single time constant measured for interface states in G–ω measurements. If there were no states in the gap between the cross-hatched area and the straight line shown in figure 59 then there would be an easily measurable upper limit to the frequency at which a $1/f$ spectrum could be observed; such a limit has never been recorded. On the other hand, conventional understanding of G–ω measurements suggests that there is only a single well defined peak corresponding to a single well defined time constant (cross-section). To resolve this apparent paradox, we carried out G–ω measurements down to 0·25 Hz such that this time-window gap was investigated for standard MOS structures (Uren *et al.* 1989a, b).

Measurements were carried out on conventional aluminium-gate MOS capacitors, of area $6{\cdot}97 \times 10^{-3}\,\mathrm{cm}^2$, fabricated on 0·3 Ω cm n-type and 2·8 Ω cm p-type [100] substrates. The dry gate oxides were grown for 3 h at 900°C to a thickness of 35 nm, followed by a 30 min post-oxidation anneal in nitrogen. Some wafers received a post-metallization anneal (PMA) in forming gas for 30 min at 425°C.

Above 50 kHz, the measurement of conductance was entirely conventional and employed an HP4192A impedance analyser. Below 50 kHz, an electrometer op-amp (Analog Devices AD515) was used as a charge-sensitive pre-amplifier with an air-gap capacitor as the feedback capacitor. A block diagram of the experimental set-up is shown in figure 60. A dual-channel spectrum analyser system (HP3565S) provided the bias voltage with a 10 mV excitation superimposed, and measured the phase and amplitude difference between two such pre-amp circuits: a reference circuit employing an air-gap capacitor in place of the sample, and the other circuit containing the MOS capacitor. With careful calibration and compensation for frequency-dependent and sample-capacitance-dependent gain, the system gave a phase resolution of 1 mdegree

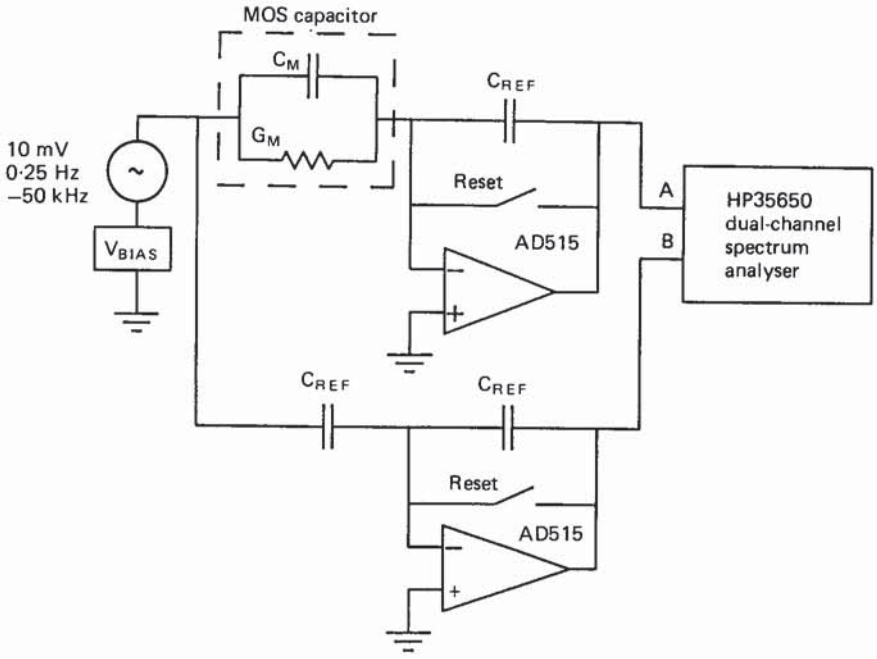

Figure 60. Block diagram of experimental set-up to measure G_P/ω from 0·25 Hz to 50 kHz.

at 1 Hz increasing to about 10 mdegrees at 50 kHz. This phase accuracy was essential to see the effects observed. To compensate for any residual inductances and the substrate series resistance, the measured conductance G_m and capacitance C_m were recorded at all measurement frequencies in strong accumulation and then subtracted from the values found in depletion to give the equivalent parallel conductance G_P of the trap. A guard ring and a nitrogen ambient atmosphere ensured that there was no surface leakage; no low-frequency loss was seen in accumulation and the oxide leakage current was < 5 fA. The surface potential was measured using a quasi-static sweep (Nicollian and Brews 1982).

Figures 61 (*a*)–(*c*) show results for G_P/ω measured against frequency for p- and n-substrate samples without PMA and a p-substrate sample with PMA. The new, striking feature present in all three figures is the presence of the distinct plateau region at low frequencies. Any plateau for the n-substrate annealed samples is around or below the measurement sensitivity (about 10^{-11} S Hz^{-1} cm^{-2}).

The peak in the three traces can be fitted to the standard G_P/ω formula as shown. Interface-state densities D_{it} for the un-annealed samples were typically about 10^{11} cm^{-2} eV^{-1} and for the annealed samples about 2×10^{10} cm^{-2} eV^{-1}. The variance of the surface potential fluctuations was between 1·5 and $3kT$.

The G_P/ω spectrum arising out of a uniform distribution of time constants can be conveniently derived using the formalism in the appendix to Nicollian and Goetzberger (1967). A tunnelling model consistent with the $1/f$ results in which the defects are uniformly distributed in energy and distance into the oxide gives the appropriate distribution. We write $\tau_n = \tau_{0n} \exp(2\kappa\xi)$, where ξ is the distance of the trap from the interface and κ is the decay constant:

$$\kappa = \frac{(8m^*\phi)^{1/2}}{h/2\pi}. \tag{7.15}$$

The barrier energy ϕ was taken to be 3·5 eV and m^* was set equal to the free-electron mass. This model ignores the capture activation energy; but to first order it is a useful approximation. (The effects of the convolution of the cross-section pre-factor and activation energy may be visible in the low-frequency conductance; we comment on this at the end of this section.) Using equation (7.13 *b*) with C_{it} replaced by $qN_t\,d\xi$, where N_t is the number of traps per unit volume per electron-volt in the oxide, we find

$$\frac{G_P}{\omega} = qN_t(2\omega\tau_{0n})^{-1} \int_0^{t_{ox}} \exp(-2\kappa\xi) \ln[1 + \omega^2\tau_{0n}^2 \exp(4\kappa\xi)]\,d\xi, \tag{7.16}$$

where the upper limit on the integral has been set equal to the oxide thickness for convenience. In the limit in which $t_{ox} \to \infty$, equation (7.16) can be simplified to

$$\frac{G_P}{\omega} = \frac{qN_t}{4\kappa}\left[\frac{\ln(1 + \omega^2\tau_{0n}^2)}{\omega\tau_{0n}} + \pi - 2\tan^{-1}\omega\tau_{0n}\right].$$

In the limit in which $\omega \ll 1/\tau_{0n}$, the model predicts a flat spectrum—as observed —and the measured value of G_P/ω is related to the trap density per unit volume via the relation

$$N_t = \frac{4\kappa G_P/\omega}{q\pi}. \tag{7.17}$$

Using equations (7.15) and (7.17) and the measured value of G_P/ω in the plateau region at low frequencies, we find $N_t \approx 2 \times 10^{16}$ cm^{-3} eV^{-1} for the annealed sample and 2×10^{17}–5×10^{17} cm^{-3} eV^{-1} for the un-annealed samples.

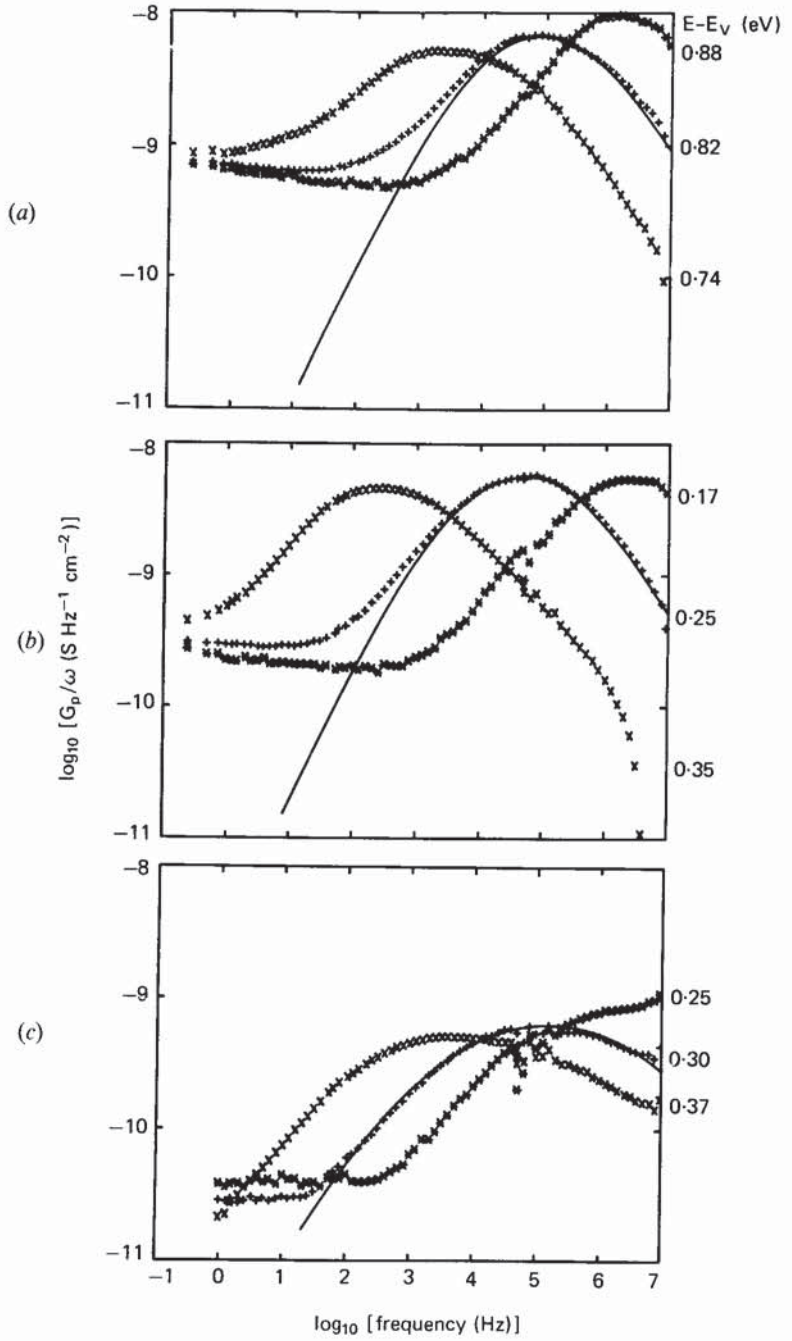

Figure 61. Equivalent parallel conductance G_P/ω against frequency for three gate biases in depletion at room temperature. (*a*) No forming gas PMA, n-substrate. For the fitted curve, interface-state density $D_{it} = 1{\cdot}6 \times 10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$, potential fluctuations $\sigma_s = 1{\cdot}5kT$, cross-section $\sigma = 5 \times 10^{-17}\,\mathrm{cm^2}$. For the low-frequency plateau at 1 Hz, $N_t = 5{\cdot}6 \times 10^{17}\,\mathrm{cm^{-3}\,eV^{-1}}$. (*b*) p-Substrate, no PMA. $D_{it} = 1{\cdot}3 \times 10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$, $\sigma_s = 1{\cdot}6kT$, $\sigma = 1{\cdot}8 \times 10^{-17}\,\mathrm{cm^2}$ and $N_t = 2{\cdot}4 \times 10^{17}\,\mathrm{cm^{-3}\,eV^{-1}}$. (*c*) p-Substrate, 425°C PMA. $D_{it} = 2{\cdot}1 \times 10^{10}\,\mathrm{cm^{-2}\,eV^{-1}}$, $\sigma_s = 2{\cdot}8kT$, $\sigma = 6 \times 10^{-16}\,\mathrm{cm^2}$ and $N_t = 2{\cdot}2 \times 10^{16}\,\mathrm{cm^{-3}\,eV^{-1}}$. From Uren *et al.* (1989a).

Our working hypothesis at this point is that the defect states responsible for the plateaux in G_P/ω shown in figures 61 (*a*)–(*c*) are also responsible for the measured $1/f$ spectrum in MOSFETs. To complete the argument, ideally one requires MOSFETs and MOS capacitors fabricated at the same time in the same process in order that the magnitude of the noise can be correlated with the magnitude of the plateau in G_P/ω. It must be borne in mind that in order to access the upper half of the silicon band-gap n-channel (p-substrate) MOSFETs are required to compare with n-substrate capacitors. Unfortunately, we do not have such a set of samples. We must therefore compare our values of N_t from G_P/ω with those that are measured from the noise in typical modern devices. Reimbold (1984) produced a simple trapping model of $1/f$ noise that allows N_t to be estimated from the magnitude of the power spectrum in both strong and weak inversion (which would correspond to accumulation and depletion for the capacitors). For the n-channel devices used in his study, he found values for N_t from 2×10^{15} to $2 \times 10^{16}\,\mathrm{cm^{-3}\,eV^{-1}}$. Similarly, our noise measurements shown in figure 53 gave $N_t \approx 10^{16}\,\mathrm{cm^{-3}\,eV^{-1}}$ in weak inversion. Our G_P/ω measurements have a resolution that corresponds at best to about $5 \times 10^{15}\,\mathrm{cm^{-3}\,eV^{-1}}$; so it is not surprising that we have not been able to see conclusively such a plateau for the n-substrate samples with PMA, although the plateau is quite clear when there is no anneal. For the valence-band-edge case we have no comparative MOS noise figures, since most PMOS devices are partly buried-channel owing to the threshold implant. But it is significant that the p-substrate capacitors with PMA have values of N_t comparable to those seen in n-channel MOSFETs. Such comparisons are of limited value because of the different gate material (aluminium *versus* polysilicon) and oxide growth conditions, but do serve to show that the values of N_t measured from G_P/ω are quite consistent with those derived from noise.

We therefore conclude that defects associated with the oxide/silicon interface can be divided into two distinct sets. The first incorporates the so-called interface states D_{it}, with cross-sections of about $10^{-16}\,\mathrm{cm^2}$ (Deal 1980). These states are in electrical communication with the inversion layer and are responsible for most of the stretch-out in C–V measurements and the loss peak in conductance data. The second set is characterized by cross-sections less than about $10^{-16}\,\mathrm{cm^2}$ with no measured lower bound. These defects are responsible for $1/f$ noise and random telegraph signals and are due to defect states in the oxide. Their density is typically an order of magnitude lower than the D_{it} states. In figure 62 we show a five-parameter fit to the measured G_P/ω loss over seven decades in frequency. The experimental data have been fitted with a D_{it} term and a background term corresponding to the states distributed into the oxide. A very satisfactory fit to the model of two sets of defects is obtained.

Referring back to figure 54 (*d*), we see that the multiphonon model of capture into oxide states predicts a rising edge to the distribution of time constants. Some evidence for this effect can be seen at low frequencies in figures 61 (*a*) and (*b*), where the measured loss starts to rise rather than just levelling off.

The origin of the D_{it} and oxide states remains an open question. The physics and chemistry of the Si/SiO_2 interface have received a great deal of attention over the years. The interested reader is referred to the conference proceedings edited by Devine (1988), Helms and Deal (1989), the review by Grunthaner and Grunthaner (1986) and the series of reviews by Poindexter (1989). There is strong evidence from electron paramagnetic resonance measurements on (111) interfaces that one type of interface

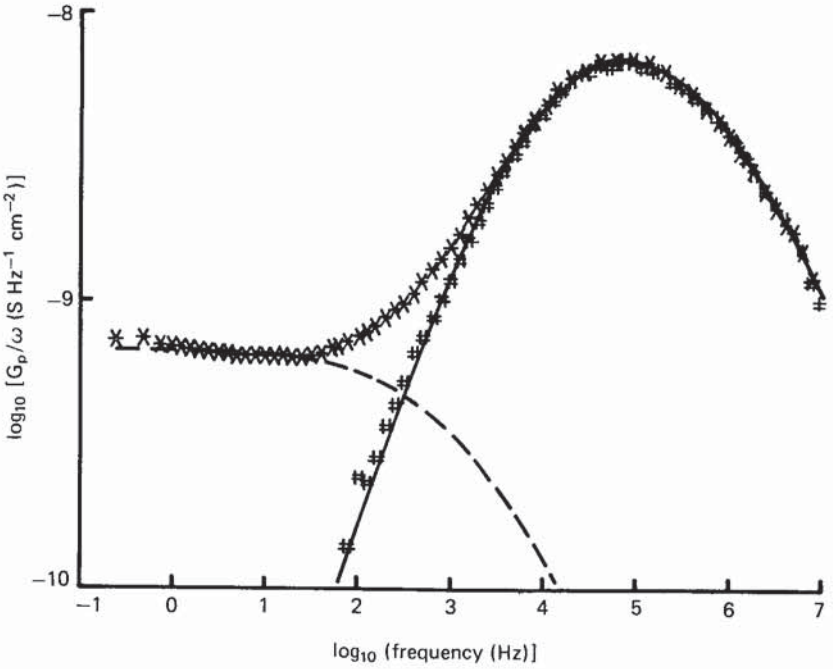

Figure 62. Equivalent parallel conductance G_P/ω against frequency for n-substrate capacitor in depletion. The stars depict the experimental data. The theoretical behaviour of G_P/ω for the oxide traps alone is shown as the broken line. The fit of equation (7.14) to the peak is the continuous line. The symbols show the behaviour of the experimental data minus the theoretical background. The figure therefore provides strong evidence that the conductance can be modelled by a set of interface traps and a different set of traps distributed into the oxide. Figure courtesy of S. Collins.

state corresponds to an unsaturated silicon dangling bond (Poindexter and Caplan 1983, Poindexter *et al.* 1984, Brower 1983, Johnson *et al.* 1983). As yet, there is no model for the physical and chemical origin of the oxide states. By extending the dynamic frequency range of G–ω measurements down to frequencies of about 0·25 Hz, we have opened up the exciting possibility of being able to monitor the effects of different oxide treatments, hot-electron injection, and so on, on the oxide states and the interface states at the same time.

8. Concluding remarks

Here we wish to tie together the major themes running through this work. There can now be no doubt that measurements of noise and RTSs in microstructures have shown definitively that $1/f$ noise in MOSFETs and MIM tunnel diodes is generated through carrier trapping. Investigations of RTS behaviour in MOSFETs as a function of gate voltage and temperature have shown that carrier capture into individual defects in the oxide, which reside close to the Si/SiO_2 interface, is thermally activated, demonstrating the presence of strong electron–lattice coupling. Cross-sections, activation energies and entropies of ionization have been measured for a number of individual defects. The multiphonon capture model gives a consistent picture of the magnitude of the low-frequency noise and the wide distribution of time constants

implicated in its production. Furthermore, the insights provided by the study of small MOSFETs has lead to a realization that there must be two classes of Si/SiO_2 interface state. The first includes the D_{it} states responsible for the usual loss peak in conductance measurements. These states reside at the interface and are probably due to some form of unsaturated dangling bond. The second class incorporates defect states residing in the oxide, which are nevertheless still in electrical communication with the inversion layer. These oxide states are responsible for $1/f$ noise and RTSs. This classification was confirmed in enhanced conductance measurements on MOS capacitors, which showed a loss peak due to the D_{it} states and a low-frequency loss plateau due to the trapping centres in the oxide.

The two outstanding problems in the switching observed in microstructures are the complexity of the signals sometimes observed and the magnitude of the RTS step height. Complex switching has been observed in many systems including MOSFETs, MOS tunnel diodes and metal nanobridges. It is difficult to provide clear proof of the underlying mechanism, but individual metastable defects provide a plausible explanation for some of the anomalous RTSs observed in MOSFETs and MIM diodes. Single-electron trapping is able to account for the average RTS amplitude observed in MOSFETs. However, a very wide range of RTS step heights is observed, and the details of the mechanisms whereby a trapped charge carrier modulates the channel conductivity still remain unclear. Multi-electron trapping would seem to be inappropriate to the silicon MOSFET, but this model requires much more thorough study for other microstructures.

Acknowledgements

We should like to thank R. Lambert and S. Partridge of the GEC Hirst Research Centre and Dr O. Jantsch of Siemens Munich for the small MOSFETs on which our own work was based. It is a pleasure also to thank the staff of the silicon-processing laboratory at RSRE for the fabrication of the MOS capacitors used in our conductance studies. During the course of this work we have benefited from the assistance of M. Britcher, B. A. Kerr and C. E. J. Kilgour. We are grateful to the following for stimulating discussions: M. O. Andersson, Professor O. Engstrom, Dr M. Bollu, D. Cobden, Dr S. Collins, Dr D. J. Day, Dr O. Jantsch, Dr K. Kandiah, A. Karwath, Dr K. Knott and Professor M. Schulz. We should also like to express our gratitude to those authors who gave permission to reproduce previously published figures. Finally, we should like to acknowledge Drs G. R. Jones, K. G. Barraclough and D. J. Marshall of RSRE for providing the environment in which our work was undertaken and this article written.

References

ANDERSON, P. W., 1975, *Phys. Rev. Lett.*, **34,** 953.
ANDERSON, P. W., HALPERIN, B. I., and VARMA, C. M., 1972, *Phil. Mag.*, **25,** 1.
ANDERSSON, M. O., and ENGSTROM, O., 1989, *Appl. Surface Sci.* (to be published).
ANDO, T., FOWLER, A. B., and STERN, F., 1982, *Rev. mod. Phys.*, **54,** 437.
BARAFF, G. A., KANE, E. O., and SCHLÜTER, M., 1979, *Phys. Rev. Lett.*, **43,** 956; 1980, *Phys. Rev.* B, **21,** 3563.
BEUTLER, D. E., MEISENHEIMER, T. L., and GIORDANO, N., 1987, *Phys. Rev. Lett.*, **58,** 1240.
BINNIG, G., and ROHRER, H., 1986, *IBM J. Res. Dev.*, **30,** 355.
BIRGE, N. O., GOLDING, B., and HAEMMERLE, W. H., 1989, *Phys. Rev. Lett.*, **62,** 195.
BOLLU, M., KOCH, F., MADENACH, A., and SCHOLZ, J., 1987, *Appl. Surface Sci.*, **30,** 142.
BOURGOIN, J., and LANNOO, M., 1983, *Point Defects in Semiconductors II* (Berlin: Springer).
BREWS, J. R., 1975a, *J. appl. Phys.*, **46,** 2181; 1975b, *J. appl. Phys.*, **46,** 2193; 1978, *Solid-St. Electron.*, **21,** 345.

BROOKS, H., 1955, *Adv. Electron. Electron Phys.*, **7,** 85.
BROWER, K. L., 1983, *Appl. Phys. Lett.*, **43,** 1111.
BUCKINGHAM, M. J., 1983, *Noise in Electronic Devices and Systems* (Chichester: Ellis Horwood).
DEAL, B. E., 1980, *IEEE Trans. Electron. Devices*, **27,** 606.
DEVINE, R. A. B. (editor), 1988, *The Physics and Technology of Amorphous SiO_2* (New York: Plenum).
DUTTA, P., and HORN, M., 1981, *Rev. mod. Phys.*, **53,** 497.
EATON, D. H., and SAH, C. T., 1972, *Phys. Stat. sol.* (a), **12,** 95.
ENGSTROM, O., and ALM, A., 1983, *J. appl. Phys.*, **54,** 5240.
ENGSTROM, O., and GRIMMEISS, H. G., 1989, *Semicond. Sci. Technol.* (to be published).
FARMER, K. R., ROGERS, C. T., and BUHRMAN, R. A., 1987, *Phys. Rev. Lett.*, **58,** 2255.
FARMER, K. R., SALETTI, R., and BUHRMAN, R. A., 1988, *Appl. Phys. Lett.*, **52,** 1749.
FENG, S., LEE, P. A., and STONE, A. D., 1986, *Phys. Rev. Lett.*, **56,** 1960.
FLEETWOOD, D. M., and GIORDANO, N., 1985, *Phys. Rev.* B, **31,** 1157.
GREEN, M. A., KING, F. D., and SHEWCHUN, J., 1974, *Solid-St. Electron.*, **17,** 551.
GRUNTHANER, F. J., and GRUNTHANER, P. J., 1986, *Mater. Sci. Rep.*, **1,** 65.
GUTTMAN, L., and RAHMAN, S. M., 1986, *Phys. Rev.* B, **33,** 1506.
HEIMAN, F. P., and WARFIELD, G., 1965, *IEEE Trans. Electron Devices*, **12,** 167.
HEINE, V., and VAN VECHTEN, J. A., 1976, *Phys. Rev.* B, **13,** 1622.
HELMS, C. R., and DEAL, B. E. (editors), 1989, *The Physics and Chemistry of SiO_2 and the Si : SiO_2 Interface* (New York: Plenum).
HENRY, C. H., and LANG, D. V., 1977, *Phys. Rev.* B, **15,** 989.
HOOGE, F. N., KLEINPENNING, T. G. M., and VANDAMME, L. K. J., 1981, *Rep. Prog. Phys.*, **44,** 479.
JACKEL, L. D., SKOCPOL, W. J., HOWARD, R. E., FETTER, L. A., EPWORTH, R. W., and TENNANT, D. M., 1985, *Proceedings of the 17th International Conference on Physics of Semiconductors*, edited by D. J. Chadi and W. A. Harrison, (New York: Springer), p. 221.
JANTSCH, O., and KIRCHER, R., 1989, *The Physics and Chemistry of SiO_2 and the Si : SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (New York: Plenum), p. 349.
JOHNSON, N. M., BIEGELSEN, D. K., MOYER, M. D., CHANG, S. T., POINDEXTER, E. H., and CAPLAN, P. J., 1983, *Appl. Phys. Lett.*, **43,** 563.
JUDD, T., CROUCH, N. R., BETON, M. J., KELLY, M. J., and PEPPER, M., 1986, *Appl. Phys. Lett.*, **49,** 1652.
KANDIAH, K., and WHITING, F. B., 1978, *Solid-St. Electron*, **21,** 1079.
KANDIAH, K., DEIGHTON, M. O., and WHITING, F. B., 1981, *Proceedings of the Sixth Conference on Noise in Physical Systems*, edited by P. H. E. Meijer, R. H. Mountain and R. J. Soulen (NBS Publication 614, US Department of Commerce), p. 75.
KARWATH, A., and SCHULZ, M., 1988, *Appl. Phys. Lett.*, **52,** 634; 1989, *The Physics and Chemistry of SiO_2 and the Si : SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (New York: Plenum), p. 327.
KIRTON, M. J., and UREN, M. J., 1986, *Appl. Phys. Lett.*, **48,** 1270.
KIRTON, M. J., UREN, M. J., and COLLINS, S., 1987, *Appl. Surface Sci.*, **30,** 148; 1988, *The Physics and Technology of Amorphous SiO_2*, edited by R. A. B. Devine (New York: Plenum), p. 267; 1989a *The Physics and Chemistry of SiO_2 and the Si : SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (New York: Plenum), p. 341.
KIRTON, M. J., UREN, M. J., COLLINS, S., SCHULZ, M., KARMANN, A., and SCHEFFER, K., 1989b *Semicond. Sci. Technol.* (to be published).
KITTEL, C., and KROEMER, H., 1980, *Thermal Physics*, second edition (San Francisco: Freeman).
KNOTT, K., 1978, *Solid-St. Electron.*, **21,** 1039; 1980, *Solid-St. Electron.*, **23,** 727.
KOCH, R. H., 1987, *Bull. Am. phys. Soc.*, **32,** 394.
KOCH, R. H., LLOYD, J. R., and CRONIN, J., 1985, *Phys. Rev. Lett.*, **55,** 2487.
KOGAN, SH. M., and NAGAEV, K. E., 1982, *Soviet Phys. Solid State*, **24,** 1921.
KOUSIK, G. S., VAN VLIET, C. M., BOSMAN, G., and HANDEL, P. H., 1985, *Adv. Phys.*, **34,** 663.
LEE, P. A., and STONE, A. D., 1985, *Phys. Rev. Lett.*, **55,** 1622.
LANDAUER, R., 1957, *IBM J. Res. Dev.*, **1,** 223; 1975, *Z. Phys.* B, **21,** 247.
MACDONALD, D. K. C., 1962, *Noise and Fluctuations: An Introduction* (New York: Wiley).
MCWHORTER, A. L., 1957, *Semiconductor Surface Physics*, edited by R. H. Kingston (Philadelphia: University of Pennsylvania), p. 207.
MACHLUP, S., 1954, *J. appl. Phys.*, **25,** 341.

MARTIN, J. W., 1971, *Phil. Mag.*, **24,** 555; 1972, *J. Phys.* F, **2,** 842.
MULS, P. A., DECLERCK, G. J., and VAN OVERSTRAETEN, R. J., 1978, *Adv. Electron. Electron Phys.*, **47,** 197.
NELKIN, M., and TREMBLAY, A.-M. S., 1981, *J. statist. Phys.*, **25,** 253.
NERI, B., OLIVO, P., and RICCO, B., 1987, *Appl. Phys. Lett.*, **51,** 2167.
NGAI, K. L., and LIU, S. T., 1982, *Thin Solid Films*, **93,** 321.
NGAI, K. L., and WHITE, C. T., 1981, *J. appl. Phys.*, **52,** 320.
NICOLLIAN, E. H., and BREWS, J. R., 1982, *MOS (Metal Oxide Semiconductor) Physics and Technology* (New York: Wiley).
NICOLLIAN, E. H., and GOETZBERGER, A., 1967, *Bell Syst. tech. J.*, **46,** 1055.
PAO, H. C., and SAH, C. T., 1965, *IEEE Trans. Electron Devices*, **12,** 139.
PELZ, J., and CLARKE, J., 1985, *Phys. Rev. Lett.*, **55,** 738; 1987, *Phys. Rev.*, B, **36,** 4479.
PHILLIPS, W. A., 1972, *J. low. Temp. Phys.*, **7,** 351.
POINDEXTER, E. H. (editor), 1989, *Semicond. Sci. Technol.* Special Issue on MOS Interface States.
POINDEXTER, E. H., and CAPLAN, P. J., 1983, *Prog. Surface Sci.*, **14,** 201.
POINDEXTER, E. H., GERARDI, G. J., RUECKEL, M.-E., CAPLAN, P. J., JOHNSON, N. M., and BIEGELSEN, D. K., 1984, *J. appl. Phys.*, **56,** 2844.
PRESS, W. H., 1978, *Comments Astrophys. Space Phys.*, **7,** 103.
PRIER, H., 1967, *Appl. Phys. Lett.*, **10,** 361.
RALLS, K. S., and BUHRMAN, R. A., 1988, *Phys. Rev. Lett.*, **60,** 2434.
RALLS, K. S., SKOCPOL, W. J., JACKEL, L. D., HOWARD, R. E., FETTER, L. A., EPWORTH, R. W., and TENNANT, D. M., 1984, *Phys. Rev. Lett.*, **52,** 228.
REIMBOLD, G., 1984, *IEEE Trans. Electron Devices*, **31,** 1190.
RESTLE, P., 1988, *Appl Phys. Lett.*, **53,** 1862.
RESTLE, P. J., HAMILTON, R. J., WEISSMAN, M. B., and LOVE, M. S., 1985, *Phys. Rev.* B, **31,** 2254.
RESTLE, P. J., WEISSMAN, M. B., GARFUNKEL, G. A., PEARAH, P., and MORKOÇ, H., 1986, *Phys. Rev.* B, **34,** 4419.
RIDLEY, B. K., 1978, *J. Phys.* C, **11,** 2323.
ROGERS, C. T., and BUHRMAN, R. A., 1984, *Phys. Rev. Lett.*, **53,** 1272; 1985, *Phys. Rev. Lett.*, **55,** 859.
SCHMIDLIN, F. W., 1966, *J. appl. Phys.*, **37,** 2823.
SCHULZ, M., 1983, *Surface Sci.*, **132,** 422.
SCHULZ, M., and JOHNSON, N. M., 1978, *Solid St. Commun.*, **25,** 481.
SHEWCHUN, J., GREEN, M. A., and KING, F. D., 1974, *Solid-St. Electron.*, **17,** 563.
SKOCPOL, W. J., 1987, *Science and Technology of Microfabrication; Materials Research Society Symposium Proceedings*, Vol. 76, edited by R. E. Howard, E. L. Hu, S. Pang and S. Namba (Pittsburg: Materials Research Society), p. 3.
SKOCPOL, W. J., MANKIEWICH, P. M., HOWARD, R. E., JACKEL, L. D., TENNANT, D. M., and STONE, A. D., 1986, *Phys. Rev. Lett.*, **56,** 2865.
STERN, F., and HOWARD, W. E., 1967, *Phys. Rev.*, **163,** 816.
STONEHAM, A. M., 1975, *Theory of Defects in Solids* (Oxford: Clarendon).
SZE, S., 1981, *Physics of Semiconductor Devices* (New York: Wiley).
UREN, M. J., COLLINS, S., and KIRTON, M. J., 1989b, *Appl. Phys. Lett.* **54,** 1448.
UREN, M. J., DAY, D. J., and KIRTON, M. J., 1985, *Appl. Phys. Lett.*, **47,** 1195.
UREN, M. J., KIRTON, M. J., and COLLINS, S., 1988, *Phys. Rev.* B, **37,** 8346; 1989a, *The Physics and Chemistry of SiO_2 and the Si: SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (New York: Plenum), p. 335.
VAN DER ZIEL, A., 1979, *Adv. Electron. Electron Phys.*, **49,** 225.
VAN VECHTEN, J. A., and THURMOND, C. D., 1976, *Phys. Rev.* B, **14,** 3539.
WELLAND, M. E., and KOCH, R. H., 1986, *Appl. Phys. Lett.*, **48,** 724.
WEISSMAN, M. B., 1988, *Rev. mod. Phys.*, **60,** 537.
WOLF, D., and HOLLER, E., 1967, *J. appl. Phys.*, **38,** 189.