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Control of the Interfacial Layer Thickness in Hafnium Oxide Gate Dielectric Grown by PECVD

Kyu-Jeong Choi, Jong-Bong Park, and Soon-Gil Yoon[z]

Department of Materials Engineering, Chungnam National University, 305-764 Daejon, Korea

The HfO_2 thin films for use in gate dielectric applications were deposited at 300°C onto p-type Si(100) substrates using $Hf[OC(CH_3)_3]_4$ as the precursor in the absence of oxygen by plasma-enhanced chemical vapor deposition (PECVD). The HfO_2 films deposited in the absence of O_2 show excellent electrical properties such as low equivalent oxide thickness (EOT) and good thermal stability. The deposited films have an interfacial layer of approximately 10 Å in thickness, resulting in a decrease in the thickness of the interfacial layer by about 50% compared to films deposited in the presence of oxygen. The leakage current density of HfO_2 films was approximately four orders of magnitude lower than an electrically comparable SiO_2 at the same EOT. The improvement of electrical properties can be attributed to the decrease in the SiO_2 interfacial layer. The thickness of the interfacial layer can be controlled by deposition in the absence of oxygen after evacuation of the reaction chamber by means of an ultrahigh vacuum.
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Considerable interest has developed in the replacement of dielectrics for use SiO_2 in metal-oxide-semiconductor (MOS) devices in which the channel lengths are less than 100 nm. The intent is to phase out conventional SiO_2 and oxynitrides due to excessive leakage current and reliability concerns. Alternative gate insulators with a higher electrical permittivity than SiO_2 are currently under widespread investigation for use in future generations of MOS transistors. Thus, high dielectric constant thin films offer the potential of increased capacitance in physically thicker films, thus providing a possible way to reduce direct tunneling.[1] Due to their thermodynamic stability, when in contact with silicon, HfO_2 and its silicates have attracted considerable attention recently.[2-4] In addition, HfO_2 is compatible with a polysilicon gate without any barrier materials.[5,6]

Thus far, HfO_2 thin films have been prepared by sputtering[3,6] as well as thermal chemical vapor deposition (CVD).[5] The thermal CVD method has been reported to be successful in producing usable HfO_2 thin films at temperatures above 500°C using $Hf[OC(CH_3)_3]_4$ and O_2. A lower deposition temperature for processing the HfO_2 thin films is necessary in order to avoid the formation of SiO_2 at the HfO_2/Si interface. Compared with thermal CVD, the plasma-enhanced chemical vapor deposition (PECVD) technique has the advantage of deposition at as low temperatures a possible. However, an amorphous interfacial layer having a thickness of about 20 Å was formed at the HfO_2/Si interface because, at the initial stage of deposition, the Si substrate was exposed to an O_2 ambient.[7] Another route to decrease the thickness of SiO_2 is to deposit HfO_2 films in the absence of O_2 after evacuating the chamber using an ultrahigh vacuum (10^{-6} Torr) because the $Hf[OC(CH_3)_3]_4$ precursor itself contains the necessary oxygen to form HfO_2. Such a method has the potential for controlling interfacial layer thickness during the deposition of HfO_2 thin films.

In this study, a hafnium oxide gate dielectric was deposited at 300°C using PECVD in the absence of O_2 after evacuating the chamber using an ultrahigh vacuum (10^{-6} Torr). The electrical properties of the Pt/HfO_2/Si capacitors were found to be improved as a result of controlling the interfacial layer thickness of the HfO_2/Si structures.

Experimental

After standard cleaning of p-type Si(100) wafers (6-9 Ω cm resistivity), HfO_2 films were deposited by PECVD using hafnium tertiary-butoxide ($Hf[OC(CH_3)_3]_4$, Techno Semichem Co., Ltd.) as the precursor in the absence of O_2. The reaction chamber before HfO_2 deposition was evacuated (10^{-6} Torr) using a diffusion pump in order to remove the residual oxygen in the chamber because its presence leads to the oxidation of the silicon surface at a deposition temperature of 300°C. In order to avoid the damage at the Si/HfO_2 interface by plasma, thermal deposition of HfO_2 without plasma was performed at the initial stage (around 1 min) and then deposition by plasma was performed after 1 min. The deposition conditions were performed at a temperature of 300°C, a pressure of 0.5 Torr, and an rf power of 40 W. The precursor was vaporized in a bubbler maintained at 30°C and was carried to the reactor using argon (purity 99.9999%) as the carrier gas. The Pt top electrodes for measurement of the electrical properties were patterned using lift-off lithography. The capacitor area for the MOS (Pt/HfO_2/Si) structure was 2×10^{-5} cm^2. After patterning the electrode, the samples were annealed at various temperatures ranging from 600 to 900°C in N_2 (purity 99.9999%) for 60 s. The physical thickness of the HfO_2 thin film was measured using high-resolution transmission electron microscopy (TEM, CM20T/STEM, Philips). The composition of HfO_2 films was determined by Rutherford backscattering spectroscopy (RBS, NEC 3SDH, 2.240 MeV $4He^{++}$). The capacitance-voltage (C-V) and current-voltage (I-V) were measured using an HP4194A impedance/gain-phase analyzer and an HP4145B semiconductor parameter analyzer, respectively.

Results and Discussion

Figure 1 shows the variation of interface trap density as a function of applied voltage in order to confirm the effect of Ar plasma damage on HfO_2 thin film growth. As shown in Fig. 1, thin films prepared by process 3 showed the lowest interface trap density compared with those by processes 1 and 2. These results suggested that the deposition (process 3) performed in this study effectively alleviated the plasma damage in Si/HfO_2 interface.

Figure 2 shows the variation of the equivalent oxide thickness (EOT) of HfO_2 films as a function of leakage current density, as measured at -1 V. The relationship between EOT and the leakage current of the SiO_2 films is also shown as a comparison with the HfO_2 films (solid square).[8] The leakage current density of the HfO_2 films deposited in the presence of O_2 varied with a tendency similar to that of SiO_2 and was approximately one order of magnitude lower than SiO_2 at the same EOT. This suggests that interfacial layers above 20 Å in thickness were formed at the HfO_2/Si interface and that they play an important role in the characteristics of the leakage current of Pt/HfO_2/Si capacitors. The leakage current density of HfO_2 films deposited in the absence of O_2 is approximately four orders of magnitude lower than SiO_2 at the same EOT.

[z] E-mail: sgyoon@cnu.ac.kr

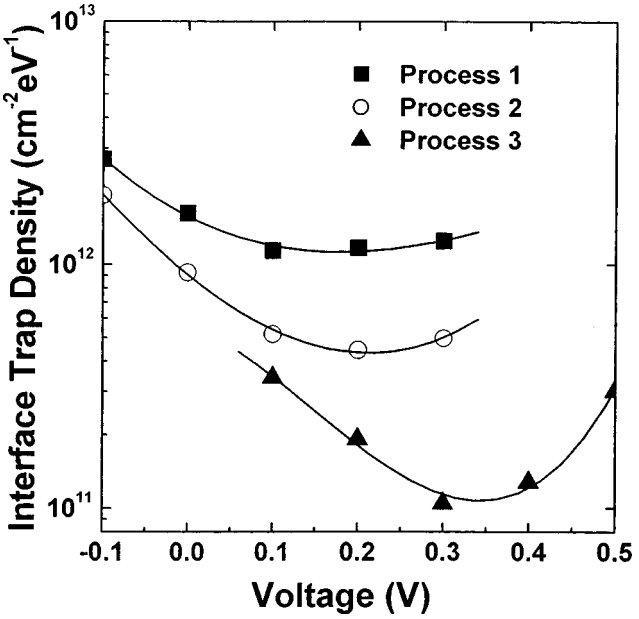

Figure 1. Interface trap densities of Pt/HfO_2/Si capacitors as a function of applied voltage. Process 1, keeping Si substrate in Ar plasma ambient for 1 min→HfO_2 deposition for 6 min in Ar plasma ambient. Process 2, thermal deposition (without plasma) of HfO_2 for 1 min→making vacuum ambient→keeping 1 min in Ar plasma→HfO_2 deposition for 5 min in Ar plasma. Process 3, thermal deposition of HfO_2 for 1 min→HfO_2 deposition for 5 min in Ar plasma ambient.

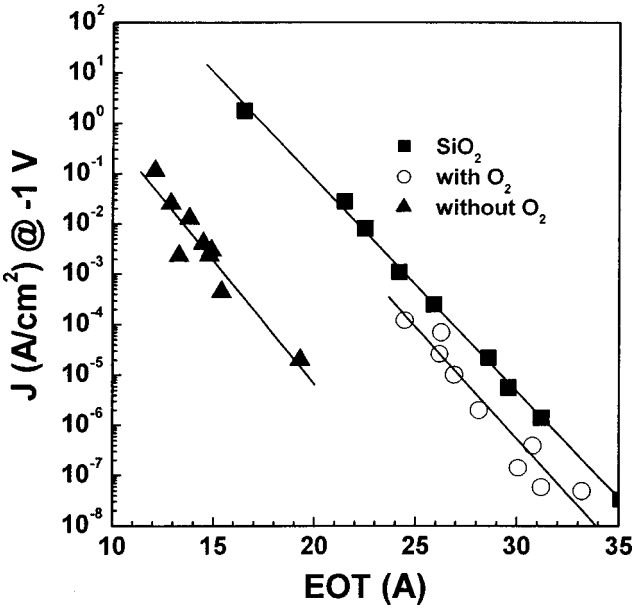

Figure 2. Leakage current density of Pt/HfO_2/Si capacitors as a function of EOT. HfO_2 films deposited in the presence of and absence of O_2 are compared with SiO_2.

The HRTEM images of as-deposited and annealed Pt/HfO_2/Si samples at 900°C for 60 s in a nitrogen ambient are shown in Fig. 3. Figure 3c shows the image of a HfO_2/Si structure annealed at the same condition without a top Pt. As shown in Fig. 3a and b, the total physical thickness of as-deposited and annealed films was approximately 45 and 42 Å, respectively. Even though the thickness of the interfacial layer is not clear because of the reaction between Hf, O, and Si, the 10 Å thick interfacial layers in the as-deposited films increased by approximately 13 Å as the result of annealing at 900°C in the nitrogen ambient. The annealed HfO_2 films showed a decrease in thickness because of their more dense crystalline nature. The densification of pure oxide materials is dependent on the complete removal of oxygen vacancies if volatile elements are absent in the bulk materials. The HfO_2 films shown in Fig. 3c showed a higher crystallinity than that of the films shown in Fig. 3b. The interfacial layer thickness of the HfO_2/Si structure (shown in Fig. 3c) increases more than that of the Pt/HfO_2/Si structure because the top Pt layer suppresses the diffusion of oxygen into the SiO_2 layer in a nitrogen ambient anneal. Any annealing treatments which have an excess of oxygen present will lead to the rapid diffusion of oxygen through the oxides, resulting in SiO or SiO_2-containing interface layers.[9] When Fig. 3b is compared with Fig. 3c, the interfacial layer thickness by oxygen contained in the nitrogen can be reduced by the deposition of the Pt top electrode before the annealing of HfO_2 films.

Figure 4 shows the frequency dependence on the *C-V* characteristics of Pt/HfO_2/Si structures annealed at 900°C for 60 s in a N_2 ambient. The Pt/HfO_2/Si structures show clear accumulation, depletion, and inversion regions. The EOT values were extracted from the accumulation capacitance of 1 MHz *C-V* curves and include the quantum mechanical deduction using the North Carolina State University CVC program.[10] The EOT and the effective dielectric constant of the Pt/HfO_2/Si capacitors annealed at 900°C were approximately 14.8 Å and 11.1, respectively. A slight frequency dependent hump of capacitance near 0 V was observed in the capacitance-voltage relationship measured at 100 kHz, consistent with originating from interface traps.[11] The inset in Fig. 4 shows the relationship between the flatband voltage and hysteresis of Pt/HfO_2/Si capacitors for various film thicknesses as a function of annealing temperature for 60 s in N_2 ambient. The flatband voltage (V_{FB}) was determined from the intercept of the $1/C^2$ *vs. V* plot.[12] The V_{FB} slightly decreased with increasing annealing temperature irrespective of film thickness. As-deposited HfO_{2+x} ($x = 0.2$, approximately) films containing an excessive oxygen from RBS analysis preserve the negative charges and then produce a shift in the value of V_{FB} toward a positive voltage. The excessive oxygen decreased with an increase of annealing temperature in a N_2 ambient (approximately $P_{O_2} \approx 10^{-3}$ Torr) and the decrease in negative charges shifted the V_{FB}

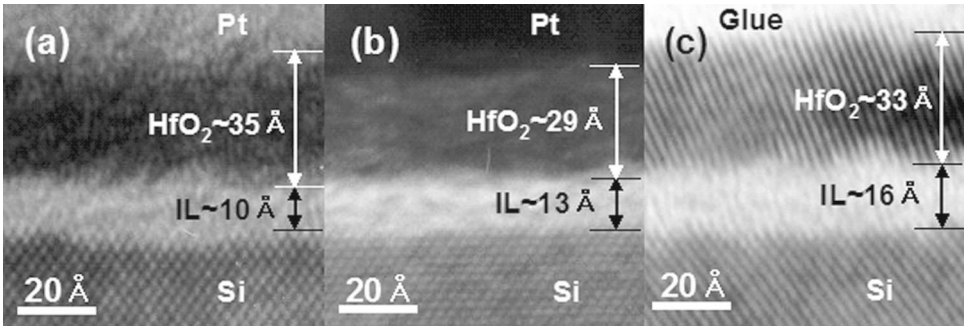

Figure 3. Cross-sectional HRTEM images of (a) as-deposited and (b) annealed Pt/HfO_2/Si capacitors, (c) annealed HfO_2/Si structures at 900°C in N_2 for 60 s.

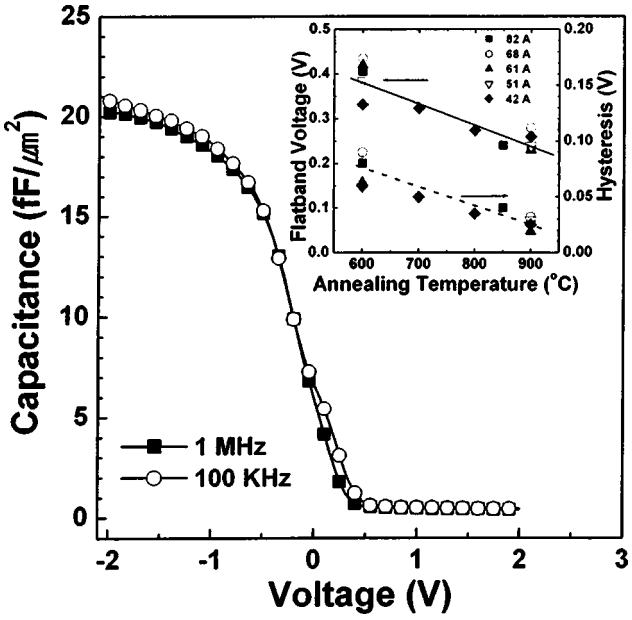

Figure 4. Capacitance *vs.* voltage characteristics of $Pt/HfO_2/Si$ capacitors annealed at 900°C in a N_2 ambient for 60 s. Inset shows the relationship between flatband voltage and hysteresis as a function of annealing temperature at 1 MHz.

toward a negative gate voltage, resulting in a decrease in flatband voltage with increasing annealing temperature in the N_2 ambient. The hysteresis due to charge trapping was reduced with increasing annealing temperature and, in samples annealed at 900°C was reduced to a negligible level of about 25 mV. This result is comparable to that of HfO_2 films deposited by reactive dc magnetron sputtering.[13]

Figure 5 shows the relationship between the EOT and the leakage current density of $Pt/HfO_2/Si$ capacitors annealed at various temperatures in N_2 for 60 s. The electrical properties of HfO_2 films deposited in the absence of oxygen were compared with those of films deposited in the presence of oxygen. The EOT and leakage current of films deposited in the presence of oxygen showed a reverse tendency, as compared with those in the absence of oxygen. The thickness of the SiO_2 interfacial layer in films annealed at 800°C in a N_2 ambient did not change with respect to that of films as-deposited with oxygen gas because the SiO_2 layer is sufficient to resist the penetration of oxygen. The decrease in thickness of HfO_2 films irrespective of an SiO_2 interfacial layer thickness plays a critical role in the decrease in EOT with increasing annealing temperature. On the other hand, the EOT of HfO_2 thin films deposited in the absence of oxygen increased with increasing annealing temperature in the N_2 ambient. The reason for this is that the SiO_2 interfacial layer rather than the HfO_2 films increased with increasing annealing temperature as shown in Fig. 3. The decrease of leakage current densities with annealing temperature in HfO_2 films deposited in the absence of oxygen can be attributed to the increase in the SiO_2 interfacial layer rather than an increase in leakage current by crystallization of the HfO_2 thin films. On the other hand, the leakage currents of HfO_2 thin films deposited in the presence of oxygen were governed by the crystallization of the HfO_2 films since the thickness of SiO_2 interfacial layers remained unchanged for increasing annealing temperatures in the N_2 ambient, resulting in an increase in leakage current with increasing annealing temperature.

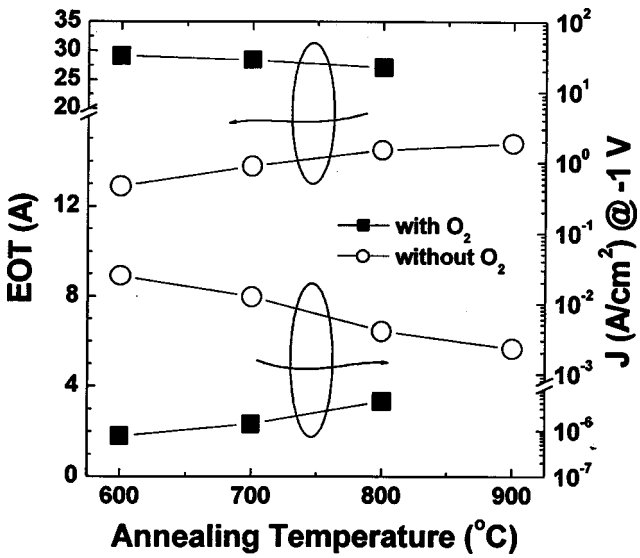

Figure 5. The EOT *vs.* leakage current density of $Pt/HfO_2/Si$ capacitors as a function of annealing temperature in a N_2 ambient.

Conclusions

Hafnium oxide thin films for use as gate dielectrics were deposited at 300°C on p-type Si(100) substrates using $Hf[OC(CH_3)_3]_4$ as the precursor in the absence of oxygen by plasma-enhanced chemical vapor deposition. Compared with HfO_2 films deposited in the presence of O_2, the films deposited in the absence of O_2 show excellent electrical properties including low capacitance equivalent oxide thickness and good thermal stability. The HfO_2 films deposited in the absence of O_2 have an interfacial layer of approximately 10 Å in thickness, resulting in a decrease in the thickness of the interfacial layer by about 50% compared to films deposited in the presence of oxygen. The leakage current density of HfO_2 films deposited in the absence of O_2 is approximately four orders of magnitude lower than that of SiO_2 for the same EOT.

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