Materials Science Forum Vols. 264-268 (1998) pp. 901-906

Vital Issues for SiC Power Devices

K. Hara

Research Laboratories, Denso Corporation,
500-1 Minamiyama, Komenoki-cho, Nisshin, Aichi 470-01, Japan

Keywords: Power EC-FET, Epi-Layer Channel, Accumulation-Mode, Specific On-Resistance, Avalanche Breakdown, Micropipe Defects, Comet-Tail Defects

Abstract: This paper provides an overview of SiC technology and identifies the vital issues for MOS based SiC power devices, specially for power MOSFETs. The major problems arise from the immaturity of device fabrication processes and crystal growth technology. To address technical difficulties, a new transistor named the epi-channel (EC)-FET was developed for power switching applications. Anisotropy in thermal oxidation and epitaxial growth of SiC was utilized to develop the EC-FET. 4H-SiC power EC-FETs have been demonstrated to have a specific on-resistance as low as $10.9 m\Omega.cm^2$ at room temperature with blocking voltage of more than 450V, surpassing the limits of Si power devices. However, the fabricated large area power devices show large leakage currents and low blocking voltage at the crystal defects. The wafer size and defect density together with epi-layer quality are the key factors for the commercial success of the SiC technology.

1. Introduction

SiC power device applications are based on its one order higher critical electric field compared to Si which allows much higher doping and thinner drift region layers for a given blocking voltage, resulting in lower specific on-resistance [1]. This implies that SiC devices can offer higher power rating at low static and dynamic losses as compare to Si devices. These theoretical appraisals make SiC a very promising material for high power uni/ bi-polar devices for high speed/voltage switching for electric vehicles [2] and electric power distribution [3]. Other applications include the high power microwave electronics for radar and communications [4] and high temperature sensors and control systems for automobile engines [5]. However, there are several vital issues related to the device fabrication processes and crystal growth that must be overcome to realize the practical electronic devices. Several problems related to the MOS interface have become apparent to date and need to be solved. The poor quality of the oxide grown on p-type SiC which results in the high interface surface states and low inversion layer mobility was reported as the major limiting factor for realizing the practical MOS based power devices [6,7]. Moreover, the RIE technique which is used to form the SiC trench structure, also produce defects in the trench surface by impact of high energy ions. The resultant surface roughness leads to surface scattering which results in the reduction of the channel mobility. This surface roughness also lowers the gate SiO_2 breakdown voltage and leads to large increases in leakage current between the source and drain. Therefore, all these factors eventually lead to a severe degradation in the device characteristics. The immaturity of the SiC crystal growth technology further degrades the device characteristics by causing early breakdown at the crystal defects. This indicates that the predicted low on-state resistance with high blocking voltage for SiC power devices cannot be achieved by conventional DIMOS or UMOS structures.

This paper reviews the recent progress made in SiC power electronics and reports our new transistor named the EC-FET, designed for SiC power switching applications[7]. EC-FET can address most of the open issues related to MOS interface viz., high fixed insulator charge and interface surface states,

low channel mobility and high electric field at the trench corner of FET. Also, the EC-FET can withstand up to the avalanche breakdown conditions and hence leads to a break-through technology for accumulation mode devices.

2. EC-FET Structure

A unit half-cell cross-section of the trench EC-FET structure is shown in Fig. 1. The main feature of designed EC-FET is that the channel region is epitaxially grown on the trench sidewall. The current flows via an accumulation mode through the channel defined in the n-type SiC trench sidewall epi-layer. Therefore, the EC-FET can counter the problems related to the poor quality of the gate oxide grown on p-type SiC in conventional MOSFETs. The epi-channel also compensates for the surface damage induced during trench formation by RIE. In this design, the epi-channel provides an independent control of the impurity concentration of the channel and the p-base region. Therefore, a power EC-FET with high blocking voltage, low on-state resistance and low threshold voltage can be designed. In particular, the lower impurity concentration of the channel region is less influenced by impurity scattering, thus improving the channel mobility, since the blocking voltage is mainly governed by the impurity concentration and thickness of the p-base and n^- drift region. Moreover, the higher p-base impurity concentration can relax the maximum electric field near trench corner of the EC-FET.

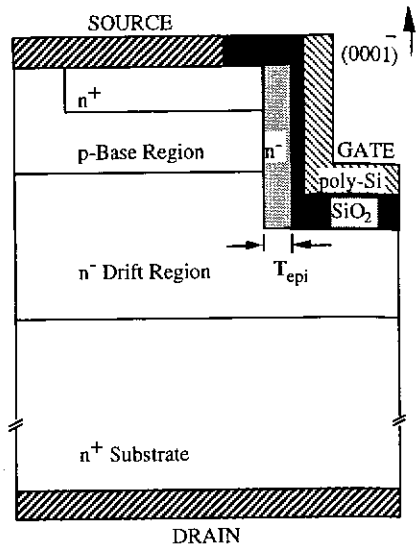

Fig.1 A unit half-cell cross-sectional structure of the trench EC-FET.

In this design, the accumulation mode MOS structure regulates the flow of electron current. The epitaxially grown n-type SiC trench sidewall layer that defines the channel region can be completely depleted by the potentials created by the work function difference between the p-type SiC base layer and the n-type SiC trench sidewall epi-layer, and the work function difference between the n-type SiC trench sidewall epi-layer and the poly-Si gate electrode. The potential created by the work function difference between the n-type SiC trench sidewall epi-layer and the poly-Si gate electrode controls the channel condition during operation. In the off-state, a depletion region is formed in the epitaxially grown n-type SiC trench sidewall layer by the built-in fields of the p-type SiC base layer and the poly-Si gate electrode. The device can be switched to the on-state by the application of a positive bias to the gate to create an accumulation layer channel in the n-type SiC trench sidewall epi-layer, extending from the n^+ source to the n^- drift region. Electrons flow vertically from the n^+ source along the accumulation layer to the n^- drift region.

Two dimensional device simulations using the TMA MEDICI simulator have been carried out to estimate the impact of epi-channel parameters on electrical characteristics of 4H-SiC trench EC-FET. The material parameters and their variation with temperature were carefully selected from the available data[8,9]. The device parameters viz., thickness and the impurity concentration of the trench n-type sidewall epi-layer, the p-base layer and n^- drift layer were optimized to minimize the on-state resistance under the condition of 1000V blocking voltage. The p-type poly-Si was used as the gate electrode. The thickness of the epi-channel in this design, depends on its impurity concentration, SiO_2 film thickness, and the type of poly-Si gate electrode. Figure 2 shows a correlation between the blocking voltage, thickness and impurity concentration of the epi-layer. It can be seen that for a given impurity

concentration, the blocking voltage strongly depends on the thickness of the epi-channel. It also depends on the type of poly-Si used for the gate electrode. It should be noted that in this design, the normally-off characteristics with a blocking voltage of 1000V can be achieved even at the impurity concentration of $1.0x10^{17}cm^{-3}$ for the epi-channel. This epi-channel can withstand up to the avalanche breakdown conditions.

Another key point of EC-FET design is the electric field relaxation near the trench corner. In conventional trench MOSFETs, the high electric field near the trench corner due to electric field crowding results in the oxide breakdown as the field in the oxide is 2.5 times higher than that of SiC material. In this structure, the impurity concentration of the p-base layer which is independent of channel region can be used as an important parameter to tailor the maximum electric field (E_{max}) near the trench corner. The impurity concentration of the p-base layer can be increased to relax the E_{max} near the trench corner of the EC-FET. Figure 3 shows a comparison of E_{max} at the trench corner of the EC-FET with conventional structure. Model was simulated for the MOSFET of 1000V blocking voltage, however, the E_{max} is plotted for applied voltage of 500V. For conventional MOSFET, the E_{max} is about 1.9MV/cm at the trench corner with p-base impurity concentration of about $1.0x10^{16}cm^{-3}$, which is of the same order as that of epi-channel layer. In the case of EC-FET, the E_{max} is about 1.5MV/cm at the trench corner with p-base impurity concentration of about $1.0x10^{18}cm^{-3}$. This value of E_{max} is about 20% lower as compared to a conventional structure. Therefore, the p-base layer is relatively highly doped compared to the channel region to relax E_{max} at the trench corner of the EC-FET.

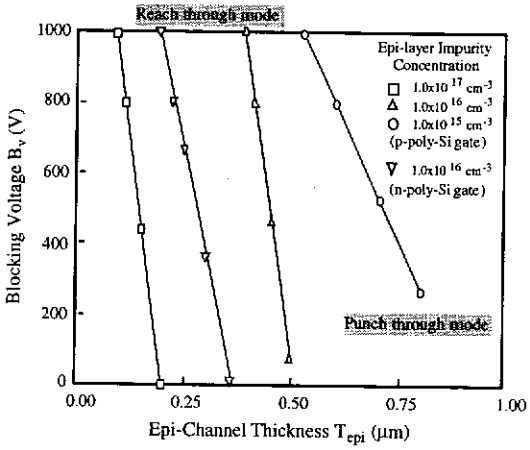

Fig.2 Blocking voltage dependence of the 4H-SiC trench EC-FET on thickness and impurity concentration of epi-channel layer.

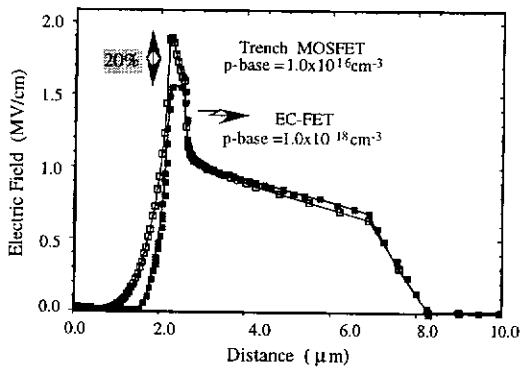

Fig.3 A comparison of maximum electric field at trench corner of the EC-FET structure and the conventional structure.

3. EC-FET Process Discription

Anisotropy in thermal oxidation and epitaxial growth of SiC was utilized to develop the EC-FET. The trench EC-FETs were fabricated using $(000\bar{1})$ C-face 4H-SiC p/n/n^+ epi-wafers. Hexagonal structure microcells of 23μm cell-pitch were selected for integration, keeping in mind the hexagonal structure of SiC crystal. The hexagonal microcells have angles of 120° between the trench sidewalls and offers improvement for the two dimensional oxidation conditions as it reduces stress at the edges. The trench was formed on the wafer surface by RIE and extends in the $[1\bar{1}00]$ direction. The epi-layer was growth on the trench sidewall $(1\bar{1}00)$ prism face plane. The gate SiO_2 was thermally grown by the pyrogenic method. The SiO_2 film was thin on the trench $(1\bar{1}00)$ prism face surface and thick on the top/bottom $(000\bar{1})$ C-face surface[10,11]. The 2380 hexagonal structure microcells of 23μm pitch

were integrated in the 2mm square size chip. A cross-sectional SEM micrograph of the fabricated accumulation mode 4H-SiC trench EC-FET is shown in Fig. 4. The trench sidewall epi-layer on $(1\bar{1}00)$ prism face plane can be seen clearly in the SEM micrograph. The epitaxial growth on the trench sidewall characteristically forms an extremely smooth surface and coverage selectively in $[1\bar{1}00]$ orientation. The measured interface state density at SiC/SiO_2 interface was about one order of magnitude lower than that without the trench sidewall epi-layer [7].

4. Electrical Characteristics

Typical drain current (I_D) - drain voltage (V_D) characteristics of the fabricated 4H-SiC trench EC-FET is shown in Fig.4. The field effect conduction of the vertical channel was observed as its I_D increases in response to gate voltage (V_G). Fabricated device has a I_D of 100mA at V_D of 0.10V (V_G=10.0V). The active area, channel length and width of 2mm square size chip were estimated as 1.095×10^{-2} cm^2, 1.5μm, and 15.66cm, respectively. The measured specific on-state resistance of the 4H-SiC trench EC-FET was 10.9mΩ.cm^2. An effective accumulation-mode channel mobility (μ_{eff}) was estimated from the plot of I_D-V_G with V_D =0.1V. The threshold voltage defined by the tangential line was 3.3V. The extracted μ_{eff} was 108.2cm^2/V.s at room temperature. This value of μ_{eff} is approximately 5 times the channel mobility reported for the inversion mode trench MOSFETs. The drain-to-source blocking voltage (B_V) was more than 450V. The breakdown phenomenon probably occurred at the trench corner due to SiO_2 breakdown. Simulations assuming the lower permissible maximum electric field of SiO_2 indicate the breakdown point near the trench corner where the electric field in SiO_2 is enhanced by a factor of 2.5 compared to SiC.

5. SiC Material Issue

The fact that SiC power devices are still unavailable today can be attributed to the technological difficulties involved in the device processing and crystal growth technology. The area of major concern in the MOS based power device processing is the SiO_2/SiC interface quality and its high temperature reliability. The EC-FET can address most of the open issues related to MOS interface, however, problems arise from the immaturity of material technology. The material quality is the main obstacle to the development of SiC power devices. The issues for the commercial success of SiC power electronics are the SiC wafer size and crystal defect density. High quality substrates are a prerequisite for industrial-scale fabrication of power semiconductor devices which to date are lacking for SiC. The commercially available SiC wafers still contain too many defects to be used for low cost production. The X-ray

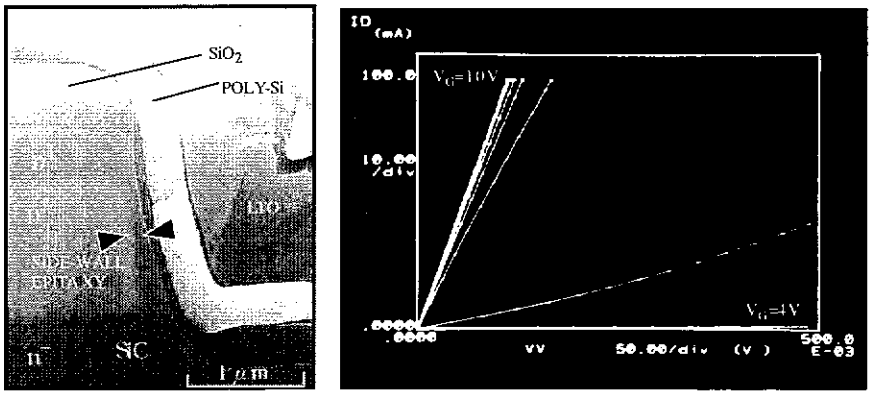

Fig.4 Cross-sectional FE-SEM micrograph and typical I_D -V_D characteristics of the fabricated 4H-SiC trench EC-FET

topogram of the 4H-SiC wafer in Fig.5 shows the structural imperfection of the SiC material. The dislocation density is typically in the order of 10^4-10^5 cm^{-2}. The secondary effects of dislocation centers on leakage current or breakdown phenomenon are not clear for unipolar devices, however, these defects can act as life time killer for bipolar devices. Dislocation centers can also serve as one of the possible origin of micropipes, a void like defect. Micropipes propagate in the growth direction from the seed crystal. Its size depends on the growth condition and the related origin. The typical value of the micropipe diameter is about 0.5 to 5μm. There are several thermodynamic, kinetic and technological mechanisms which causes micropipes in SiC wafers grown by modified Lely seeded sublimation method [13]. Reduction of the micropipe defect that limits the fabrication of large area power devices is one vital issue for the application of SiC technology. The optical micrograph of the 4H-SiC wafer in Fig. 6 (i) shows the plan view of micropipe defects. Micropipe defects present in the SiC wafer generally propagate into the CVD grown epitaxial layers which lead to premature junction breakdown well below the maximum permissible electric field due to generation of microplasmas at the micropipes [14]. Therefore, a single micropipe defect in the high voltage pn-junction can destroy the junction's ability to block the higher voltages. In addition to micropipe defects, the quality of CVD epi-layers, free from other poly-type inclusions, is also a major issue for the realization of high power devices. One of the common defects observed in SiC CVD epitaxial growth is the hexagonal comet tail defect as shown in Fig.6 (ii) for (000$\bar{1}$) C-face epi-layer. This defect may originate from the crystal imperfections that suppress the step flow growth and results in the 2-dimensional nucleation of 3C-SiC poly-type. The fabricated devices show large leakage currents and result in low blocking voltage at the comet tail defects hence also limit the high performance of power devices.

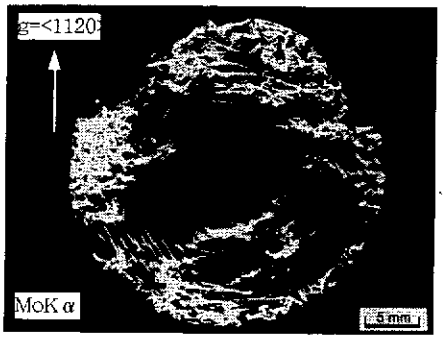

Fig 5. X-ray topogram of 4H-SiC wafer with large dislocation density.

The density of micropipe defects has come down from 1000cm^{-2} to <30cm^{-2} in the last few years. This level must be reduced down to <1cm^{-2} to realize large area power devices. Figure 7 shows a correlation between the yield and the chip size for a given defect density. The experimental data for the developed EC-FET is also plotted in the figure. A process yield of more than a few percent is only possible for the EC-FET chip of 4mm square size. This restricts the maximum current rating of developed SiC power devices to a few amperes. Therefore, these defects have to be eliminated for the development of practical SiC power devices.

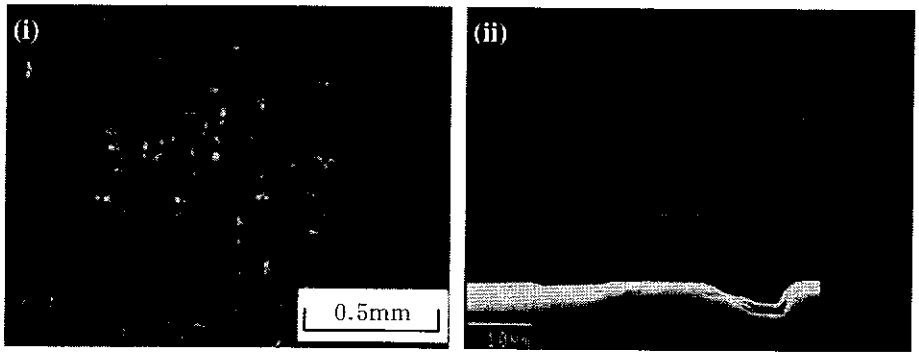

Fig 6. Optical micrograph of 4H-SiC wafer showing (i). plan view of micropipe defects and (ii). hexagonal comet tail defects (inset: SEM cross-sectional view).

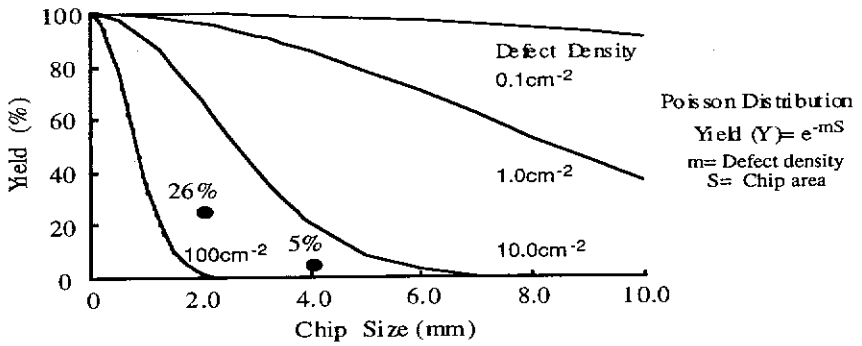

Fig 7. A correlation of EC-FET yield and chip size as a function of defect density.

6. Conclusions

Several vital issues related to MOS based SiC power device fabrication processes and material technology have been reviewed. To address MOS interface related issues, the EC-FET was exclusively developed for SiC power devices. It was demonstrated that the EC-FET can address most of the open issues related to MOS interface viz., high fixed insulator charge and interface surface states, low channel mobility and high electric field at the trench corner of the FET. The 2mm square size chip of 4H-SiC trench EC-FET feature the on-state resistance as low as 10.9mΩ.cm^2 at room temperature with blocking voltage of more than 450V, surpassing the limits of Si power devices. The accumulation mode epi-channel has improved the channel mobility to more than 100cm^2/V.s. However, major problems comes from the immaturity of SiC material technology. The fabricated SiC power devices shows large leakage currents and result in low blocking voltage at the crystal and epi-layer defects. Therefore, these defects have to be eliminated for the development of practical SiC power devices.

References

[1] M. Bhatnagar and B. J. Baliga, IEEE Trans. Electron Devices 40 (1993), p. 645.
[2] B. J. Baliga, Proceedings of the IEEE 82 (1994), p. 1112.
[3] N. G. Hingorani and K. E. Stahlkopf, Scientific American 269 (1993), p. 78.
[4] R. J. Trew, J.-B. Yan, and P. M. Mock, Proceedings of the IEEE 79 (1991), p. 598.
[5] W. C. Nieberding and J. A. Powell, IEEE Trans. Industrial Electronics 29 (1992), p. 103.
[6] A.K. Agarwal, R. R. Siergiej, S. Seshadri, M. H. White, P. G. McMullin, A.A. Burk, L.B. Rowland, C.D. Brandt, and R.H. Hopkins, Proc. 8th Int. Symposium on Power Semiconductor Devices & ICs, Hawaii, May 20-23, 1996 , p.119.
[7] S. Onda, R. Kumar, and K. Hara, Phys. Stat. Sol. (a) 162, (1997), In press.
[8] M. Ruff, H. Mitlehner, and R. Helbig, IEEE Transactions on Electron Devices 41 (1993), p. 1040.
[9] W.J. Schaffer, H.S. Kong, G.H. Negley, and J.W. Palmour, Proc. 5th SiC and Related Material Conf., Washington, DC, 1993, Inst. Phys. Conf. Ser. 137 (1993), p.155.
[10] T. Miyajima, N. Tokura, A. Fukumoto, H. Hayashi, and K. Hara, Jpn. J. Appl. Phys. 35 (1996), p. 1231.
[11] N. Tokura, K. Hara, Y. Takeuchi, T. Miyajima, and K. Hara, Proc. 6th SiC and Related Material Conf., Kyoto, 1995, Inst. Phys. Conf. Ser. 142 (1995), p.637.
[12] N.Tokura, K. Hara, T. Miyajima, H. Fuma, and K. Hara, Jpn. J. Appl. Phys. 34 (1995), p. 5567.
[13] V.F. Tsetkov, S.T. Allen, H.S. Kong, and C.H. Carter, Jr., Inst. Phys. Conf. Ser., 142 (1996), p.17.
[14] P.G. Neudeck and J.A. Powell, IEEE Electron Device Lett., 15 (1994), p. 63.