Journal of The Electrochemical Society, **157** (6) H643-H646 (2010)
0013-4651/2010/157(6)/H643/4/$28.00 © The Electrochemical Society

Wet Chemical Etching of Si, $Si_{1-x}Ge_x$, and Ge in $HF:H_2O_2:CH_3COOH$

B. Holländer,[a,z] D. Buca,[a,*] S. Mantl,[a,*] and J. M. Hartmann[b,*]

[a]*Institute of Bio- and Nanosystems and JARA-Fundamentals of Future Information Technology, Forschungszentrum Jülich GmbH, D-52425 Jülich, Germany*
[b]*CEA-LETI, MINATEC, F-38054 Grenoble Cedex 9, France*

Device concepts are applied to strained layers ranging from pure Si to pure Ge to achieve higher carrier mobilities. Strain is generated by growth on $Si_{1-x}Ge_x$ buffer layers with an appropriate Ge content. Processing of these heterostructures requires selective removal of individual layers. Different approaches to the etch Si, $Si_{1-x}Ge_x$, and Ge layers have been evaluated in terms of the etch rate, selectivity, and isotropy. All investigated etching methods used highly selective chemical etching solutions composed of HF, hydrogen peroxide, and acetic acid ($HF:H_2O_2:CH_3COOH$). The effect of the different HF content on the etch rate of pure Si, pure Ge, and $Si_{1-x}Ge_x$ alloys with Ge mole fractions between 20 and 75% is presented. In general, the etch rate increases significantly with the increase in Ge content. As an example, the etch rate increases by a factor of more than 100 when the Ge content increases from 20 up to 75 atom %.
 [DOI: 10.1149/1.3382944]

Manuscript submitted January 13, 2010; revised manuscript received March 8, 2010. Published April 23, 2010.

Today the whole complementary metal oxide semiconductor community is looking for solutions to meet the International Technology Roadmap for Semiconductors (ITRS) roadmap requirements. Process induced strain techniques are widely used today for 65 and 45 nm node technologies to boost the mobility in short devices. Nevertheless, for 32 nm and below, aggressive design rules reduce the efficiency of such techniques and such "local strain approaches" are not efficient enough to fulfill the ITRS roadmap requirement in terms of the drive current. To compensate for this, the wafer level tensely strained silicon-on-insulator (sSOI) approach gained a lot of attention today. Silicon-on-insulator (SOI) is already on the roadmap for high performance as well as low power and radio-frequency applications seen as electrostatic and dynamic booster solutions, thanks to improved subthreshold swing (for fully depleted devices), smaller parasitic elements, and, in partially depleted technology, to floating body effects. Tensely strained Si enhances the electron mobility in n-type Metal Oxide Semiconductor Field Effect Transistor (nMOSFETs),[1-3] whereas uniaxially, compressively strained Si channels increase the hole mobility in p-type Metal Oxide Semiconductor Field Effect Transistor (pMOSFETs).[4] Heteroepitaxy of SiGe on Si is a promising route to obtain such strained structures. The difference in lattice parameter between Si and Ge yields elastically strained layers. Furthermore, novel substrates, such as strained SiGe-on-insulator (SGOI) or Ge-on-insulator (GOI) can be fabricated with the SmartCut or the Ge enrichment processes. A significant electron mobility enhancement has been successfully demonstrated in biaxially tensely sSOI layers.[3,5] High hole mobilities can be achieved in devices built on thin SiGe layers on top of biaxially strained, on relaxed/strained SGOI with a high Ge fraction or even better strained /unstrained GOI substrates.[6,7] In general, strain in individual layers is generated by growth on the appropriate $Si_{1-x}Ge_x$ buffer layers. The amount of strain is determined by the lattice constant of the buffer layer, which depends on the Ge content.

An SOI substrate is fabricated by the transfer of a Si layer onto an oxidized handle wafer by wafer bonding and layer splitting (the so-called SmartCut process). The fabrication of an sSOI substrate is slightly more complicated. It first requires the growth of a thin strained Si layer on top of a thick relaxed SiGe buffer[8] or a thin strained SiGe layer on Si and subsequent relaxation, creating a virtual substrate for the epitaxial growth of the desired strained Si layer.[9] Through a process similar to the one used for the SOI fabrication, the strained Si/relaxed SiGe layer stack is then transferred to an oxidized handle wafer.

For the strained Si fabrication using a graded buffer approach SiGe layers with a Ge content up to 40% are grown. In the more complex process of strained and unstrained Ge layer growth, a reverse graded buffer layer approaches the Ge content reaching up to 100%. Although the on-insulator substrate fabrication typically requires thick layer etching, high but selective etching rates are necessary to remove the remaining SiGe layers and end up with the desired substrate. One could, to that end, employ either dry plasma etching (e.g., CF_4 plasma), gaseous in situ HCl thermal etching or wet chemical etchings, which have strengths and drawbacks each. The former two methods are more suitable for lateral etching of the Si/SiGe heterostructure.[10,11]

Conventional wet chemical etching solutions for SiGe alloys include an oxidizer and an oxide removal agent. The most common solutions are HF for silicon oxide etching and a solution composed of hydrogen peroxide and acetic acid ($H_2O_2:CH_3COOH$) for SiGe oxidation. $HF:H_2O_2:CH_3COOH$ was reported to serve as a highly selective etchant to remove $Si_{1-x}Ge_x$ over Si with improved smoothness compared to solutions based on HF and H_2O_2 diluted in water.[12,13]

In this study, we present the etching of Si, Ge, and $Si_{1-x}Ge_x$ using different wet chemical etching conditions and extend SiGe etching rate data to Ge mole fractions between 20 and 100%. The etching rates are compared in three cases: (*i*) blanket etching in a bath, (*ii*) blanket etching in a single wafer spin processor, and (*iii*) lateral etching of SiGe/Si heterostructures.

Experimental

Intrinsic $Si_{1-x}Ge_x$ layers with thicknesses of about 1 μm were grown by reduced pressure-chemical vapor deposition (RP-CVD) on thick, linearly graded $Si_{1-y}Ge_y$ ($y \leq x$) buffer layers on Si(100) substrates.[14] Chemical mechanical polishing was used on as-grown stacks to get rid of the surface crosshatch. The Ge contents of the different alloys were verified by Rutherford backscattering spectrometry. In addition, an RP-CVD grown, thermally cycled 2.5 μm Ge layer on Si(100) [15] as well as a pure Si(100) wafer were investigated for comparison. The samples were partially masked with a polymer before etching to form a suitable etch step. After etching and removal of the mask, the height of the etch step was measured using a Dektak 6M stylus surface profiling instrument. Etching for times between 30 s and 10 min was performed in polypropylene beakers at room temperature (25°C) with slight agitation.

Three different $HF:H_2O_2:CH_3COOH$ etching solutions with volume ratios of 1:2:3 were prepared using H_2O_2 [30% in ultralarge-scale integration (ULSI)-grade water], CH_3COOH (99.8%), and HF with various concentrations: 50, 20, and 10% (in ULSI-grade water). For brevity, the solutions were named HF50, HF20, and HF10, respectively. The etching rate of $HF:H_2O_2:CH_3COOH$ solutions varies

* Electrochemical Society Active Member.
z E-mail: b.hollaender@fz-juelich.de

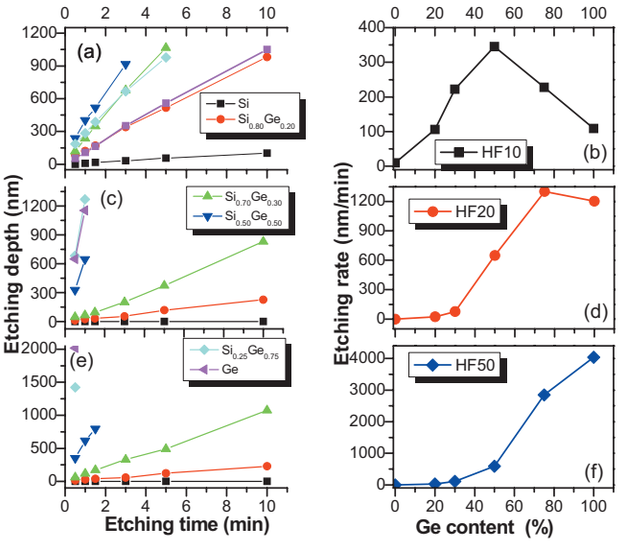

Figure 1. [(a), (c) and, (e)] Etching depth as a function of the etching time and [(b), (d), and (f)] etching rate as a function of the Ge atom % for Si, Ge, and SiGe alloys using the [(a) and (b)] HF10 [(c) and (d)] HF20, and [(e) and (f)] HF50 chemical solutions (bath).

in time, starting with a low etch rate for a freshly prepared solution and reaching a higher and constant etch rate after 48 h. Aging is necessary to obtain a stable equilibrium of the concentrations of H_2O_2, CH_3COOH, and their reaction product peracetic acid, which acts as the oxidizing species.[16]

For the study of the lateral etching speed and selectivity, SiGe/Si staircase heterostructures were epitaxially grown on Si(100) and then patterned by lithography and anisotropic etching. In this case, the etching efficiency was measured employing cross-sectional scanning electron microscopy (SEM).

Results and Discussion

Blanket, vertical layer etching in a bath.— Detailed bath etching experiments were performed to determine the etch depth vs time and thus etch rates. Initial experiments showed that the etching rate obtained after the aging of the freshly prepared solutions for 2 days is stable for at least a week. Because the solution HF50 leads to rather fast etching of SiGe with a higher Ge content, two different solutions using a more diluted HF, namely, HF20 and HF10, were tested to obtain slower and more appropriate etching rates. Etching times of 30 s, 60 s, 90 s, 3 min, 5 min, and 10 min were used. The measured etch depth in pure Si, pure Ge, and several SiGe layers with different Ge contents vs time obtained by etching in HF10 are shown in Fig. 1a. The results showed that the etch depth is nearly linear with time. The etch rate depends significantly on the Ge content of the layers. The etching depth increases linearly with the etching time within the investigated times and experimental accuracy. The etching rate also increases with the Ge content up to about 50 atom % Ge followed by a slight decrease for higher Ge contents up to pure Ge. Figure 1b shows the etch rate vs the Ge content averaged over all the applied etching times for the HF10 solution. The etch rate increases from about 10 nm/min for pure Si to a maximum of 350 nm/min for $Si_{.50}Ge_{.50}$ and then decreases again to a value of 110 nm/min for pure Ge. The etching process consists of two individual reactions. The material is first oxidized by the mixture of hydrogen peroxide and acetic acid and the oxide is finally dissolved by HF. The etching rate is limited by the slowest of both processes. Similar experiments were carried out with the etching solution called HF20, which contained HF in a higher concentration. The corresponding etch depth obtained for pure Si, pure Ge, and SiGe layers with different Ge contents as a function of etching time in HF20 are shown in Fig. 1c. As for the HF10 etching, a linear increase in the etching depth with increasing time was also observed. Significantly higher etch rates were obtained, especially for higher Ge contents, whereas the etching of pure silicon was retarded. The highest etch rate was measured for a SiGe alloy with a Ge content of 75 atom %. The etch rates averaged over all the data points of Fig. 1c are shown in Fig. 1d. Finally, the etching experiments were performed with the HF50 solution. Data on the selective etching of SiGe over Si with HF50 were already reported for Ge contents up to 40 atom %.[12,17] Figure 1e shows the corresponding etch step heights obtained in pure Si, pure Ge, as well as SiGe alloys with different Ge contents after etching with the HF50 solution. Also in this case, the etch depth increased linearly with etching time. A much higher selectivity (defined as the etch rate of SiGe or pure Ge divided by the Si etch rate) was observed for the HF50 solution. Etching of high Ge content SiGe layers and pure Ge was indeed extremely fast. About 2000 nm of pure Ge were already etched after 30 s in the HF50 solution. The corresponding etch rates shown in Fig. 1f exhibit a strong increase with increasing Ge content in the range of 50 atom % and pure Ge. In general, the selectivity is higher for etching solutions containing a higher amount of HF. The etching rates for SiGe alloys with high Ge content or pure Ge layers were extremely large. The strong increase in the etch rate with increasing Ge content shifts and occurs in the range of Ge atom % of 0–50, 20–75, and 50–100 for the HF10, HF20, and HF50 solutions, respectively. This effect allows choosing a proper etching solution depending on the Ge content in the layer and the required selectivity.

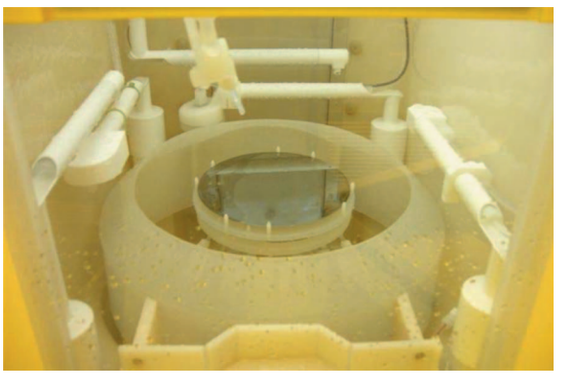

Figure 2. The single wafer spin processor chamber.

Blanket, vertical layer etching in a spin etch processor.— To determine the feasibility of the wet chemical etch of SiGe in the large scale industrial fabrication process, we transferred the SiGe etching process to a single wafer spin processor tool that offers controlled dispensing of the etch solution via movable arms (see Fig. 2). This tool is equipped with optical end-point detection capability, allowing to fully automate the process. Dispense of the chemicals is done via movable arms that span the whole wafer area and whose speed can be controlled, whereas the wafer rotates underneath the arm. This results in a homogeneous distribution of the chemicals over the wafer. A heat transfer system is also available, giving the opportunity of heating the solution up to 90°C.

The etching process consists of an oxidation and an oxide etch step. The etch rate varies with the time given for the solution to react with the material. In this respect, the wafer rotation defines the chemical reaction time. High rotation speeds (over 600 rpm) lead to low rate, nonuniform etches. The rotation speed should be chosen in such a way to maximize the etching rate and to reduce consumption of the chemicals. A speed of 200 rpm gives the best balance between the etch rate and the efficient use of the solution.

Dispensing of the chemicals on the wafers is a key parameter for etching uniformity. The best results regarding uniformity have been obtained using stream instead of a spray dispense. A better wafer

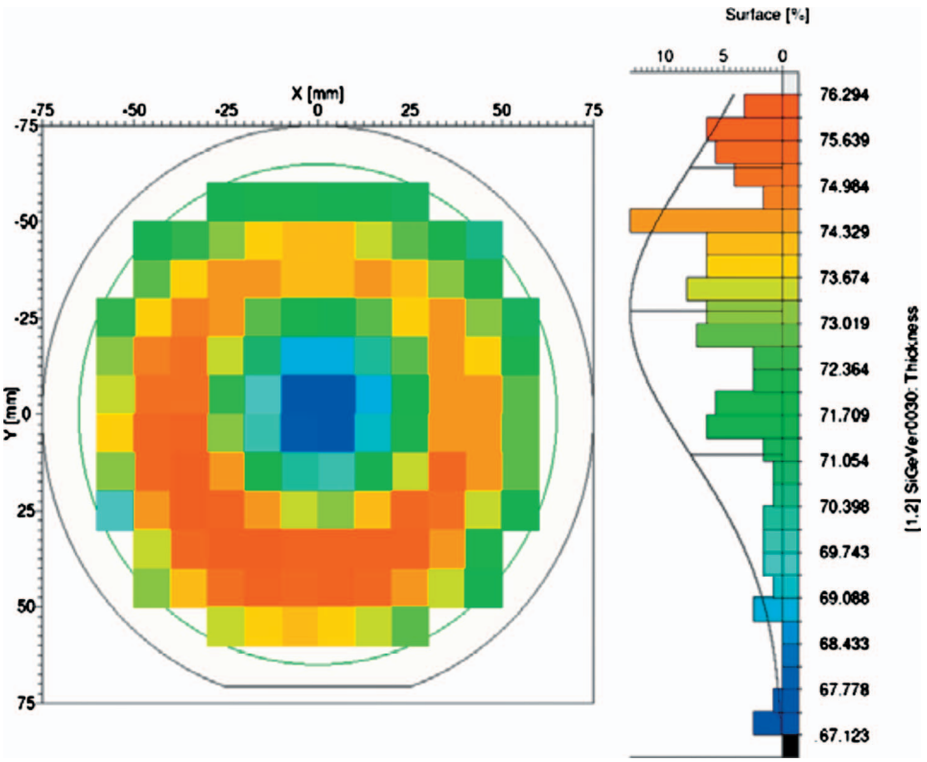

Figure 3. Spectroscopic ellipsometry mapping of the thickness (on a 150 mm wafer) of an initially 170 nm thick $Si_{0.78}Ge_{0.22}$ layer after a 1 min etching in the single wafer spin processor chamber (etched thickness: ~70 nm).

coverage is then obtained. The solution delivery starts at the wafer edge and the dispense arm travels uniformly across the wafer. The etch time is given by the speed of the dispense arm and the number of scans. The etch rate was determined by measuring the remaining SiGe layer after etch processes of 30 s. The resulting etch uniformity is determined by ellipsometric wafer mapping, as shown in Fig. 3, for a 170 nm thick $Si_{0.78}Ge_{0.22}$ layer after 1 min etch using the HF10 solution at a wafer rotation speed of 200 rpm. A very uniform etching over the 150 mm wafer is obtained: The standard deviation of the remaining $Si_{0.78}Ge_{0.22}$ thickness is indeed less than 2% after the removal of roughly 100 nm.

The etch rate can be further increased by increasing the oxide removing rate (HF concentration) at the same oxidation rate. Higher HF concentrations decompose $SiGeO_2$ formed faster, exposing the SiGe surface to the action of the oxidizing agent. SiGe 22% etch rates using 10 and 49% HF concentrations are given in Table I as a function of wafer rotation speed and solution aging.

Table I. The $Si_{0.78}Ge_{0.22}$ etch rate as a function of the wafer rotation speed, HF volume concentration, and solution aging time in the spin etch chamber shown in Fig. 2.

HF(10%):H_2O_2:CH_3COOH = 1:2:3, 20°C, fresh prepared 400 rpm, 30 s etching time; etch rate: 11 nm/min
HF(10%):H_2O_2:CH_3COOH = 1:2:3, 20°C, fresh prepared 200 rpm, 30 s etching time; etch rate: 17 nm/min
HF(10%):H_2O_2:CH_3COOH = 1:2:3, 20°C, 2 days aging 400 rpm, 30 s etching time; etch rate: 50 nm/min
HF(50%):H_2O_2:CH_3COOH = 1:2:3, 20°C, fresh prepared 200 rpm, 30 s etching time; etch rate: 22 nm/min
HF(50%):H_2O_2:CH_3COOH = 1:2:3, 20°C, 2 days aging 200 rpm, 30 s etching time; etch rate: 140 nm/min

Wet chemical lateral selective etching of $Si/Si_{1-x}Ge_x$ heterostructures.— Very good results for the uniform vertical etching of full wafers or pieces of blanket SiGe layers were presented in subchapters A and B. To determine the lateral etch rate of SiGe as a function of the Ge content (in a bath), we have epitaxially grown the following stack (from top to bottom): 2 nm Si/80 nm $Si_{0.60}Ge_{0.40}$/20 nm Si/100 nm $Si_{0.65}Ge_{0.35}$/20 nm Si/150 nm $Si_{0.70}Ge_{0.30}$/20 nm Si/100 nm $Si_{0.80}Ge_{0.20}$/Si(100) substrate. Using standard optical lithography and a photoresist mask, stripes with a width of 5 and 5 μm spacing are patterned into the heterostructure by dry reactive ion etching (RIE), as shown in Fig. 4.

The RIE process used for patterning is already a slightly selective process, as indicated by the appearance of steps at the edge of the stripe in Fig. 4.[11] The lateral etching of $Si_{1-x}Ge_x$ layers increases with the increase in the Ge content. The samples containing SiGe stripes were afterward wet chemically etched in a bath with the mixture that gives the best etch rate in the wafer spin etching processor HF50. After etching, the samples were stripped and observed by cross-sectional SEM to measure the resulting tunnel depth. The etch rate of the different Ge content SiGe layers is obtained by measuring the remaining width of the SiGe layer as follows

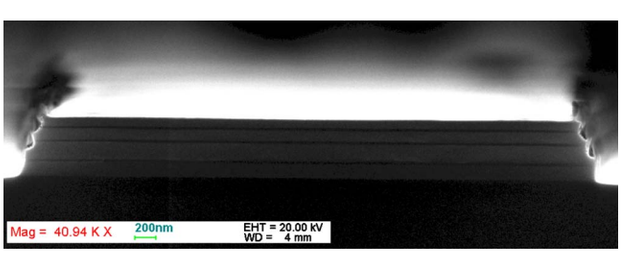

Figure 4. (Color online) Cross-sectional SEM picture of a 5 μm wide Si/SiGe/Si stripe.

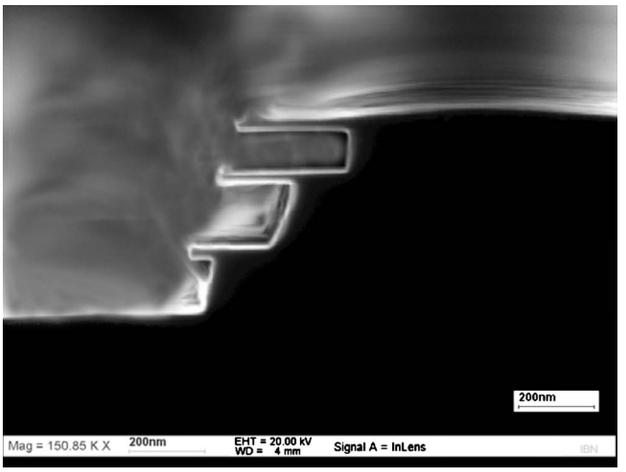

Figure 5. Cross-sectional SEM picture of a Si/SiGe/Si stripe etched for 2 min in HF50%. The top SiGe layer containing 40 atom % Ge is completely removed.

$$R(Si_{1-x}Ge_x) = (w_i\text{-}w_f)/2xt_{etch} \quad [1]$$

where the w_i and w_f are the initial (i.e., after stripe patterning) and final (after etch) widths of the SiGe layer, respectively, and t_{etch} is the corresponding etching time. The very thin (2 nm only) Si cap is etched very fast, thereby exposing the $Si_{0.6}Ge_{0.4}$ layer vertically and laterally to the etching solution. In all our experiments (etching time of 1, 2, 3, and 5 min), this SiGe layer is completely removed (as can be seen in Fig. 5 and 6).

The following etch rates are obtained

$$R(Si_{0.65}Ge_{0.35}) = 170 \text{ nm/min}$$

$$R(Si_{0.70}Ge_{0.30}) = 100 \text{ nm/min}$$

$$R(Si_{0.80}Ge_{0.20}) = 50 \text{ nm/min}$$

Very deep trenches can be obtained, and the lateral etch rate does not decrease with depth. The top Si "wing," shown in Fig. 6, that bent down touching the lower Si layer has a length of 1.2 μm. The same bath etch rate for the SiGe layer with a Ge content of 20 atom % is obtained as in spin etching of a SiGe layer with a Ge content of 22 atom %.

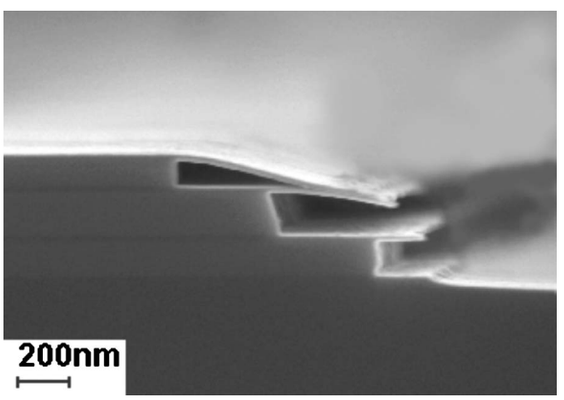

Figure 6. Scanning electron microscope image of a Si/SiGe/Si stripe etched for 5 min. The top Si wing has a 1.2 μm length.

Conclusions

Detailed bath etching experiments were performed to determine the etch depth vs time and etch rates of pure Si, $Si_{0.8}Ge_{0.2}$, $Si_{0.7}Ge_{0.3}$, $Si_{0.5}Ge_{0.5}$, $Si_{0.25}Ge_{0.75}$, and pure Ge. Several series of samples were partially masked and etched in three different types of solutions containing HF, H_2O_2, and CH_3COOH in a volume ratio of 1:2:3. The three different solutions contained HF in concentrations of 50, 20, and 10% and were aged for 2 days before the etching experiments. In general, the selectivity (defined as the SiGe etch rate divided by the Si etch rate) is higher for etching solutions containing a higher amount of HF. Etching rates of SiGe alloys with a high Ge content or pure Ge layers were extremely large. This effect allows choosing a proper etching solution depending on the specific Ge content and the required selectivity. Bath etching experiments were compared to planar etching experiments using an automatic spin etching tool as well as to the lateral etching of the Si/SiGe stacks with different Ge contents.

Acknowledgment

This work was supported by the European Commission, Information Society Technology (IST), within the framework of PULLNANO, contract no. IST-026828.

Forschungszentrum Jülich GmbH assisted in meeting the publication costs of this article.

References

1. M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, *J. Appl. Phys.*, **97**, 011101 (2005).
2. G. Taraschi, A. J. Pitera, L. M. McGill, Z.-Y. Cheng, M. L. Lee, T. A. Langdo, and E. A. Fitzgerald, *J. Electrochem. Soc.*, **151**, G47 (2004).
3. F. Andrieu, O. Faynot, F. Rochette, J.-C. Barbe, C. Buj, Y. Bogumilowicz, F. Allain, V. Delaye, D. Lafond, and F. Aussenac, et al., *Dig. Tech. Pap. - Symp. VLSI Technol.*, **2007**, 50.
4. K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, and R. Chau, et al., *Tech. Dig. - Int. Electron Devices Meet.*, **2007**, 247.
5. I. Cayrefourq, A. Boussagnol, and G. Celler, *ECS Trans.*, **3**(7), 399 (2006).
6. H. Shang, J.O. Chu, S. W. Bedell, and J. Ott, *ECS Trans.*, **3**(7), 679 (2006).
7. E. Augendre, L. Sanchez, L. Benaissa, T. Signamarcheix, J.-M. Hartmann, C. Le Royer, M. Vinet, W. Van Den Daele, J.-F. Damlencourt, K. Romanjek, et al., *ECS Trans.*, **25**(7), 351 (2009).
8. J. M. Hartmann, A. Abbadie, D. Rouchon, J. P. Barnes, M. Mermoux, and T. Billon, *Thin Solid Films*, **516**, 4238 (2008).
9. M. Reiche, C. Himcinschi, U. Gösele, S. Christiansen, S. Mantl, D. Buca, Q. T. Zhao, S. Feste, R. Loo, D. Nguyen, et al., *ECS Trans.*, **6**(4), 339 (2007).
10. T. Salvetat, V. Destefanis, S. Borel, J. M. Hartmann, O. Kermarrec, and Y. Campidelli, *ECS Trans.*, **16**(10), 439 (2008).
11. S. Barnola, C. Vizioz, N. Vulliet, C. Dupré, T. Ernst, P. Gautier, C. Arvet, B. Guillaumot, E. Bernard, S. Pauliac-Vaujeour, et al., *ECS Trans.*, **16**(10), 923 (2008).
12. T. K. Cams, M. O. Tanner, and K. L. Wang, *J. Electrochem. Soc.*, **142**, 1260 (1995).
13. A. Abbadie, J. M. Hartmann, C. Di Nardo, T. Billon, Y. Campidelli, and P. Besson, *Microelectron. Eng.*, **83**, 1986 (2006).
14. Y. Bogumilowicz, J. M. Hartmann, F. Laugier, G. Rolland, T. Billon, N. Cherkashin, and A. Claverie, *J. Cryst. Growth*, **283**, 346 (2005).
15. J.M. Hartmann, A. Abbadie, N. Cherkashin, H. Grampeix, and L. Clavelier, *Semicond. Sci. Technol.*, **24**, 055002 (2009).
16. M. Guder, B. O. Kolbesen, C. Delattre, C. Fischer, H. Schier, and G. Wagner, *Solid State Phenom.*, **134**, 79 (2008).
17. G. K. Chang, T. K. Carns, S. S. Rhee, and K. L. Wang, *J. Electrochem. Soc.*, **138**, 202 (1991).