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Characterisation of $CdCl_2$ treated electrodeposited CdS/CdTe thin film solar cell

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An over 10% efficient electrodeposited CdS/CdTe solar cell has been prepared after $CdCl_2$ treatment. The open circuit voltage, V_{oc}, short-circuit current, J_{sc} and fill factor, FF were 758 mV, 21 mA cm^{-2} and 0.65 respectively. The diode factor calculated from current–voltage–temperature measurements changed from 1.54 at 324 K to 2.64 at 146 K. The voltage factor, α ranged from 22.83 at 324 K to 29.46 at 146 K. Data from current–voltage–temperature measurements agrees with the model of Miller and Olsen and indicates that the current transport was a combination of tunneling and interface recombination. Capacitance–voltage–temperature measurements showed that capacitance decreased with increasing frequency and increased with temperature. Capacitance was insensitive to temperature indicating an intrinsic or low-doped depletion layer. The density of interface states was found to be 6.4×10^{10} cm^{-2} eV^{-1} at 293 K. The carrier concentration of CdTe calculated from Mott–Schottky plot was 1.5×10^{16} cm^{-3}.

1. Introduction

Cadmium telluride material is one of the most promising base materials for a solar cell because of its optimum bandgap of 1.45 eV and high absorption coefficient. Cadmium sulphide, with a bandgap of 2.42 eV, is suitable for a window material for a CdS/CdTe solar cell. The promising approach for the mass production of photovoltaic arrays is the use of a thin film semiconductor deposited onto a low-cost substrate. Efficient CdS/CdTe polycrystalline solar cells have been prepared by different methods such as electrodeposition [1–11], metallorganic chemical vapor deposition (MOCVD) [12], close-spaced vapor transport (CSVT) [13–16], vacuum evaporation [3,17], molecular-beam epitaxy (MBE) [12,18], screen printing [19,20], and sintering [21,22]. Bube et al. [23] reviewed of CdS/CdTe cell research. There are substantial differences in the cell models and characteristics presented by various groups probably due to the differences of the deposition techniques of the materials. Among different techniques, electrodeposition is the most suitable low-cost method. The advantages of this method were (a) the film can be deposited on the desired areas of the substrate, thus minimizing material cost, (b) the deposition can be easily controlled, providing the films of reproducible

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quality, (c) equipment is relatively cheap and the same plating solution can be used for several months.

To obtain a highly efficient solar cell it is necessary to improve the grain size of CdTe to avoid significant bulk recombination, high resistance and large density of interface states. Several groups [18,24–28] have investigated the influence of $CdCl_2$ treatment on the microstructure of CdTe and properties of CdS/CdTe solar cell. Solar cell performance has been previously investigated [24–26] for CdTe films prepared by a high temperature ($T > 600$°C) sintering process using $CdCl_2$ in the CdTe slurry prior to CdTe film formation. CdTe films prepared by electrodeposition, vacuum deposition or MOCVD requires a post deposition of heat treatment with $CdCl_2$ for getting high efficient [28] solar cell. This paper presents the characteristics of the electrodeposited CdS/CdTe solar cells that are treated with $CdCl_2$/methanol.

2. Experimental procedure

The substrate material was indium tin oxide (ITO)/glass (10 Ω/□, purchased from Hoya Electronics, Japan). The substrate was cleaned successively in ultrasonic baths of acetone, methanol and isopropanol followed by isopropanol vapor degreasing.

Details of deposition procedures of CdS and CdTe were previously reported [4]. Here I briefly describe the deposition steps. Cadmium sulphide plating solution of pH 2 was made up as 0.2 M Cd^{2+} and 0.01 M $S_2O_3^{2-}$ by using $CdCl_2 \cdot H_2O$ (analytical grade reagent), $Na_2S_2O_3 \cdot 5H_2O$ (analytical grade reagent) and HCl (BDH chemicals). Cadmium telluride plating solution of pH 2 was made up as 2.5 M Cd^{2+} by using $3CdSO_4 \cdot 8H_2O$ (analytical grade reagent), H_2SO_4 (BDH Chemicals) and by pushing Te (120 ppm) from spectroscopic grade tellurium rod. CdS was deposited onto ITO/glass substrate at a 40 mV more positive potential than the measured cadmium potential. About 100 nm thick CdS film was deposited in about 2 h. In about 1.5 h 1.8 μm thick CdTe film was deposited onto the CdS/ITO/glass substrate at +20 mV QRP (quasi-rest potential) of measured cadmium potential. The dried as-deposited sample was dipped in saturated solution of $CdCl_2$/methanol and dried. The sample was annealed in air at 400°C for the formation of the n-CdS/p-CdTe heterojunction. Basol et al. [29] reported the type conversion of as-deposited n-CdTe to p-CdTe for the electrodeposited CdS/CdTe cells. Prior to copper (2 nm) and gold (100 nm) deposition for electrical connection, the annealed film was etched in 1:1 $H_2SO_4/K_2Cr_2O_7$ solution followed by hydrazine hydrate treatment [1]. Several cells of 0.0314 cm^2 were made.

Current–voltage (I–V) measurements were obtained by a computer controlled system with a 300 W Oriel simulator to produce 100 W m^{-2} AM1 radiation tested by a Si-cell which was calibrated at National Renewable Energy Laboratory (NREL), Golden, CO, USA. Capacitance–voltage–temperature measurements were taken with different frequencies ranging from 10 to 10^5 Hz and temperature

ranging from 211 K to 293 K by using a PAR lock-in amplifier (model 124A) and a Universal programmer (model 175). X-ray diffraction pattern was taken by using a Philips PW 1050/25 diffractometer with Cu Kα radiation.

3. Results and discussion

Fig. 1 shows the X-ray diffraction (XRD) pattern of an air-annealed (400°C/15 min, as a part of cell fabrication) $CdCl_2$/methanol treated CdTe film. As-deposited CdTe film displayed (not shown in figure) a strong XRD peak of (111) with relatively low intensity peaks of (220) and (311). When $CdCl_2$ treated film was annealed in air at 400°C all (111), (220) and (311) peaks showed a high intensity with an extra peak of (440). This indicates the improvement of the crystallinity of the film. We have previously [4,7,9,10] reported that the XRD of an annealed CdTe film (400°C/15 min, without $CdCl_2$ treatment) displayed XRD patterns similar to those of fig. 1. The only difference is that all the peaks are sharper for the $CdCl_2$ treated film relative to the air-annealed one. This indicates that $CdCl_2$ treatment further improves the crystallinity of CdTe.

Current–voltage–temperature measurements in the dark were performed for determining the current transport mechanism of the cell. The I–V characteristics of the device was obtained by using the simple diode equation,

$$J = J_0\{\exp[(q/AkT)(V - iR_s)] - 1\}, \tag{1}$$

where A is the ideality factor, k is the Boltzmann constant, T is the temperature, and R_s is the series resistance: q/AkT is called the voltage factor, α and J_0 is the reverse saturation current. The saturation current, J_0 can be expressed as

$$J_0 = J_{00} \exp(-E_a/kT), \tag{2}$$

where E_a is the activation energy, and J_{00} is a weak function of temperature.

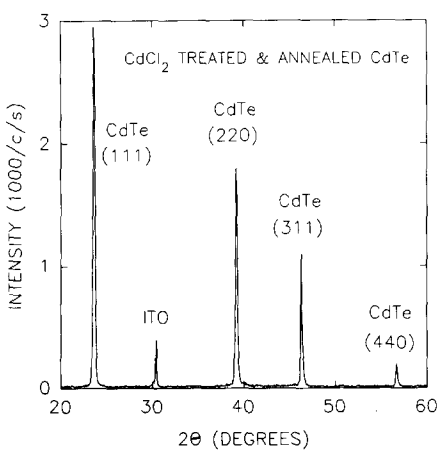

Fig. 1. X-ray diffraction pattern of $CdCl_2$ treated and annealed (400°C/15 min in air) CdTe film.

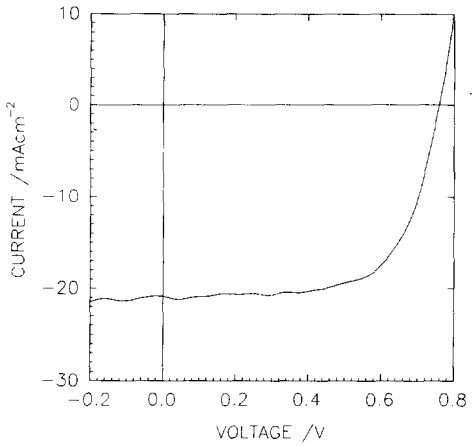

Fig. 2. Current density versus voltage (J–V) characteristics under 1000 W m^{-2} solar simulation of a 10.3% cell.

Fig. 2 shows the current–voltage characteristics of a 10.3% $CdCl_2$ treated cell under 1000 W m^{-2} illumination. The cell parameters are: open circuit voltage, $V_{oc} = 758$ mV, short-circuit current, $J_{sc} = 21.0$ mA/cm^2 and fill factor (FF) = 0.65.

Fig. 3 shows the dark current–voltage characteristics of the cell of fig. 2 at different temperatures ranging from 324 K to 146 K. The extrapolation of the curves upto $V = 0$ gave the values of the saturation currents, J_0, at each individual

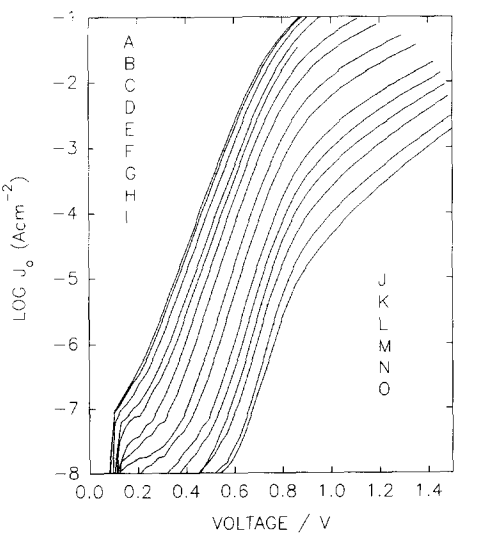

Fig. 3. Current density versus voltage (J–V) characteristics in dark for the cell of fig. 2 at different temperatures. (A) 324 K, (B) 322 K, (C) 315.5 K, (D) 305.5 K, (E) 294 K, (F) 276 K, (G) 261 K, (H) 247 K, (I) 232.5 K, (J) 210 K, (K) 202 K, (L) 192 K, (M) 183 K, (N) 166 K, (O) 146 K.

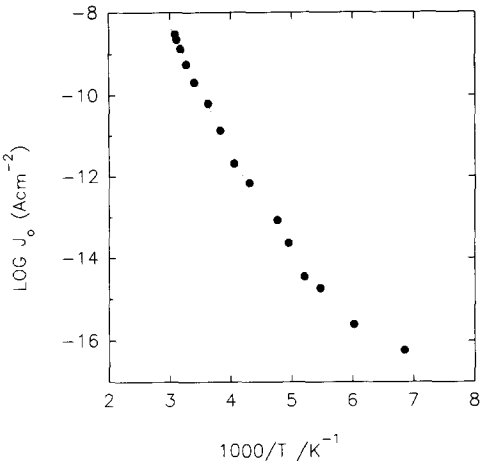

Fig. 4. Temperature dependence of saturation current of the cell of fig. 2.

temperature. The value of the ideality factor, voltage factor and the saturation current are the direct indicators of the properties of the depletion layer and junction properties.

Fig. 4 shows the variation of the saturation current, J_0, with temperature. For a transport mechanism dominated by tunneling, J_0 is essentially temperature independent whereas strongly temperature dependent J_0 indicates a thermally activated process. In fig. 4 it is clear that the saturation current is relatively insensitive to temperature changes below 233 K. This suggests that a tunneling process could be one of the possible current mechanisms at lower temperatures. The activation energy calculated from the log J_0 versus $1/T$ plot gave a value of 0.58 eV. For interface recombination the value of activation energy [30] should be equal to $V_D + \delta P$, where V_D is the diffusion potential and δP is the difference between Fermi level and the valence band of CdTe. The theoretical value of $V_D + \delta P$ for CdS/CdTe device is usually 1.2 eV taking the electron affinity of CdS as 4.5 eV and that of CdTe as 4.28 eV. The activation energy derived from the log J_0 versus $1/T$ plot is much less than the desired value for the condition of interface recombination as being the dominant current mechanism. The ideality factor can be expressed as

$$A = 1 + (N_A \epsilon_{CdTe})/(N_D \epsilon_{CdS}), \tag{3}$$

where N_A and N_D are the carrier concentrations of CdTe and CdS. For our CdS/CdTe device $N_D \gg N_A$. Therefore, $A \approx 1$ for interface recombination as the dominant current mechanism. The value of the ideality factor varies from 1.54 at 324 K to 2.64 at 146 K. This wide variation of ideality factor with temperature also eliminates the possibility of interface recombination being the dominant current mechanism. Several groups [16,18,31–33] have reported the current transport mechanism of their CdS/CdTe solar cells prepared by different techniques. Singh et al. [31] reported the junction transport characteristics of sprayed CdS/CdTe cell

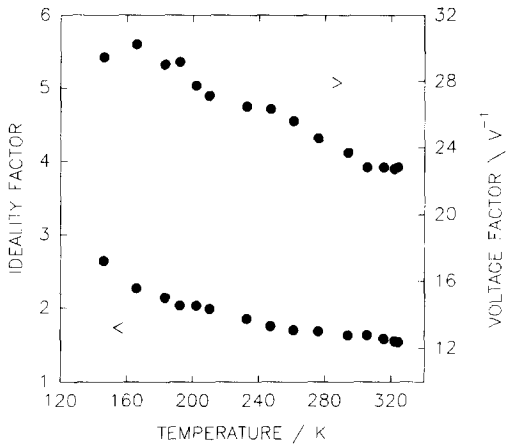

Fig. 5. Temperature dependence of ideality factor, A and voltage factor, α of the cell of fig. 2.

fabricated at Photon Energy Inc. They observed that the ideality factor was sensitive to temperature whereas the voltage factor was almost constant with temperature. The zero bias depletion layer width was more than 1 μm. They proposed a model which explains that the current mechanism was likely due to tunneling across a thin high space charge layer near the interface followed by recombination. Mitchell et al. [32] reported that the bulk recombination dominated at levels near the middle of the gap for their single crystal CdTe/CdS solar cell whereas Anthony et al. [33] suggested recombination either through interface states or through levels in the depletion region displaced from midgap for their thin film CdS/CdTe cell prepared by CSVT technique. Chu et al. [16] reported that the electrical characteristics of the CdS/CdTe heterojunction prepared by close-spaced sublimation (CSS) depend strongly on the cleanliness of the interface. They observed that the current mechanism was controlled by thermally activated process, presumably interface recombination when the surface of CdS was in-situ cleaned prior to CdTe deposition whereas with no in-situ cleaning of CdS showed high reverse saturation current and current transport was dominated by tunneling at lower temperature below 298 K.

Fig. 5 shows the variation of the ideality factor, A, and the voltage factor, α. The voltage factor varies from 22.83 at 324 K to 29.46 at 146 K. The temperature dependence of the voltage factor rules out the direct tunneling mechanism as proposed by Riben and Feucht [34]. The variation of the voltage factor, α, with temperature suggest that thermally assisted tunneling could be the alternative current mechanism. To test the suitability of the recombination/generation in the depletion layer as the dominant mechanism for current flow in our device, the activation energy was calculated from the plot of $\log(J_0 T^{-2.5})$ versus $1/T$ and was found to be 0.57 eV. But the value of activation energy should be close to 0.73 eV, i.e. half of the bandgap of CdTe for such CdS/CdTe device for the recombination/generation in the depletion layer dominated current mechanism. So, recom-

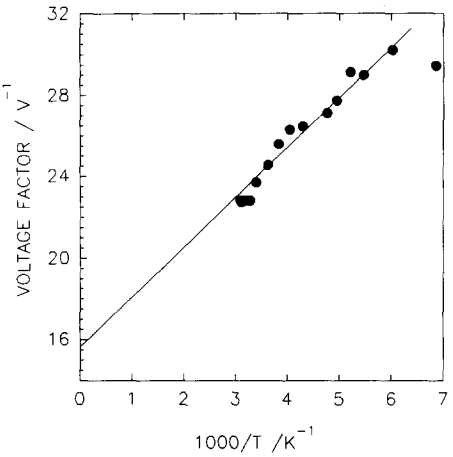

Fig. 6. Plot of voltage factor versus $1/T$ of the cell of fig. 2.

bination/generation is not the dominant current mechanism in our CdS/CdTe cell. Miller and Olsen [35] proposed a model for tunneling/interface recombination (T/IR) transport mechanism which approximates thermally assisted tunneling process of the combination of direct tunneling and pure interface recombination. According to this model, the voltage factor, α, can be expressed as

$$\alpha = (1-f)B + f/AkT, \tag{4}$$

where B is the temperature independent of tunneling, A is the diode factor, k is the Boltzmann constant, and T is the temperature. The value of f quantifies the degree of tunneling character, with $f=0$ being simple tunneling and $f=1$ being simple interface recombination. Fig. 6 shows the plot of voltage factor, α, versus $1/T$. From this plot the value of $(1-f)B$ and f/A were determined to be 15.7 V^{-1} and 0.21, respectively, indicating the current mechanism is controlled by both interface recombination and tunneling. Ringel et al. [18] investigated the electronic mechanism responsible for the improvement in cell performance for $CdCl_2$ treatment of a molecular-beam epitaxy grown polycrystalline CdS/CdTe solar cell. The current mechanism of their $CdCl_2$ treated CdS/CdTe cell was dominated by depletion region recombination whereas our $CdCl_2$ treated CdS/CdTe cell showed both interface recombination and tunneling controlled current transport and this was probably due to the different preparative technique of our CdS/CdTe cell.

The value of barrier height, Φ, can be found from the relation between open-circuit voltage and temperature and can be expressed as

$$V_{oc} = \Phi - (AkT/q)\ln(J_L/J_{00}), \tag{5}$$

where J_L is the light dependent current and other symbols are of usual meaning.

Fig. 7 shows the plot of V_{oc} versus temperature. The value of barrier height was derived from the extrapolation of the straight line to $V=0$ and was found to be

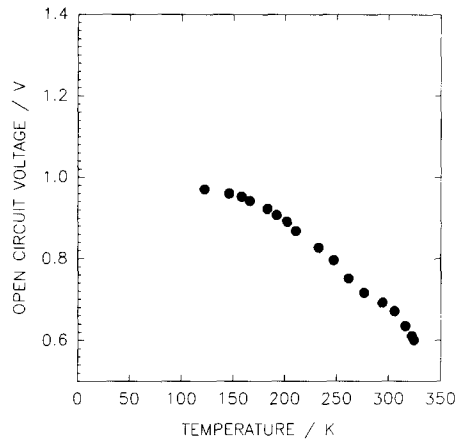

Fig. 7. Temperature dependence of open circuit voltage, V_{oc} of the cell of fig. 2.

1.34 eV, which was very close to the value (1.35 eV) obtained by Fardig and Phillips [36] for their CdS/CdTe cell prepared by vacuum evaporation.

Fig. 8 shows the variation of the capacitance with bias voltage at three different frequencies, 30, 300 and 10^4 Hz. From this figure it is clear that the capacitance decreased with increasing frequency and this indicates a contribution to the junction space charge from relatively slow deep levels at or near the interface of CdS/CdTe. Fig. 9 shows the plots of capacitance versus temperature at different frequencies (10, 10^2, 10^3, 10^4 and 10^5 Hz). At higher frequencies capacitance slowly increased with temperature. At lower frequencies capacitance slowly increased with temperature up to 250 K and then rapidly increased. Fig. 10 is the Mott–Schottky plot of the cell in the dark at 10 kHz frequency. Zero bias

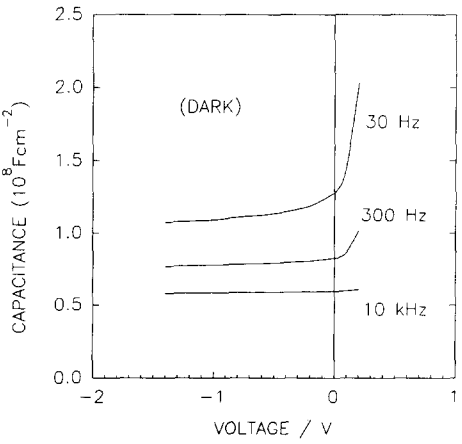

Fig. 8. Variation of capacitance with bias voltage at different frequencies of the cell of fig. 2

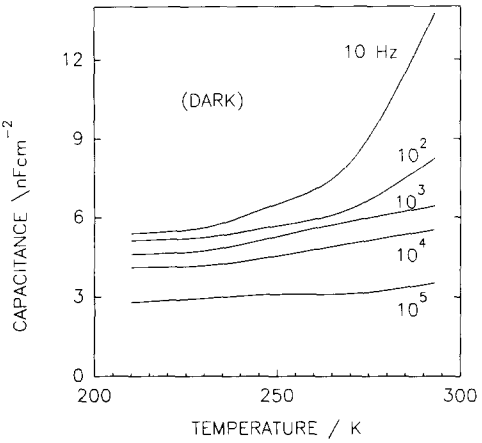

Fig. 9. Variation of capacitance with temperature at different frequencies of the cell of fig. 2.

capacitance yields a depletion layer width (W) of 1.5 μm. Depletion layer width is almost insensitive with reverse bias indicating the intrinsic or low doped depletion layer assuming the doping concentration of CdS is much higher and the depletion layer is mainly inside CdTe. The slope of the plot of fig. 10 gave the value of carrier concentration and was found to be 1.5×10^{16} cm^{-3}. The large value of the voltage intercept of the Mott–Schottky plot at $V = 0$ is not the diffusion voltage.

The total number of states due to depletion and interface can be calculated from the measured capacitance at lower frequency whereas the capacitance at higher frequency is associated with depletion only. The number of interface states can be calculated by using the relation [37]

$$N_{IS} = (C_{LF} - C_{HF})/q, \tag{6}$$

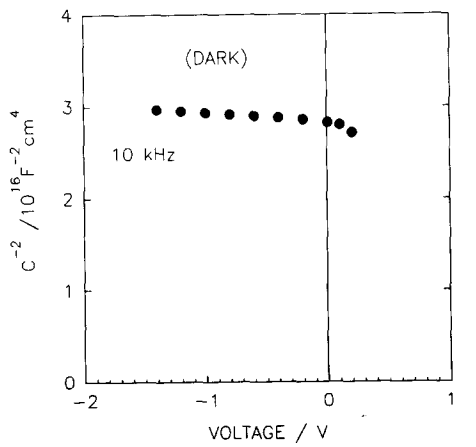

Fig. 10. Mott–Schottky plot at 10 kHz of the cell of fig. 2.

where N_{IS} is the total number of interface states, C_{LF} and C_{HF} are the capacitances at lower (≈ 10 Hz) and higher ($\approx 10^5$ Hz) frequencies, q is the electronic charge. The value of interface states decreased with decreasing temperature. The density of interface states calculated from eq. (6) are 6.4×10^{10} and 1.6×10^{10} cm^{-2} eV^{-1} at 293 K and 231 K respectively.

4. Conclusion

$CdCl_2$ treated CdS/CdTe solar cells have been prepared by electrodeposition technique after $CdCl_2$/methanol treatment. The cell parameters are: $V_{oc} = 758$ mV, $J_{sc} = 21$ mA cm^{-2}, FF = 0.65 and efficiency = 10.3%. Current–voltage–temperature measurements show that the value of the diode factor varies from 1.54 at 324 K to 2.64 at 146 K. Voltage factor, α, varies from 22.83 at 324 K to 29.46 at 146 K. The data of C–V–T measurements indicate that the current transport is controlled by both tunneling and interface recombination. Capacitance–voltage–temperature measurements show that the capacitance increased with decreasing frequency and increased with temperature. Capacitance was insensitive to reverse bias indicating intrinsic or low doped depletion layer. The interface state density calculated from capacitance measurements at low and high frequencies gave the value of 6.4×10^{10} cm^{-2} eV^{-1} in dark at 293 K. The carrier concentration of CdTe layer calculated from Mott–Schottky plot was 1.5×10^{16} cm^{-3}.

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