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Tailoring Electrical Transport Across Grain Boundaries in Polycrystalline Graphene

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Graphene produced by chemical vapor deposition (CVD) is polycrystalline, and scattering of charge carriers at grain boundaries (GBs) could degrade its performance relative to exfoliated, single-crystal graphene. However, the electrical properties of GBs have so far been addressed indirectly without simultaneous knowledge of their locations and structures. We present electrical measurements on individual GBs in CVD graphene first imaged by transmission electron microscopy. Unexpectedly, the electrical conductance improves by one order of magnitude for GBs with better interdomain connectivity. Our study suggests that polycrystalline graphene with good stitching may allow for uniformly high electrical performance rivaling that of exfoliated samples, which we demonstrate using optimized growth conditions and device geometry.

Most three-dimensional electronic materials produced in macroscopic quantities are not homogeneous but incorporate numerous classes of dislocations and defects that degrade electrical performance (*1*). Although large-scale graphene films produced by chemical vapor deposition (CVD) (*2*, *3*) might be expected to be nearly defect free, recent transmission electron microscopy (TEM) studies (*4*, *5*) have shown that these films are polycrystalline. Electrical transport between single-crystal domains could be affected by scattering at the grain boundary (GB), as has been shown theoretically (*6*–*9*). Although TEM has provided a fast and accurate means to identify and image the structure of GBs in CVD graphene, the electrical impact of GBs has so far been studied only indirectly in experiments. Previous work by Huang *et al*. detects no measurable electrical resistance from GBs within instrument limits (*4*), and ensemble measurements done by various groups find very weak correlation between the average domain size of the graphene film and overall device mobility (*4*, *10*). In contrast, Yu *et al*. and Jauregui *et al*. inferred the presence of GBs from the shape of partially grown graphene islands and extracted a finite GB resistance from their measurements (*11*, *12*). The ambiguity in these findings arose from a lack of knowledge of the precise domain morphology for the graphene measured. To this end, we have devised an experimental scheme to first image (using TEM) and then electrically address individual domains and GBs in polycrystalline graphene. Such a capability is crucial, because graphene domain structures generated during synthesis form nontrivial patterns that are strongly dependent on growth conditions and difficult to predict a priori.

In Fig. 1A, we show false-color dark-field TEM (DF-TEM) images of graphene films grown under three different conditions [see supplementary materials (*13*)] taken in a manner similar to Huang *et al*. (*4*). Each colored region corresponds to a separate graphene crystalline domain with distinct lattice orientation. The image is generated by using an aperture in the back-focal plane of the microscope to collect electrons diffracted from only a narrow range of angles by the graphene lattice. In general, different graphene domains produce a diffraction pattern rotated with respect to one another, so each domain can be imaged separately, colorized, and then combined.

In growth A, graphene was synthesized under high reactant flow rates, which produced fast growth and also small average domain size $D \approx 1$ μm. Graphene from growth B was synthesized in a diluted methane environment, whereas growth C was further enclosed in copper foil, after Li *et al*. (*14*), resulting in slower growths. The latter films were terminated after only partial surface coverage to highlight their growth structures. In subsequent microscopy and electrical measurements, however, we used continuous films, for which growth B yielded $D \approx 10$ μm and growth C, $D \approx 50$ μm. The overall shapes of partially grown graphene islands in growth B were polygons, whereas growth C generally formed flowered islands (fig. S1). Despite

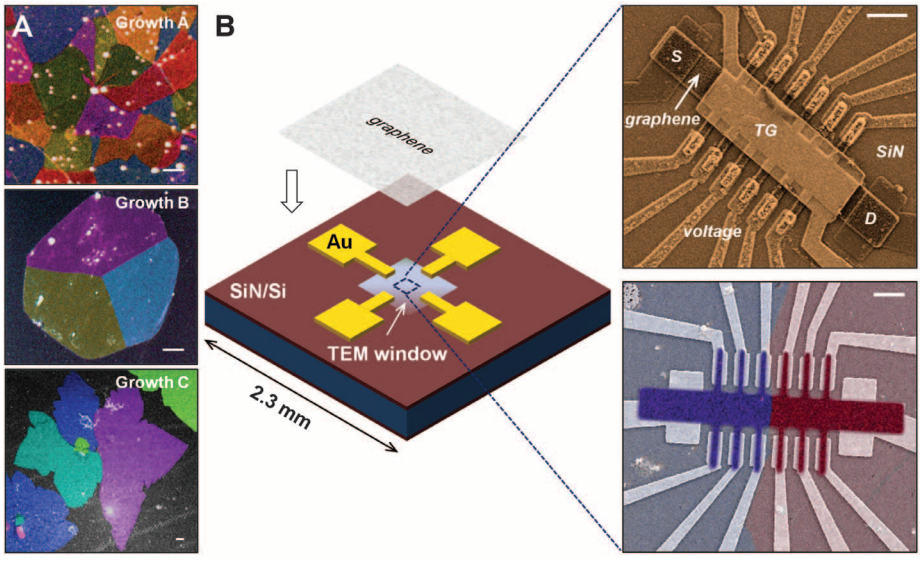

Fig. 1. (**A**) Composite false-color DF-TEM images of CVD graphene produced using three different growth conditions—A, B, and C—yielding average domain size *D* of 1, 10, and 50 μm, respectively, in continuous films. (**B**) (Left) Schematic of specially fabricated TEM chip compatible with electron-beam lithography and electrical measurements. (Top right) SEM image of top-gated, graphene Hall bar device. (Bottom right) Overlaid SEM and DF-TEM images showing device crossing a single GB of two domains from growth C. Scale bars, 1 μm.

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these differences, DF-TEM shows that even a single graphene island can contain several distinct domains, revealing the complexities of graphene growth inherent in even seemingly simple growth structures.

To study the impact of individual GBs on electronic properties, electrical measurements and TEM imaging need to be done in conjunction. However, complicated sample preparation processes and constraints arising from chip geometry make TEM studies currently incompatible with other experimental schemes, such as nanofabrication. Here, we describe a method to electrically address a material with nanometer resolution after TEM characterization. In Fig. 1B (left), we show a schematic of a specially fabricated TEM chip (see supplementary materials and fig. S2) that is 2.33 mm wide on each side, 200 μm thick, and fits standard TEM holders. In the center is a fully suspended, silicon nitride (SiN) TEM window (80 by 80 μm, 20 nm thickness) with metalized alignment marks. On the periphery are large electrical leads and contacts patterned by optical lithography. After graphene was transferred and imaged, we selected an area of interest and used electron-beam lithography to pattern a field-effect transistor device with four-terminal geometry. Raman spectra taken after our TEM imaging suggests that our graphene was not damaged during this process (fig. S3). In three separate lithography steps, we (i) defined electrodes, (ii) patterned the graphene, and (iii) defined a top gate. A completed structure is shown in the scanning electron microscopy (SEM) image on the top right of Fig. 1B. By combining TEM and standard fabrication methods, we electrically addressed individual domains and GBs in CVD graphene with ≈50-nm accuracy. In the bottom right, we show an SEM image of a representative device (before defining the top gate) overlaid with a false-color DF-TEM image of the underlying graphene, consisting of a single GB between two large domains. The areas with faded colors represent graphene that was subsequently etched away, leaving behind only the high-contrast pattern in the center.

We first performed room-temperature transport measurements on a GB from growth A ($D \approx 1$ μm). In the upper inset of Fig. 2A, we show the composite image of a particular device consisting of an individual GB. In the top panel, we plot four-terminal sheet resistance $R_{\square}$ versus gate voltage for the left (L) and right (R) domains, as well as that across the GB (L-R), measured simultaneously for the same gate voltage sweep. The single-domain measurements showed field-effect behavior that was typical for graphene with a Dirac point at $V_{Dirac} \approx 7$ V. More strikingly, the two showed nearly identical values for the entire gated range. The cross-domain measurement showed similar qualitative behavior with a comparable Dirac position. However, L-R exhibited an increased resistance, particularly at gate biases near V_{Dirac}, that we attributed to additional scattering caused by the GB. Also, L-R seemed to scale from single-domain resistivity ($\rho_{\square}$) by a constant factor of 1.4 for all gate values, as shown by the dashed curve. Finally, by subtracting the averaged L and R values from L-R, we can extract the resistivity per micrometer length of the GB itself, ρ_{GB}, which we plot in the bottom panel as a function of gate voltage. ρ_{GB} exhibited a similar gate-tunable behavior as $\rho_{\square}$: It is 4 kΩ-μm at V_{Dirac} and decreased with doping, reaching a saturated value of 0.5 kΩ-μm in the *p*-type regime.

The results of our measurement can be interpreted to describe the presence of a GB as simply an extension of the conductance channel defined by an effective length $\lambda = \rho_{GB}/\rho_{\square}$. When a device of dimensions L and W crossed a GB, resistance increased from the intrinsic, monocrystalline resistance $R = \rho_{\square}(L/W)$ to $R' = \rho_{\square}(L/W) + \rho_{GB}/W = \rho_{\square}(L+\lambda)/W$. Hence, the channel length effectively increased by λ, and both the electrical conductance and the carrier mobility were reduced by a factor $R'/R = 1+\lambda/L$. Because R'/R closely followed a fixed scaling with gate voltage in our measurements, λ was approximately constant and independent of carrier density (fig. S4). This effect, as diagrammed in the lower inset of Fig. 2A, is a key finding of this report. In particular, the introduction and determination of λ (representing GB connectivity), along with average domain size D, will allow tailoring of overall electrical transport in devices of all length scales. For this particular device, we extracted a value of $\lambda \approx 200$ nm.

Different electrical behavior was observed for analogous measurements at a GB from growth C ($D \approx 50$ μm), which we show in Fig. 2B. Here, L

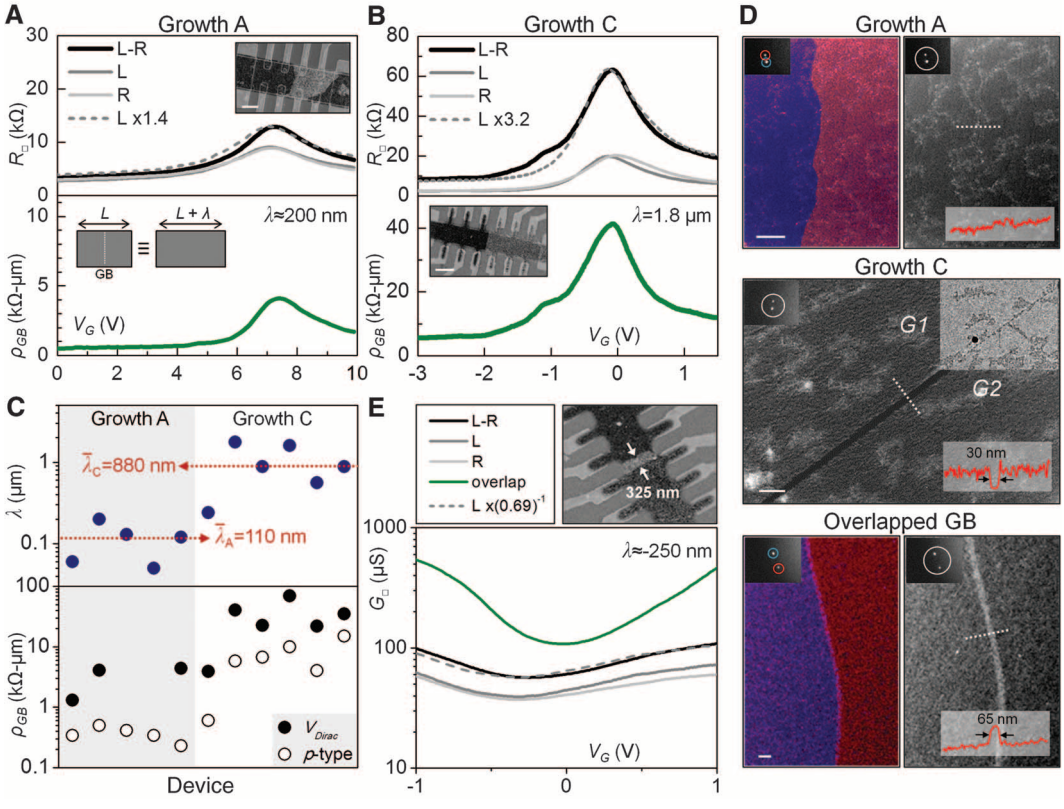

Fig. 2. (**A**) (Top) Four-terminal sheet resistance $R_{\square}$ of device crossing a single GB from growth A (SEM/DF-TEM shown in inset; scale bar, 1 μm) measured in left (L), right (R), and across (L-R) domains as a function of gate bias. L-R scales L by a factor of 1.4. (Bottom) Extracted gate-dependent GB resistivity ρ_{GB}. GB acts to increase channel length by $\lambda \approx 200$ nm at all gate biases. (**B**) Corresponding measurement of more resistive GB from growth C device (scale bar, 1 μm). L-R scales L by 3.2; $\lambda = 1.8$ μm. (**C**) λ and ρ_{GB} (at V_{Dirac} and *p*-type doping) across 11 single-GB devices from growths A and C. Overall, GBs from growth C are an order of magnitude more resistive. (**D**) (Top and middle) Higher resolution DF-TEM images of GBs from suspended growth A and C samples show better stitching from growth A. (Bottom) DF-TEM of overlapped GB often observed in growth C. The diffraction spots and relative aperture positions used to form the images are shown as insets. Scale bars, 100 nm. (**E**) Electrical measurements of device consisting of GB overlapped by 325 nm show improved GB conductance. $\lambda \approx -250$ nm.

and R also showed similar gate dependences, but L-R was considerably greater at all gate values, signifying increased scattering at the GB. In fact, we extracted a gate-dependent GB resistivity (5 to 40 kΩ-μm) that was overall an order of magnitude greater than that measured for growth A. Nevertheless, $R'/R \approx 3.2$ was again roughly constant with gate bias, from which we determined $\lambda = 1.8$ μm for this GB, or twice as long as the device channel itself.

We fabricated 11 graphene devices with a single GB and performed similar measurements (five devices from growth A and six from C). In Fig. 2C, we plot their GB resistivities measured both at V_{Dirac} and with *p*-type doping. Although we observed a range of different values, GBs from growth C were an order of magnitude more resistive overall. We also plot the corresponding gate independent λ values: The mean for growth A samples was 110 nm, and it was 880 nm for C. In contrast, we observe no strong correlation between $\rho_{\square}$ and different growth conditions (fig. S5).

The poorer conductance of GBs from growth C can be explained by careful investigation of their GB structure. Although graphene in growth A exhibited much greater polycrystallinity, it yielded highly uniform coverage of the underlying copper surface. However, for growth C, we often observed many areas between islands with small gaps and overlaps, suggesting a reduced tendency for different domains to stitch (fig. S6). To study the morphology of individual GBs with higher resolution, we suspended separate graphene samples from the same growths on top of perforated SiN chips to examine with DF-TEM. We found distinct classes of GB behavior from growths A and C.

In Fig. 2D (top left), we show a DF-TEM image of a GB between two colored domains from growth A, with their respective diffraction spots circled in the inset. On the right, we take an image of the entire region by selecting both spots simultaneously and see a relatively featureless boundary region, which is further highlighted by the flat intensity profile taken across the boundary along the marked line. Recently, Huang *et al.* have imaged a particular GB of this type with angstrom resolution and demonstrated that it can form an atomically sharp junction locally at the nanometer scale (*4*). In contrast, domains from growth C showed a markedly different behavior, as seen in the middle panel. Here, two domains have physically connected, as can be seen in the bright-field image in the inset, and showed no slack at the boundary despite being suspended. However, selecting the diffraction spots for both domain orientations simultaneously revealed a dark strip 30 nm wide where the domains join. This result implies that this extended boundary region had a structure different from that of the crystals on either side, suggesting that the domains were joined together either by graphitic material at another orientation or by amorphous material, although atomic resolution imaging would be needed to confirm this directly. The presence of grain boundaries with greater crystalline discontinuity for growth C appeared to be a general trend (fig. S7). Additionally, we have observed growth C domains to connect via an overlapping region. An example is shown in the bottom panel of Fig. 2D. Again, the overlap was seen most clearly by selecting diffraction spots from both domains simultaneously, because the double-layered region appeared twice as intense in the dark-field image. Here, one domain extended 65 nm on top of the other, although overlaps as large as 1 μm were observed for longer growths. Similar behavior has also been observed by Robertson *et al.* using atomically resolved TEM imaging (*15*). We therefore conclude that the electrical properties of GBs in CVD graphene are not universal but are, rather, keenly sensitive to growth conditions and reflect the quality of the connection between domains. In particular, the high-reactivity environment from growth A that yielded a faster growth rate could also contribute to better interdomain stitching.

We have also fabricated a device across two domains from growth C that have overlapped at their boundary, which we show in Fig. 2E. Here, the domains overlapped by 325 nm. Instead of an increased cross-domain resistivity, we observed a conductance that was enhanced by a factor of 1.45, which implies an effective negative $\lambda \approx -250$ nm. We also plotted the square conductance from the overlapped graphene exclusively by removing contributions from the L and R domains, and we saw that it was an order of magnitude greater than single-layered graphene. This result suggests that the scattering properties in double-layered graphene are improved from single-layer, so reliable synthesis of grain boundaries with large overlap, if possible, would be an exciting advance. At the same time, we would also expect this effect to be sensitive to the length of overlap, because a narrow overlap could still potentially hinder interdomain transport.

To better understand the origin of GB resistance for our devices with nonoverlapping domains, we plotted in Fig. 3A the GB conductivity $\sigma_{GB} = 1/\rho_{GB}$ as a function of carrier density $n = C|V_G - V_{Dirac}|/e$ for the two devices shown in Fig. 2, A and B, where *C* is the gate capacitance per unit area. The GB from growth A was overall an order of magnitude more conductive, as discussed previously. At low carrier concentrations

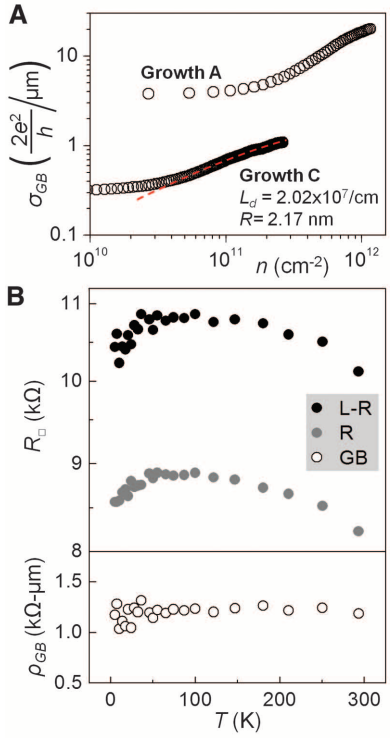

Fig. 3. (**A**) GB conductance as a function of carrier density from data in Fig. 2, A and B. Growth C data are fit to a model of defect scattering from midgap states. (**B**) Temperature dependence of inter- (L-R) and intra- (R) domain resistance from growth A device shows that ρ_{GB} is insensitive to temperature.

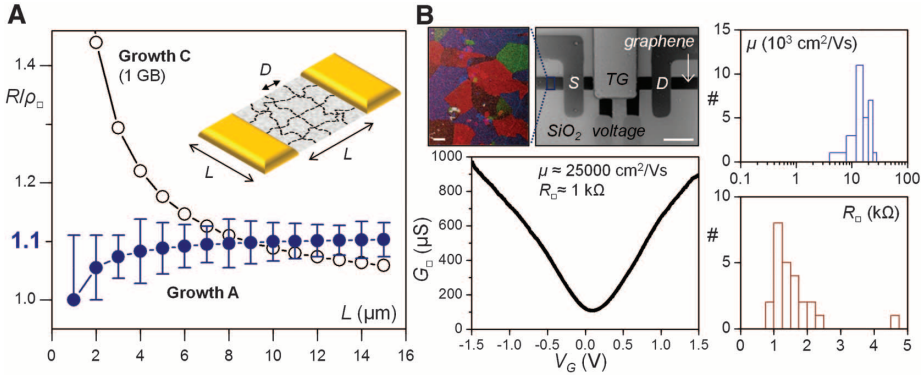

Fig. 4. (**A**) Model of device resistance as a function of device size for growths A and C, using empirically determined λ and *D*. Smaller devices with 1 GB from growth C are very resistive, while growth A devices with the statistically expected number of GBs show uniform high performance over a large range of sizes. (**B**) (Left) Grayscale SEM image (scale bar, 10 μm) of ≈5 by 5 μm growth A–type graphene device fabricated on SiO_2/Si and representative color DF-TEM image (scale bar, 1 μm) of domain structure. Transport characteristics demonstrate performance on par with exfoliated graphene. (Right) Histograms for field-effect mobility and *p*-type sheet resistance of 28 similarly fabricated devices show excellent electrical behavior overall.

near the neutrality point, both values saturated to a minimum as a result of the residual density induced by charge inhomogeneities (*16*). Away from their minima, σ_{GB} increased slightly sublinearly with n. The increase of GB conductance with doping indicates long-range scattering, because weak point disorder is insensitive to carrier density (*17*). Currently, both charge-impurity disorder (*18*) and strong disorder giving rise to midgap states (*19*) are expected to yield conductivity that is roughly linear with carrier density, so it is difficult to untangle these effects a priori. However, the latter predicts increasingly sublinear behavior as the size of the disorder is increased. If we assume that strong disorder dominates the GB resistance in the limit of large ρ_{GB} as from growth C, we can model $\sigma_{GB} = (2e^2/\pi h)(n/L_d)\ln^2(\sqrt{\pi}n\,R)$, where L_d is the linear density of defects at the GB and R is the radius of the defect potential. Fitting our data for growth C to this expression away from the conductivity minimum, we obtained $L_d = 2.0 \pm 0.1 \times 10^7$ cm^{-1}, $R \approx 2$ nm. By comparison, R here was an order of magnitude greater than that modeled from ion-induced single-atom vacancies reported previously (*20*).

Although defect scattering from GBs was sensitive to carrier density, we expected it to be completely insensitive to the effects of temperature. In Fig. 3B, we show the intradomain (R) and cross-domain (L-R) resistivities for another device (growth A), taken simultaneously as a function of temperature from 5 K to 250 K at *p*-type doping. We see similar weak temperature dependence for both measurements, which may be the result of impurities in the graphene or on the substrate for this particular sample (*21*). L-R, however, always appears a fixed value larger throughout, from which we extract a relatively constant GB resistivity of 1 kΩ-μm for the entire temperature range, consistent with our picture of defect-dominated transport.

The results of our TEM and transport measurements on individual GBs in CVD graphene show that the conductance of GBs was highly correlated with their structure. Our data also suggest that it is necessary to control GB connectivity as well as domain size in order to maximize the overall electrical transport properties in polycrystalline graphene. For this, it is essential to develop a systematic understanding of the combined electrical effect of λ (representing GB connectivity) and D (domain size) under various graphene growth conditions and device geometries. Below, we present a simple model based on these two empirically derived parameters that can be used to optimize electrical performance in graphene devices at all length scales.

There are two necessary criteria to uphold in order to successfully integrate CVD graphene into electronic applications. Not only is it important to maximize the performance of individual graphene devices, but achieving uniform performance across many devices is also highly desirable. Because GBs introduce inhomogeneity in the graphene film on the length scale D, a trade-off occurs for the above two criteria. In the limit where device size $L = W << D$, graphene consisting of a single domain will clearly have the best individual performance, as device resistance is $R = \rho_{\square}$. However, devices that cross a GB will have $R = \rho_{\square}(1+\lambda/L)$, which could pose a hindrance if λ is large, such as in growth C. In the opposite limit, where $L >> D$, the devices see $R = \rho_{\square}(1+n\lambda/L)$, where n is the number of GBs crossed. However, we expect $n \approx L/D$, so all devices will see a uniform $R \approx \rho_{\square}(1+\lambda/D)$, which also may not severely degrade performance if λ is small, such as in growth A. The plot in Fig. 4A captures what is described here quantitatively. Here, we calculated normalized device resistance $R/\rho_{\square}$ as a function of device size L up to 15 μm for graphene from the two electrically characterized growths A ($D \approx 1$ μm) and C ($D \approx 50$ μm). The curve in black shows the result of growth C crossing one GB using the empirically obtained $\lambda_C = 880$ nm. Normalized resistance is very large at small L and decreases asymptotically to 1, the intrinsic limit without GBs. The curve in blue shows the result of growth A as the device crosses the expected number of GBs $n = L/D - 1$ (the error bars indicate a $\pm\sqrt{n}$ standard deviation from this number, rounded to the nearest integer). Here, resistance is 1 at small L and slowly increases, as calculated by $\lambda_A = 110$ nm. The two curves cross at $L \approx 9$ μm. However, even above this length, the growth A sample will not severely degrade in performance as resistance eventually saturates to only 10% ($\approx\lambda/D$) larger than the intrinsic limit for monocrystalline graphene. Similarly, device mobility will approach 90% ($\approx 1 - \lambda/D$) of that of a single crystal. Of equal importance, such devices show uniform performance over a large range of lengths with less likelihood of failure for an individual device.

This analysis suggests that well-stitched GBs are not the dominant scattering mechanism to affect large-scale device transport (*22*) and points to an exciting potential for the high electrical performance of polycrystalline graphene. Although the synthesis of growth C could, in principle, be further optimized to achieve large domains together with better GB connectivity, it seems that we can already achieve most of the performance capability of single-crystal graphene in large-scale, polycrystalline devices using our current growth conditions (growth A), despite limited domain size.

We have now demonstrated the performance potential of such samples experimentally, as shown in Fig. 4B. We have fabricated a set of ultra-clean graphene devices on oxidized silicon wafers (≈5 by 5 μm, with 100-nm SiO_2 top gates) using growth A–type synthesis from a semiconductor-grade CVD system that is thoroughly helium leak-checked and conventional lithography without the additional imaging steps of TEM. For a particular high-performance device, we achieved a field-effect mobility of 25,000 cm^2/Vs and sheet resistance of ≈1 kilohm at a relatively low carrier density (~3×10^{11} cm^{-2}) (Fig. 4B, bottom left), on par with that of supported, exfoliated graphene (*16*). The use of boron nitride as a gate dielectric could perhaps be used to further improve device performance (*23*, *24*). On the right, we plotted statistics across 28 similarly fabricated devices and saw that almost all devices had field-effect mobilities above 10,000 cm^2/Vs and resistances below 2 kilohm. Thus, GBs in chemically grown, polycrystalline graphene can be optimized to have a minimal electrical impact on the overall transport properties of the device, in accordance with our model and findings above. We note that our experimental techniques presented here are not limited to the study of graphene but pave the way for electrical studies of other newly reported nanomaterials, such as layered, two-dimensional inorganic compounds and their hybrids (*25*), together with the imaging power of TEM.

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Supplementary Materials

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Figs. S1 to S7
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